- **Bus Transceivers/Registers**

- **Independent Registers and Enables for A and B Buses**

- **Multiplexed Real-Time and Stored Data**

- **Choice of True and Inverting Data Paths**

- **Choice of 3-State or Open-Collector Outputs to A Bus**
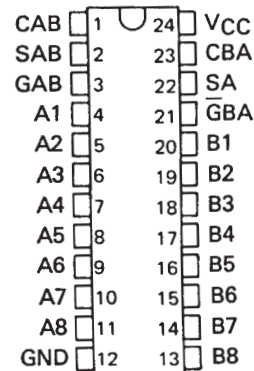
- **Dependable Texas Instruments Quality and Reliability**

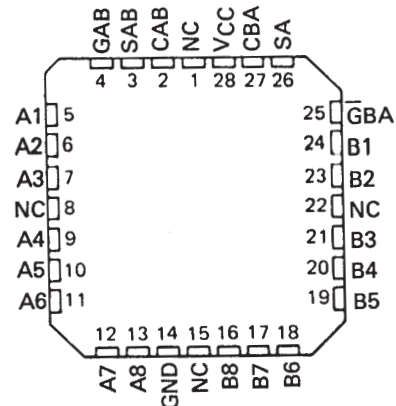| DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS651	3-State	3-State	Inverting
'LS652	3-State	3-State	True
'LS653	Open-collector	3-State	Inverting

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether realtime or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651, 'LS652, and 'LS653.
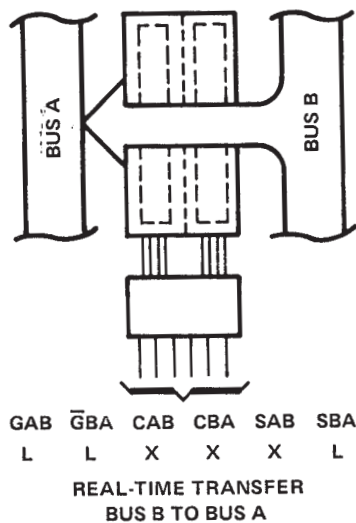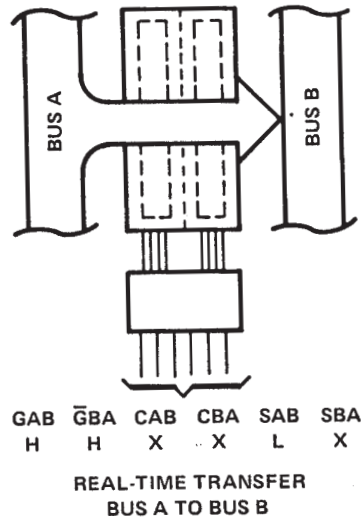
SN54LS' . . . JT PACKAGE
SN74LS' . . . DW OR NT PACKAGE
(TOP VIEW)

CAB	1	24	V_{CC}
SAB	2	23	CBA
GAB	3	22	SA
A1	4	21	$\overline{GBA}$
A2	5	20	B1
A3	6	19	B2
A4	7	18	B3
A5	8	17	B4
A6	9	16	B5
A7	10	15	B6
A8	11	14	B7
GND	12	13	B8

SN54LS' . . . FK PACKAGE
(TOP VIEW)

Top pins (4, 3, 2, 1, 28, 27, 26): GAB, SAB, CAB, NC, VCC, CBA, SA

A1	5	25	$\overline{GBA}$
A2	6	24	B1
A3	7	23	B2
NC	8	22	NC
A4	9	21	B3
A5	10	20	B4
A6	11	19	B5

Bottom pins (12, 13, 14, 15, 16, 17, 18): A7, A8, GND, NC, B8, B7, B6

NC – No internal connection

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

**REAL-TIME TRANSFER
BUS B TO BUS A**

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA
H	H	X	X	L	X

**REAL-TIME TRANSFER
BUS A TO BUS B**

TEXAS
INSTRUMENTS

GAB	GBA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

**STORAGE FROM
A AND/OR B**

GAB	GBA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

**TRANSFER
STORED DATA
TO A AND/OR B**
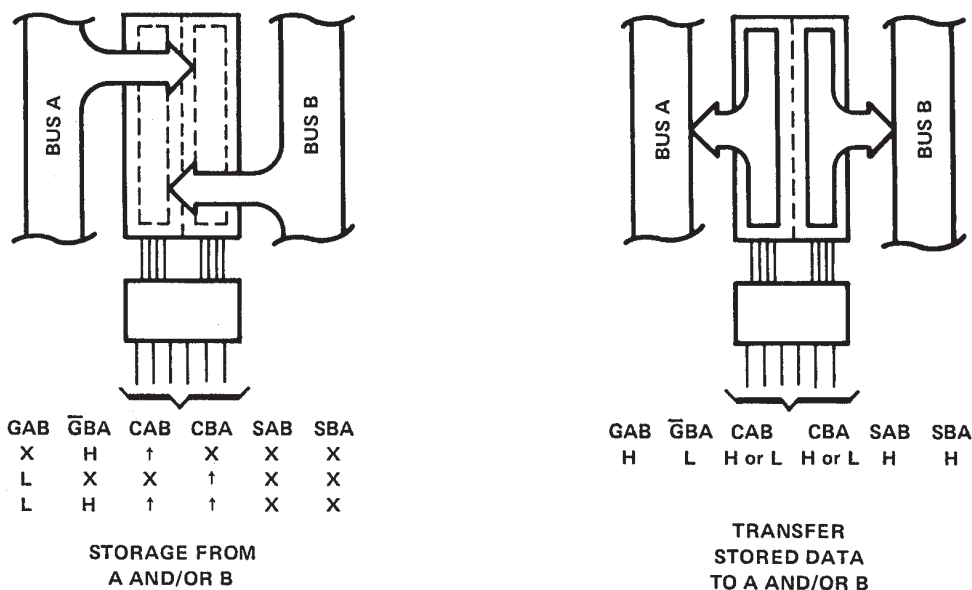
Data on the A or B data bus, or both, can be stored in the internal D flip-flop by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB or SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54LS651 through SN54LS653 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS651 through SN74LS653 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS651, 'LS653	'LS652, 'LS654
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B̄ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B̄ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time Ā Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored Ā Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored Ā Data to B Bus and Stored B̄ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

TEXAS INSTRUMENTS

logic diagrams (positive logic)

'LS651, 'LS653
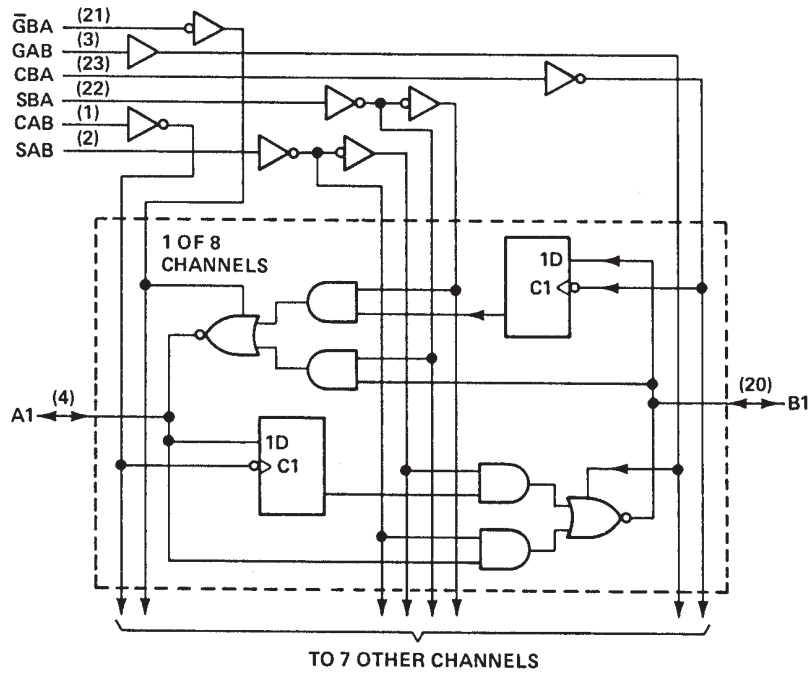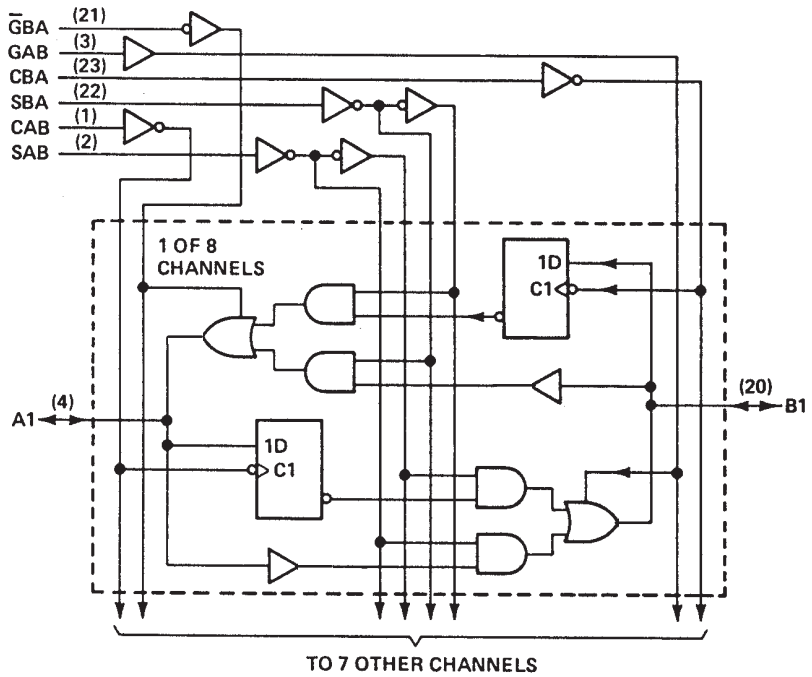
TO 7 OTHER CHANNELS

'LS652

TO 7 OTHER CHANNELS

Pin numbers shown are for DW, JT or NT packages.

logic symbols †

'LS651

'LS652

'LS653
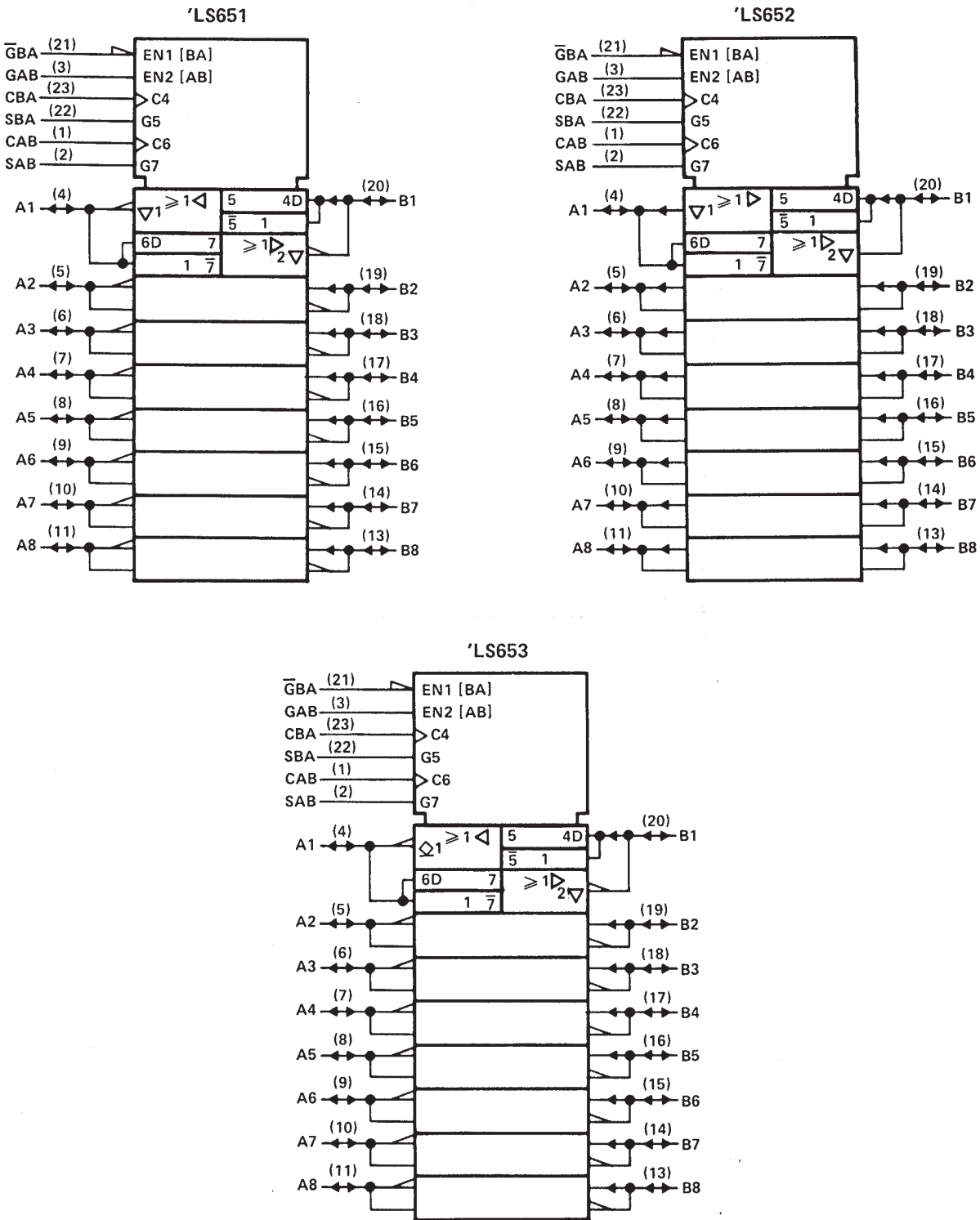
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . .7 V
Input voltage: Control inputs . . . . .7 V
               I/O ports . . . . 5.5 V
Operating free-air temperature range: SN54LS651, SN54LS652 . . . . − 55°C to 125°C
                            SN74LS651, SN74LS652 . . . . 0°C to 70°C
Storage temperature range . . . . − 65°C to 150°C

recommended operating conditions

			SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				− 12			− 15	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CBA or CAB high	15			15			ns
		CBA or CAB low	15			15			
		Data high or low	15			15			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			15			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = − 18 mA			− 1.5			− 1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	I_{OH} = − 3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = − 12 mA	2						
			I_{OH} = − 15 mA				2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
	A or B ports[¶]					20			20	
I_{IL}	Control inputs	V_{CC} = MAX,	V_I = 0.4 V			− 0.4			− 0.4	mA
	A or B ports[¶]					− 0.4			− 0.4	
I_{OS}[§]		V_{CC} = MAX,	V_O = 0 V	− 40		− 225	− 40		− 225	mA
I_{CC}	LS651	V_{CC} = MAX	Outputs high		95	145		95	145	mA
			Outputs low		103	165		103	165	
			Outputs disabled		103	165		103	165	
	LS652		Outputs high		95	145		95	145	
			Outputs low		103	165		103	165	
			Outputs disabled		120	180		120	180	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
[¶] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

TEXAS
INSTRUMENTS

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS651 MIN	'LS651 TYP	'LS651 MAX	'LS652 MIN	'LS652 TYP	'LS652 MAX	UNIT
t_{PLH}	Clock	Bus			14	24		15	25	ns
t_{PHL}	Clock	Bus			23	35		24	36	ns
t_{PLH}	Bus	Bus			9	18		12	18	ns
t_{PHL}	Bus	Bus			20	30		13	20	ns
t_{PLH}	Select, with bus input high†	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		31	47		23	35	ns
t_{PHL}	Select, with bus input high†	Bus			22	33		21	32	ns
t_{PLH}	Select, with bus input low†	Bus			23	35		33	50	ns
t_{PHL}	Select, with bus input low†	Bus			19	30		15	23	ns
t_{PZH}	$\overline{GBA}$	A Bus			29	44		30	45	ns
t_{PZL}	$\overline{GBA}$	A Bus			40	60		36	54	ns
t_{PZH}	GAB	B Bus			19	29		20	30	ns
t_{PZL}	GAB	B Bus			26	40		25	38	ns
t_{PHZ}	$\overline{GBA}$	A Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2		25	38		25	38	ns
t_{PLZ}	$\overline{GBA}$	A Bus			19	30		19	30	ns
t_{PHZ}	GAB	B Bus			25	38		25	38	ns
t_{PLZ}	GAB	B Bus			19	30		19	30	ns

t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
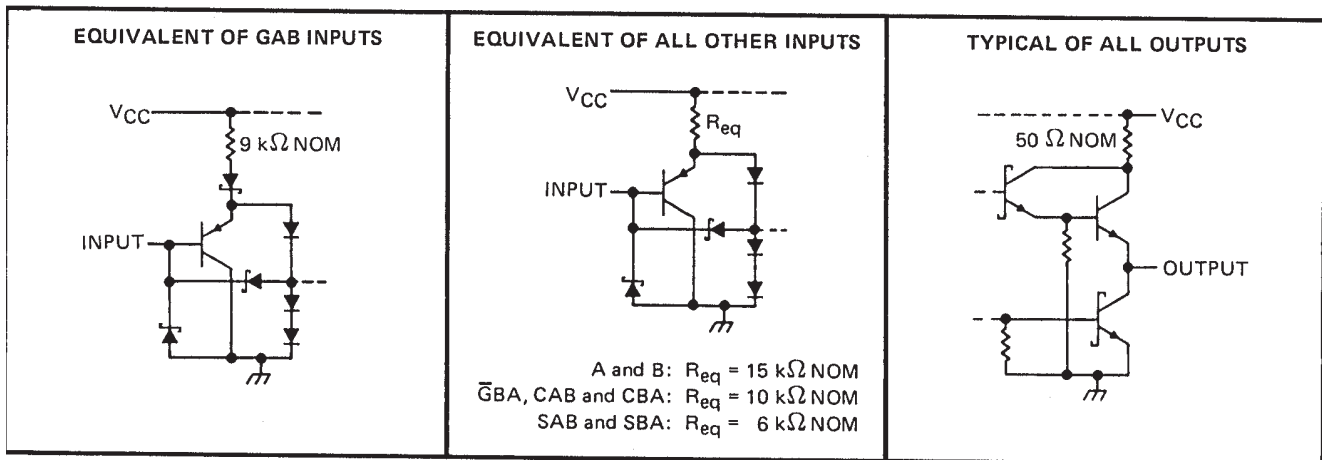t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs

| EQUIVALENT OF GAB INPUTS | EQUIVALENT OF ALL OTHER INPUTS | TYPICAL OF ALL OUTPUTS |

V_{CC} — 9 kΩ NOM — INPUT

V_{CC} — R_{eq} — INPUT

50 Ω NOM — V_{CC} — OUTPUT

A and B: R_{eq} = 15 kΩ NOM
$\overline{GBA}$, CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} .... 7 V
Input voltage: All inputs and A I/O ports 7V
               B I/O ports .... 5.5 V
Operating free-air temperature range: SN54LS653 .... −55°C to 125°C
                           SN74LS653 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

recommended operating conditions

			SN54LS653			SN74LS653			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CBA or CAB high	15			15			ns
		CBA or CAB low	30			30			
		Data high or low	30			30			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			15			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS653			SN74LS653			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	B ports	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = −12 mA	2						
			I_{OH} = −15 mA					2		
I_{OH}	A ports	V_{CC} = MIN,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
	A or B ports ¶					20			20	
I_{IL}	Control inputs	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	A or B ports ¶					−0.4			−0.4	
I_{OS}§	B ports	V_{CC} = MAX,	V_O = 0 V	−40		−225	−40		−225	mA
I_{CC}	LS653	V_{CC} = MAX	Outputs high		95	145		95	145	mA
			Outputs low		103	165		103	165	
			Outputs disabled		103	165		103	165	
	LS654		Outputs high		95	145		95	145	
			Outputs low		105	170		105	170	
			Outputs disabled		120	180		120	180	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	CBA	A Bus			25	38	ns
t_{PHL}					26	39	
t_{PLH}	CAB	B Bus			15	23	ns
t_{PHL}					24	36	
t_{PLH}	A Bus	B Bus			10	18	ns
t_{PHL}					20	30	
t_{PLH}	B Bus	A Bus			21	32	ns
t_{PHL}			R_L = 667 Ω, C_L = 45 pF, See Note 2		16	24	
t_{PLH}	SBA† (with B high)	A Bus			38	57	ns
t_{PHL}					26	39	
t_{PLH}	SBA† (with B low)	A Bus			34	51	ns
t_{PHL}					23	35	
t_{PLH}	SAB† (with A high)	B Bus			32	48	ns
t_{PHL}					22	33	
t_{PLH}	SAB† (with A low)	B Bus			24	36	ns
t_{PHL}					20	30	
t_{PLH}	$\overline{G}$BA	A Bus			23	35	ns
t_{PHL}					37	55	
t_{PZH}	GAB	B Bus			19	29	ns
t_{PZL}			R_L = 667 Ω, C_L = 5 pF, See Note 2		25	38	
t_{PHZ}	GAB	B Bus			26	39	ns
t_{PLZ}					19	29	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs

| EQUIVALENT OF GAB INPUTS | EQUIVALENT OF ALL OTHER INPUTS | TYPICAL OF B OUTPUTS | TYPICAL OF A OUTPUTS |

A and B: R_{eq} = 15 kΩ NOM
$\overline{G}$BA, CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM
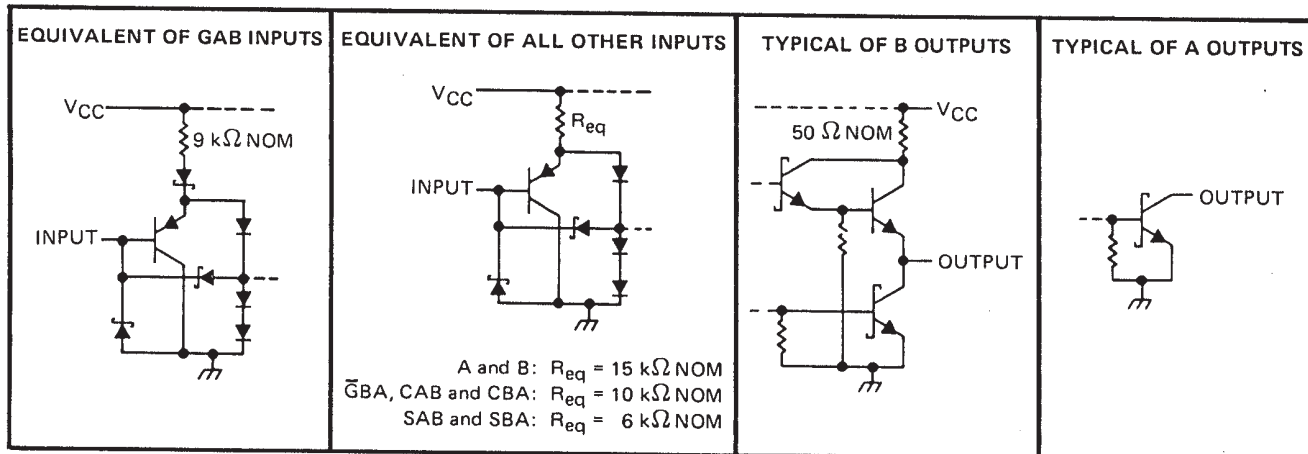
PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LS651DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74LS651DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74LS651NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN74LS652DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS652DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS652DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS652DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS652NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS652NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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