

# SN74GTLPH1655

## 16-BIT LVTTTL-TO-GTL+ ADJUSTABLE-EDGE-RATE UNIVERSAL BUS TRANSCEIVER

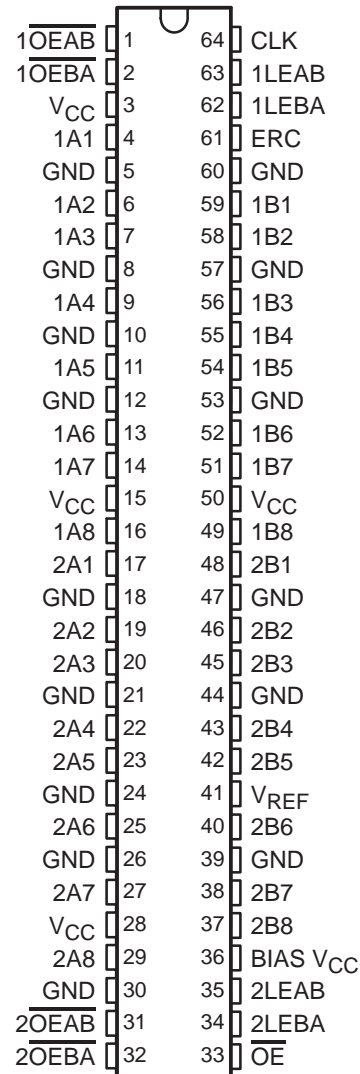
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- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Bidirectional Interface Between GTL+ Signal Levels and LVTTTL Logic Levels**
- **Partitioned as Two 8-Bit Transceivers With Individual Latch Timing and Output Control but With a Common Clock**
- **LVTTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTL+ Outputs (100 mA)**
- **LVTTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTL+ Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity**
- **I<sub>off</sub>, Power-Up 3-State, and BIAS V<sub>CC</sub> Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V<sub>CC</sub> and GND-Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Option Includes Plastic Thin Shrink Small-Outline Package**

### description

The SN74GTLPH1655 is a high-drive 16-bit universal bus transceiver (UBT) that provides LVTTTL-to-GTL+ and GTL+-to-LVTTTL signal-level translation. It is partitioned as two 8-bit transceivers and allows for transparent, latched, and clocked modes of data transfer similar to the '16501 function. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTL+ signal levels. High-speed (about two times faster than standard LVTTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, and output edge control (OEC™). Improved GTLP OEC circuits minimize bus settling time and have been designed and tested using several backplane models. The high drive is suitable for driving double-terminated low-impedance backplanes using incident-wave switching.

DGG PACKAGE  
(TOP VIEW)



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## 16-BIT LVTTTL-TO-GTL+ ADJUSTABLE-EDGE-RATE

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#### description (continued)

GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The AC specification of the SN74GTLPH1655 is given only at the preferred higher noise margin GTL+, but the user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2\text{ V}$  and  $V_{REF} = 0.8\text{ V}$ ) or GTL+ ( $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$ ) signal levels.

Normally, the B port operates at GTL or GTL+ levels, while the A-port and control inputs are compatible with LVTTTL logic levels and are 5-V tolerant.  $V_{REF}$  is the reference input voltage for the B port.

This device is fully specified for live-insertion applications using  $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and  $V_{CC}$  adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ( $\overline{OE}$ ) input should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTLPH1655 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### functional description

The SN74GTLPH1655 is a high-drive (100 mA) 16-bit UBT containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or clocked modes and is similar to a '16501 function. The device is uniquely partitioned as two 8-bit transceivers with individual latch timing and output signals and a common clock for both transceiver words. It can replace any of the functions shown in Table 1.

**Table 1. SN74GTLPH1655 UBT Replacement Functions**

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541
Latched transceiver	'543			'16543
Latch	'373, '573	'843	'841	'16373
Registered transceiver	'646, '652			'16646, '16652
Flip-flop	'374, '574		'821	'16374
SN74GTLPH1655 UBT replaces all above functions				

Data flow for each word is determined by the respective latch enables ( $xLEAB$  and  $xLEBA$ ), output enables ( $xOEAB$  and  $xOEBA$ ), and clock (CLK). The output enables ( $1OEAB$ ,  $1OEBA$ ,  $2OEAB$ , and  $2OEBA$ ) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively. Note that CLK is common to both directions and both 8-bit words.  $\overline{OE}$  also is common and disables all I/O ports simultaneously.

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**functional description (continued)**

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When  $\overline{OEAB}$  is low, the outputs are active. With  $\overline{OEAB}$  high, the outputs are in the high-impedance state.

Data flow for the B-to-A direction is identical, but uses  $\overline{OEBA}$ , LEBA, and CLK.

**Function Tables**

FUNCTION†				OUTPUT B	MODE
INPUTS					
$\overline{OEAB}$	LEAB	CLK	A		
H	X	X	X	Z	Isolation
L	H	X	L	L	Transparent
L	H	X	H	H	Transparent
L	L	↑	L	L	Registered
L	L	↑	H	H	Registered
L	L	H	X	B <sub>0</sub> ‡	Previous state
L	L	L	X	B <sub>0</sub> §	Previous state

† A-to-B data flow is shown. B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLK.

‡ Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

**OUTPUT ENABLE**

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{OEAB}$	$\overline{OEBA}$	A PORT	B PORT
L	L	L	Active	Active
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

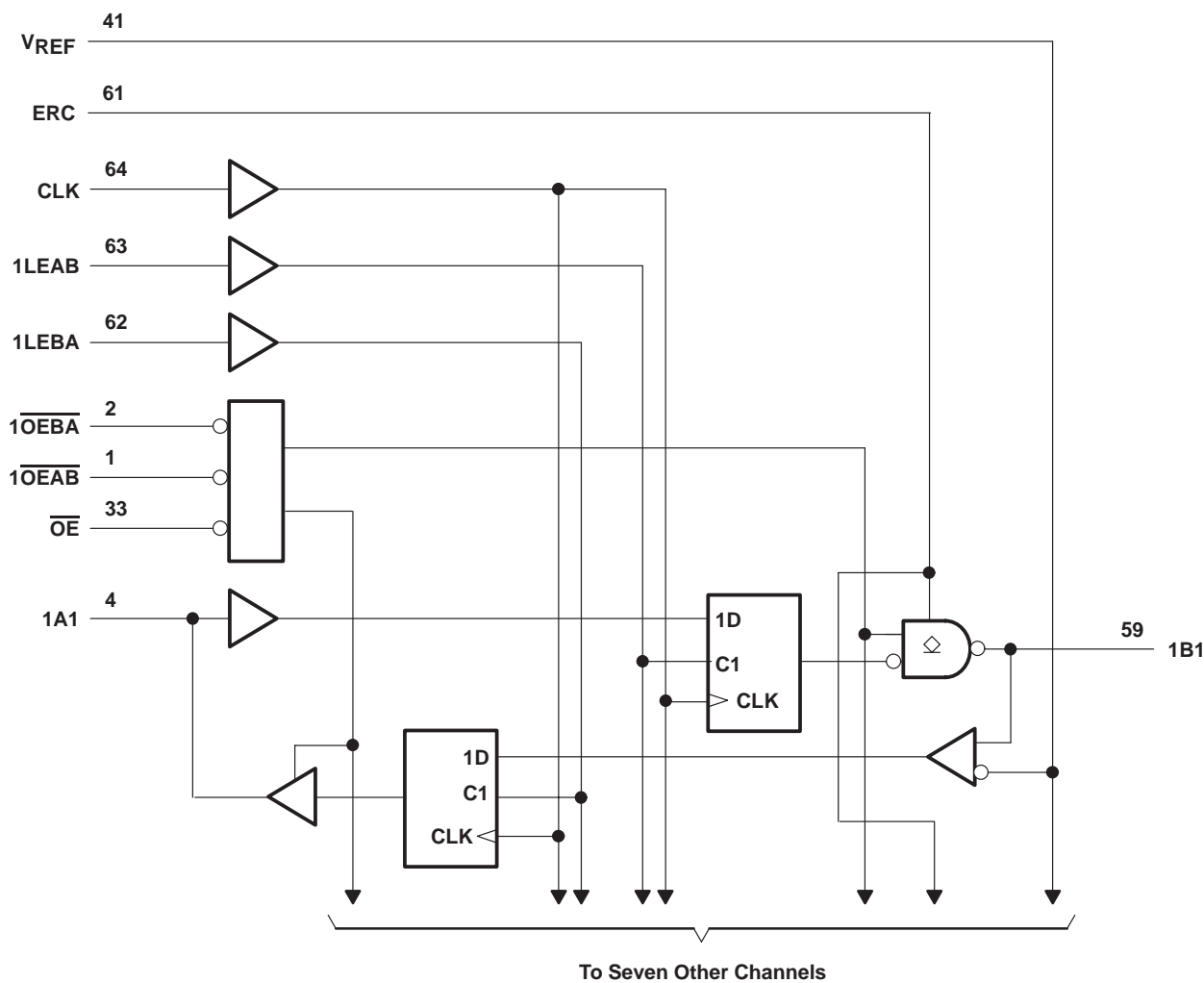
**B-PORT EDGE-RATE CONTROL (ERC)**

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V <sub>CC</sub>	Slow
L	GND	Fast

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**logic diagram (positive logic)**

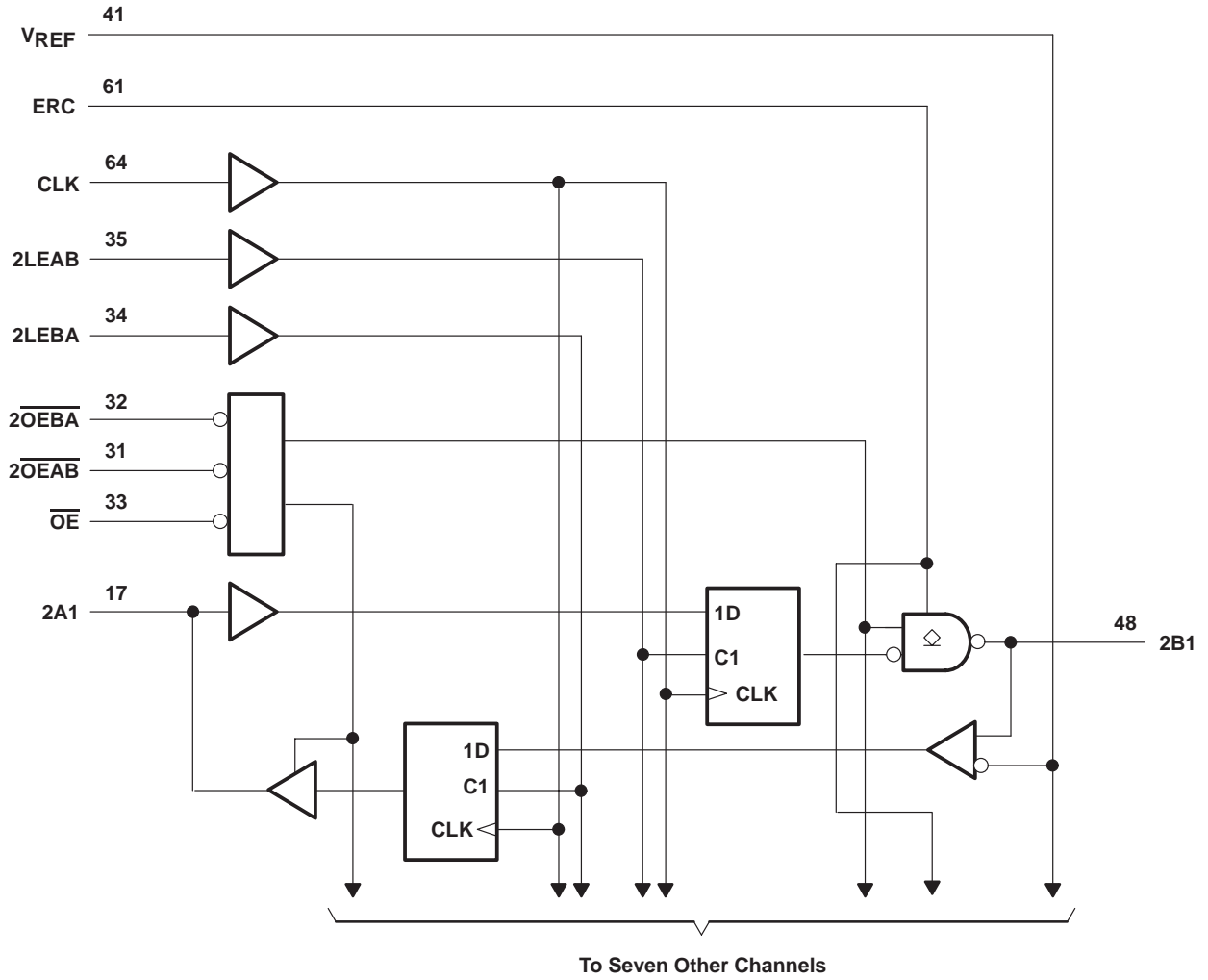


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logic diagram (positive logic) (continued)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ and BIAS $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): A-port and control inputs .....	-0.5 V to 7 V
B port, ERC, and $V_{REF}$ .....	-0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	
(see Note 1): A port .....	-0.5 V to 7 V
B port .....	-0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, $V_O$	
(see Note 1): A port .....	-0.5 V to $V_{CC} + 0.5$ V
B port .....	-0.5 V to 4.6 V
Current into any output in the low state, $I_O$ : A port .....	48 mA
B port .....	200 mA
Current into any A-port output in the high state, $I_O$ (see Note 2) .....	48 mA
Continuous current through each $V_{CC}$ or GND .....	$\pm 100$ mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	55°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51.

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**recommended operating conditions (see Notes 4 through 6)**

		MIN	NOM	MAX	UNIT	
$V_{CC}$ , BIAS $V_{CC}$	Supply voltage	3.15	3.3	3.45	V	
$V_{TT}$	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
$V_{REF}$	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
$V_I$	Input voltage	B port	$V_{TT}$		V	
		Except B port	$V_{CC}$			
$V_{IH}$	High-level input voltage	B port	$V_{REF}+0.05$		V	
		ERC	$V_{CC}-0.6$	$V_{CC}$		
		Except B port and ERC	2			
$V_{IL}$	Low-level input voltage	B port	$V_{REF}-0.05$		V	
		ERC	GND	0.6		
		Except B port and ERC	0.8			
$I_{IK}$	Input clamp current			-18	mA	
$I_{OH}$	High-level output current	A port		-24	mA	
$I_{OL}$	Low-level output current	A port		24	mA	
		B port		100		
$T_A$	Operating free-air temperature	-40		85	°C	

- NOTES: 4. All unused control and B-port inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, BIAS  $V_{CC}=3.3$  V second, and  $V_{CC}=3.3$  V, I/O, control inputs,  $V_{TT}$  and  $V_{REF}$  (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and  $V_{CC}=3.3$  V, BIAS  $V_{CC}=3.3$  V, I/O, control inputs,  $V_{TT}$  and  $V_{REF}$  (any order) last. When  $V_{CC}$  is connected, the BIAS  $V_{CC}$  circuitry is disabled.
6.  $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute  $I_{OL}$  ratings. Similarly,  $V_{REF}$  can be adjusted to optimize noise margins, but normally is  $2/3 V_{TT}$ .

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**electrical characteristics over recommended operating free-air temperature range for GTL+ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 3.15 V, I <sub>I</sub> = -18 mA				-1.2	V
V <sub>OH</sub>	A port	V <sub>CC</sub> = 3.15 V to 3.45 V, I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V
		V <sub>CC</sub> = 3.15 V, I <sub>OH</sub> = -12 mA		2.4			
		V <sub>CC</sub> = 3.15 V, I <sub>OH</sub> = -24 mA		2			
V <sub>OL</sub>	A port	V <sub>CC</sub> = 3.15 V to 3.45 V, I <sub>OL</sub> = 100 μA		0.2			V
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 12 mA		0.4			
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 24 mA		0.5			
	B port	V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 10 mA		0.2			
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 64 mA		0.4			
		V <sub>CC</sub> = 3.15 V, I <sub>OL</sub> = 100 mA		0.55			
I <sub>I‡</sub>	B port	V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 0 to 1.5 V		±10			μA
	A-port and control inputs	V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 0 or V <sub>CC</sub>		±10			
		V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 5.5 V		±20			
I <sub>BHL</sub> §	A port	V <sub>CC</sub> = 3.15 V, V <sub>I</sub> = 0.8 V		75			μA
I <sub>BHH</sub> ¶	A port	V <sub>CC</sub> = 3.15 V, V <sub>I</sub> = 2 V		-75			μA
I <sub>BHLO</sub> #	A port	V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 0 to V <sub>CC</sub>		500			μA
I <sub>BHHO</sub>	A port	V <sub>CC</sub> = 3.45 V, V <sub>I</sub> = 0 to V <sub>CC</sub>		-500			μA
I <sub>CC</sub>	A or B port	V <sub>CC</sub> = 3.45 V, I <sub>O</sub> = 0, V <sub>I</sub> (A-port or control input) = V <sub>CC</sub> or GND, V <sub>I</sub> (B port) = V <sub>TT</sub> or GND		Outputs high		40	mA
				Outputs low		40	
				Outputs disabled		40	
ΔI <sub>CC</sub> ☆		V <sub>CC</sub> = 3.45 V, One A-port or control input at V <sub>CC</sub> - 0.6 V, Other A-port or control inputs at V <sub>CC</sub> or GND		1.5			mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.15 V or 0					pF
C <sub>io</sub>	A port	V <sub>O</sub> = 3.15 V or 0					pF
	B port	V <sub>O</sub> = 1.5 V or 0					

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>I</sub> includes the off-state output leakage current.

§ The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub>max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub>max.

¶ The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub>min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub>min.

# An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

|| An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**live-insertion specifications for A port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I <sub>off</sub>	V <sub>CC</sub> = 0,	BIAS V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V		100	μA
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V,	V <sub>O</sub> = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	μA
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0,	V <sub>O</sub> = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	μA

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**live-insertion specifications for B port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0,$	BIAS $V_{CC} = 0,$	$V_I$ or $V_O = 0$ to 1.5 V		100	$\mu A$
$I_{OZPU}$	$V_{CC} = 0$ to 1.5 V,	$V_O = 0.5$ V to 1.5 V,	$\overline{OE} = 0$		$\pm 100$	$\mu A$
$I_{OZPD}$	$V_{CC} = 1.5$ V to 0,	$V_O = 0.5$ V to 1.5 V,	$\overline{OE} = 0$		$\pm 100$	$\mu A$
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0$ to 3.15 V	BIAS $V_{CC} = 3.15$ V to 3.45 V,	$V_O$ (B port) = 0 to 1.5 V		5	mA
	$V_{CC} = 3.15$ V to 3.45 V				10	$\mu A$
$V_O$	$V_{CC} = 0,$	BIAS $V_{CC} = 3.3$ V		0.95	1.05	V
$I_O$	$V_{CC} = 0,$	BIAS $V_{CC} = 3.15$ V to 3.45 V,	$V_O$ (B port) = 0.6 V	-1		$\mu A$

**timing requirements over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5$  V and  $V_{REF} = 1$  V for GTL+ (unless otherwise noted)**

			MIN	MAX	UNIT
$f_{clock}$	Clock frequency				MHz
$t_w$	Pulse duration	LEAB or LEBA high			ns
		CLK high or low			
$t_{su}$	Setup time	A before CLK			ns
		B before CLK			
		A before LEAB $\downarrow$ , CLK = don't care			
		B before LEBA $\downarrow$ , CLK = don't care			
$t_h$	Hold time	A after CLK			ns
		B after CLK			
		A after LEAB $\downarrow$ , CLK = don't care			
		B after LEBA $\downarrow$ , CLK = don't care			

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$f_{max}$							MHz
$t_{pd}$	A	B	Slow				ns
			Fast				
	LEAB	B	Slow				
			Fast				
	CLK	B	Slow				
			Fast				
$t_{en}$	$\overline{OE}$	B	Slow				ns
$t_{dis}$							
$t_{en}$	$\overline{OE}$	B	Fast				ns
$t_{dis}$							
$t_{en}$	$\overline{OEAB}$	B	Slow				ns
$t_{dis}$							
$t_{en}$	$\overline{OEAB}$	B	Fast				ns
$t_{dis}$							
$t_r$	Rise time, B outputs (0.6 V to 1.3 V)		Slow				ns
			Fast				
$t_f$	Fall time, B outputs (1.3 V to 0.6 V)		Slow				ns
			Fast				
$t_{pd}$	B	A					ns
	LEBA						
	CLK						
$t_{en}$	$\overline{OE}$	A					ns
$t_{dis}$							
$t_{en}$	$\overline{OEBA}$	A					ns
$t_{dis}$							

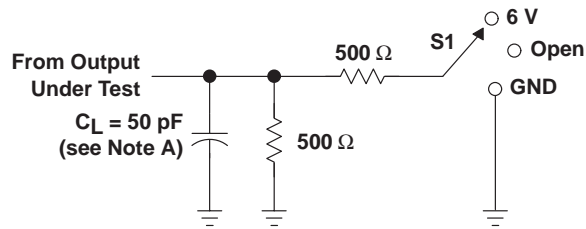
† Slow (ERC =  $V_{CC}$ ) and Fast (ERC = GND)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

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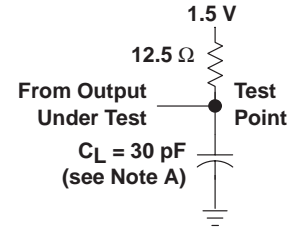


**PARAMETER MEASUREMENT INFORMATION**

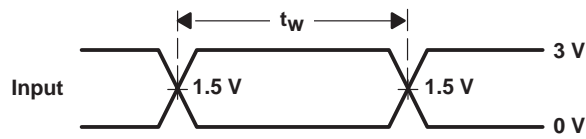


**LOAD CIRCUIT FOR A OUTPUTS**

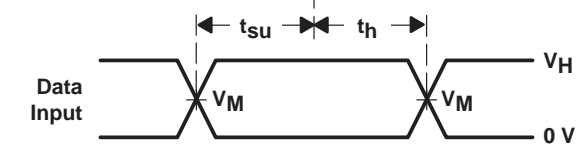
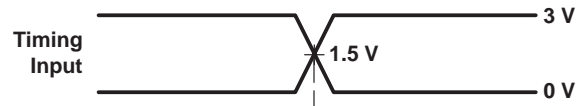
TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	6 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND



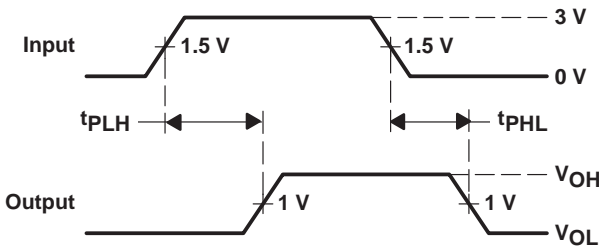
**LOAD CIRCUIT FOR B OUTPUTS**



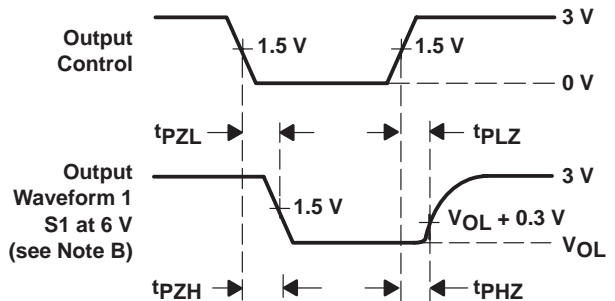
**VOLTAGE WAVEFORMS  
PULSE DURATION**



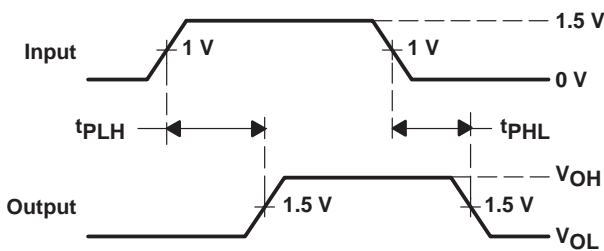
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**  
(VM = 1.5 V for A port and 1 V for B port)  
(VH = 3 V for A port and 1.5 V for B port)



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(A port to B port)**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
(A port)**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(B port to A port)**

- NOTES: A. CL includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, slew rate ≤ 1 V/ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PRODUCT PREVIEW**

**SN74GTLPH1655**  
**16-BIT LVTTTL-TO-GTL+ ADJUSTABLE-EDGE-RATE**  
**UNIVERSAL BUS TRANSCEIVER**

SCES294 – OCTOBER 1999

**DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS**

This data sheet is specified for and tested to the lump load shown in Figure 1. However, the designer probably uses this GTLP device in a distributed load like that shown in Figure 2, in which actual B-port backplane switching characteristics are different. Therefore, the device is modeled as shown in Figure 3, which very closely matches the results obtained using Figure 2. Switching characteristics based on Figure 3 more closely match actual backplane design requirements.

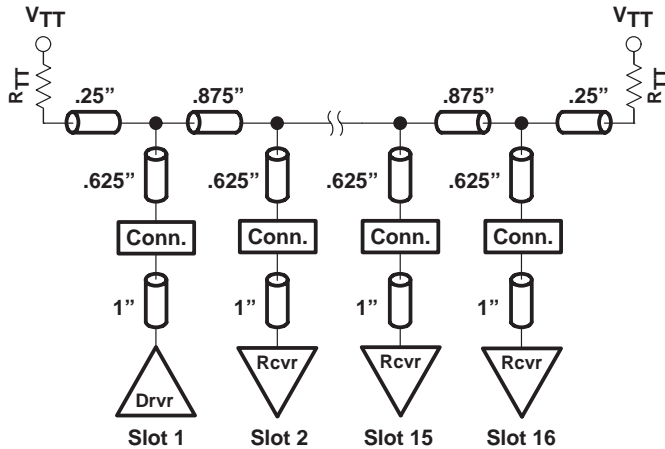


Figure 2. Test Backplane Model

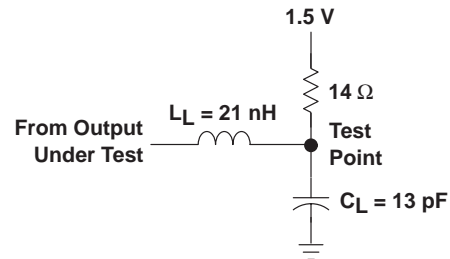


Figure 3. Distributed-Load Circuit for B Outputs

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTL+ (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$f_{max}$							MHz
$t_{pd}$	A	B	Slow				ns
			Fast				
	LEAB	B	Slow				
			Fast				
	CLK	B	Slow				
			Fast				
$t_{en}$	$\overline{OE}$	B	Slow			ns	
$t_{dis}$							
$t_{en}$	$\overline{OE}$	B	Fast			ns	
$t_{dis}$							
$t_{en}$	$\overline{OEAB}$	B	Slow			ns	
$t_{dis}$							
$t_{en}$	$\overline{OEAB}$	B	Fast			ns	
$t_{dis}$							
$t_r$	Rise time, B outputs (0.6 V to 1.3 V)		Slow			ns	
			Fast				
$t_f$	Fall time, B outputs (1.3 V to 0.6 V)		Slow			ns	
			Fast				

† Slow (ERC =  $V_{CC}$ ) and Fast (ERC = GND)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

PRODUCT PREVIEW



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