T-4607-07

54H/74H71

JK MASTER/SLAVE FLIP-FLOP

(With AND-OR Inputs)

DESCRIPTION — The '71 is a high speed JK master/slave flip-flop with AND-OR gate inputs. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from AND-OR gate inputs to master; 3) disable AND-OR gate inputs; 4) transfer information from master to slave. The logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

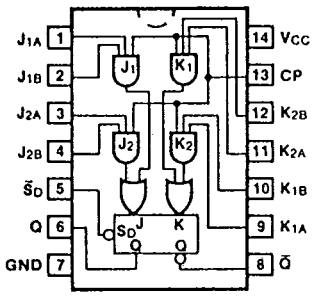
H = HIGH Voltage Level
L = LOW Voltage Level

CLOCK WAVEFORM

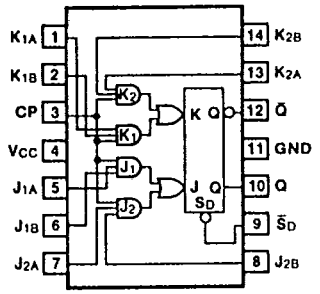
Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

$J = (J_{1A} \cdot J_{1B}) + (J_{2A} \cdot J_{2B})$
$K = (K_{1A} \cdot K_{1B}) + (K_{2A} \cdot K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

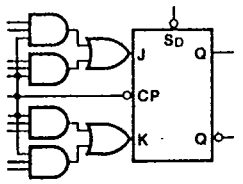
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL



V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

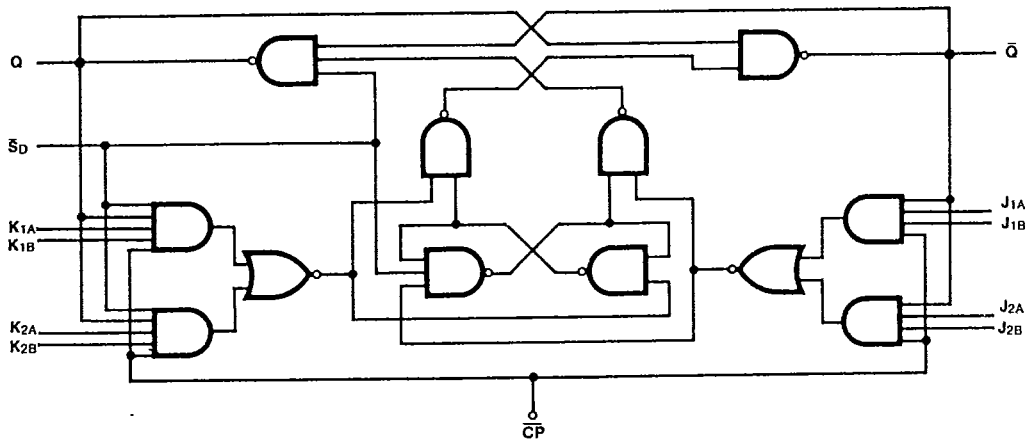
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H71PC		9A
Ceramic DIP (D)	A	74H71DC	54H71DM	6A
Flatpak (F)	B	74H71FC	54H71FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_{1A}, J_{1B}, J_{2A}, J_{2B} K_{1A}, K_{1B}, K_{2A}, K_{2B}	Data Inputs	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	2.5/2.5
$\overline{S}_D$	Direct Set Input (Active LOW)	3.75/3.75
Q, $\overline{Q}$	Outputs	12.5/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		30	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω Min	54/74H C_L = 25 pF R_L = 280 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		21 27	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_D$ to Q or $\overline{Q}$		13 24	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_h (H)	Hold Time HIGH, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_s (L)	Setup Time LOW, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_h (L)	Hold Time LOW, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	12 28		ns	Fig. 3-9
t_w (L)	$\overline{S}_D$ Pulse Width LOW	16		ns	Fig. 3-10