National Semiconductor

MICROCIRCUIT DATA SHEET

MV54ACT109-X REV 0A0

Original Creation Date: 09/26/97
Last Update Date: 07/30/99
Last Major Revision Date: 09/26/97

Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

General Description

The ACT109 consists of two high-speed completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:

LOW input to $\overline{S}$D (Set) sets Q to HIGH level

LOW input to $\overline{C}$D (Clear) sets Q to LOW level

Clear and Set are independent of clock.

Simultaneous LOW on $\overline{C}$D an $\overline{S}$D makes both Q and $\overline{Q}$ HIGH

Industry Part Number

54ACT109

Prime Die

J109

Controlling Document

5962-88534

NS Part Numbers

54ACT109E-QMLV*
54ACT109ERQMLV*
54ACT109J-QMLV**
54ACT109JRQMLV**
54ACT109W-QMLV***
54ACT109WRQMLV***

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25 C
2	Static tests at	+125 C
3	Static tests at	-55 C
4	Dynamic tests at	+25 C
5	Dynamic tests at	+125 C
6	Dynamic tests at	-55 C
7	Functional tests at	+25 C
8A	Functional tests at	+125 C
8B	Functional tests at	-55 C
9	Switching tests at	+25 C
10	Switching tests at	+125 C
11	Switching tests at	-55 C

Features

- Outputs source/sink 24 mA
- ACT109 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - ACT109: 5962-8853401V2A*, VCA**, VDA***
  - ACT109: 5962R8853401V2A*, VCA**, VDA***

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	-0.5V to +7.0V
DC Input Diode Current (Iik)	
Vi = -0.5V	-20 mA
Vi = Vcc +0.5V	+20 mA
DC Input Voltage (Vi)	-0.5V to Vcc +0.5V
DC Output Diode Current (Iok)	
Vo = -0.5V	-20 mA
Vo = Vcc +0.5V	+20 mA
DC Output Voltage (Vo)	-0.5V to Vcc +0.5V
DC Output Source or Sink Current (Io)	$\pm$50 mA
DC Vcc or Ground Current per Output Pin (Icc or Ignd)	$\pm$50 mA
Storage Temperature (Tstg)	-65 C to +150 C
Junction Temperature(Tj)	175 C
Thermal Resistance, junction-to-case (jc)	See MIL-STD-1835
Maximum Power Dissipation (pd)	500 mW
Lead Temperature (soldering, 10 seconds)	+300 C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT TM circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (Vcc)	4.5V to 5.5V
Input Voltage (Vi)	0V to Vcc
Output Voltage (Vo)	0V to Vcc
Operating Temperature (Ta)	-55 C to + 125 C
Minimum Input Edge Rate (Delta V/Delta t)	
AC Devices	
Vin from 0.8V to 2.0V	
Vcc @ 4.5V, 5.5V	125 mV/ns
Maximum High Level Output Current (Ioh)	-24 mA
Maximum Low Level Output Current (Iol)	+24 mA

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp. Range: -55C to 125C.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	High level input Current	VCC=5.5V, VM=5.5V	1, 2	INPUT		0.1	uA	1
			1, 2	INPUT		1.0	uA	2, 3
IIL	Low level input Current	VCC=5.5V, VM=0.0V	1, 2	INPUT		-0.1	uA	1
			1, 2	INPUT		-1.0	uA	2, 3
VOL	Low level output Voltage	VCC=4.5V, VIH=2.0V, VIL=0.8V, IOL=50.0uA	1, 2	OUTPUT		.10	V	1, 2, 3
		VCC=5.5V, VIH=2.0V, VIL=0.8V, IOL=50.0uA	1, 2	OUTPUT		.10	V	1, 2, 3
		VCC=4.5V, VINH=4.5V, VIH=2.0V, VIL=0.8V, IOL=24.0mA	1, 2	OUTPUT		.36	V	1
			1, 2	OUTPUT		.50	V	2, 3
		VCC=5.5V, VINH=5.5V, VIH=2.0V, VIL=0.8V, IOL=24.0mA	1, 2	OUTPUT		.36	V	1
			1, 2	OUTPUT		.50	V	2, 3
VIOL	Dynamic Output current LOW	VCC=5.5V, VINH=5.5V, VIH=2.0V, VIL=0.8V, IOL=50.0mA	1, 2, 5	OUTPUT		1.65	V	1, 2, 3
VOH	High Level Output Voltage	VCC=4.5V, VIH=2.0V, VIL=0.8V, IOH=-50.0uA	1, 2	OUTPUT	4.40		V	1, 2, 3
		VCC=5.5V, VIH=2.0V, VIL=0.8V, IOH=-50.0uA	1, 2	OUTPUT	5.40		V	1, 2, 3
		VCC=4.5V, VINH=4.5V VIH=2.0V, VIL=0.8V, IOH=-24.0mA	1, 2	OUTPUT	3.86		V	1
			1, 2	OUTPUT	3.70		V	2, 3
		VCC=5.5V, VINH=5.5V, VIH=2.0V, VIL=0.8V, IOH=-24.0mA	1, 2	OUTPUT	4.86		V	1
			1, 2	OUTPUT	4.70		V	2, 3
VIOH	Dynamic Output Current HIGH	VCC=5.5V, VIHN=5.5V, VIH=2.0V, VIL=0.8V, IOH=-50.0mA	1, 2, 5	OUTPUT	3.85		V	1, 2, 3
ICCH	Supply Current Outputs HIGH	VCC=5.5V, VINL=0.0V	1, 2	VCC		100	nA	1
			1, 2	VCC		40	uA	2, 3
ICCL	Supply Current Outputs LOW	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 2	VCC		100	nA	1
			1, 2	VCC		40	uA	2, 3
ICCF	Supply Current Functional	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 2	VCC		100	nA	1
			1, 2	VCC		40	uA	2, 3
ICCT	Supply Current per Input	VCC=5.5V, VIHT=VCC-2.1	1, 2	VCC		1.0	mA	1
			1, 2	VCC		1.6	mA	2, 3
VIC+	Positive Input Clamp Voltage	VCC=0.0V, IM=1.0 mA	8, 9	INPUT	0.40	1.50	V	1

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp. Range: -55C to 125C.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIC-	Negative Input Clamp Voltage	VCC=Open, IM=-1.0 mA	8, 9	INPUT	-0.40	-1.5	V	1

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TRISE=3.0ns, TFALL=3.0ns, Temp Range: -55C to 125C.

tpLH(1)	Propagation Delay	VCC=4.5V	3, 4, 7	CP to Q/$\overline{Q}$	1.5	11.0	ns	9
			3, 4, 7	CP to Q/$\overline{Q}$	1.5	14.0	ns	10, 11
tpHL(1)	Propagation Delay	VCC=4.5V	3, 4, 7	CP to Q/$\overline{Q}$	1.5	10.0	ns	9
			3, 4, 7	CP to Q/$\overline{Q}$	1.5	12.0	ns	10, 11
tpLH(2)	Propagation Delay	VCC=4.5V	3, 4, 7	$\overline{CD}$/$\overline{SD}$ to Q/$\overline{Q}$	1.5	9.5	ns	9
			3, 4, 7	$\overline{CD}$/$\overline{SD}$ to Q/$\overline{Q}$	1.5	11.5	ns	10, 11
tpHL(2)	Propagation Delay	VCC=4.5V	3, 4, 7	$\overline{CD}$/$\overline{SD}$ to Q/$\overline{Q}$	1.5	10.0	ns	9
			3, 4, 7	$\overline{CD}$/$\overline{SD}$ to Q/$\overline{Q}$	1.5	12.5	ns	10, 11
ts(H/L)	Setup Time HIGH or LOW	VCC=4.5V	6	Jn/$\overline{Kn}$ to CP	5.5		ns	9, 10, 11
th(H/L)	Hold Time HIGH or LOW	VCC=4.5V	6	Jn/$\overline{Kn}$ to CP	2.0		ns	9, 10, 11
tw(H/L)	CP Pulse Width	VCC=4.5V	6	CP or $\overline{CD}$ or $\overline{SD}$	5.0		ns	9, 10, 11
tw(L)	CP Pulse Width	VCC=4.5V	6	$\overline{CD}$ or $\overline{SD}$ to CP	6.5		ns	9
			6	$\overline{CD}$ or $\overline{SD}$ to CP	7.0		ns	10, 11
trec	Recovery Time	VCC=4.5V	6	$\overline{CD}$ or $\overline{SD}$ to CP	0.5		ns	9, 10, 11
FMAX	Maximum Clock Frequency	VCC=4.5V	6	CP	95		MHz	9
			6	CP	85		MHZ	10, 11

Note 1: SCREEN TESTED 100% ON EACH DEVICE AT +25C & +125C TEMPERATURE, SUBGROUPS 1, 2, 7, & 8.

(Continued)

Note 2: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C, +125C, & -55C TEMPERATURE, SUBGROUPS A1, 2, 3, 7 & 8.
Note 3: SCREEN TESTED 100% ON EACH DEVICE AT +25C TEMPERATURE ONLY, SUBGROUP A9.
Note 4: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C, +125C, & -55C TEMPERATURE, SUBGROUPS A9, 10, & 11.
Note 5: TRANSMISSION LINE DRIVING TEST, GUARDBAND LIMITS SET FOR +25C, 2 MSEC DURATION MAX.
Note 6: GUARANTEED BUT NOT TESTED (DESIGN CHARACTERIZATION)
Note 7: MIN LIMITS GUARANTEED FOR 5.5V BY GUARDBANDING 4.5V MIN. LIMITS.
Note 8: SCREEN TESTED 100% ON EACH DEVICE AT +25C TEMPERATURE ONLY, SUBGROUP A1.
Note 9: SAMPLE TESTED (METHOD 5005, TABLE 1) AT +25C TEMPERATURE ONLY, SUBGROUP A1.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002546	07/30/99	Linda Collins	Initial MDS Release