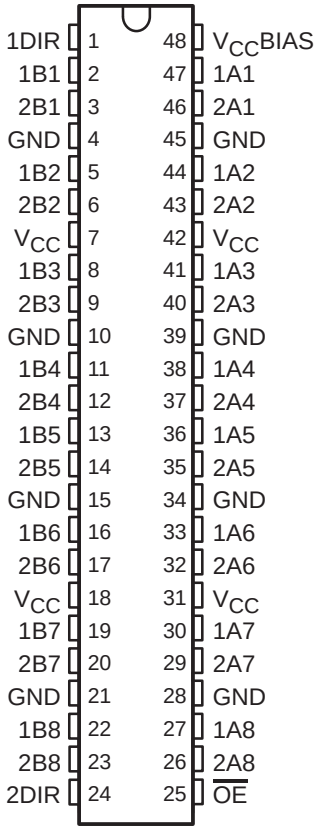
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Support the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Equivalent 25-Ω Series Damping Resistor on B Port**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings**

SN54ABTE16245 . . . WD PACKAGE
SN74ABTE16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The ’ABTE16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has an equivalent 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also on the B port to hold unused or floating inputs at a valid logic level.

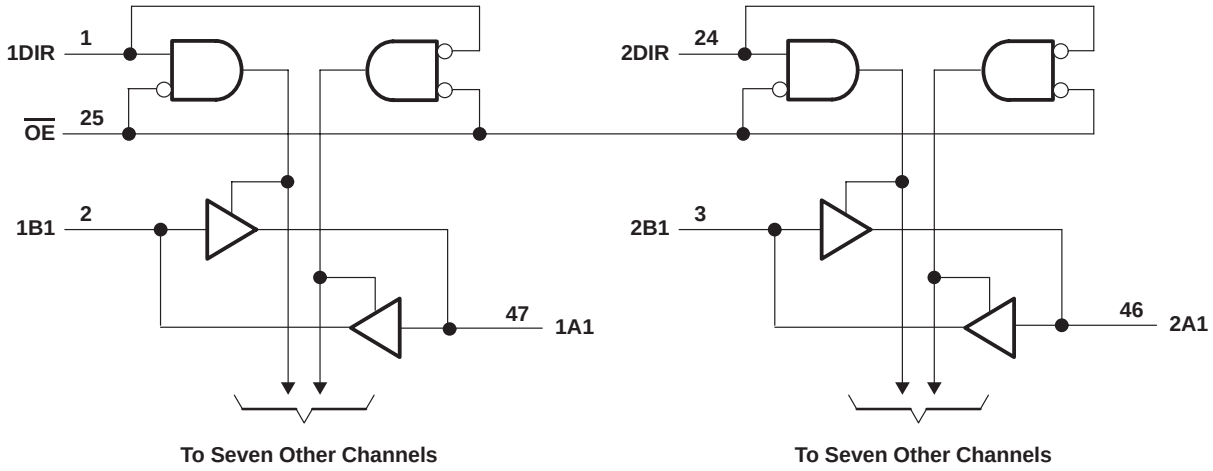
The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN54ABTE16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTE16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54ABTE16245			SN74ABTE16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			2			V
		Except $\overline{OE}$	1.6			1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8			0.8	V
		Except $\overline{OE}$			1.4			1.4	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			–12			–12	mA
		A bus			–24			–60	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTE16245			SN74ABTE16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = –100 μA			V_{CC}–0.2			V_{CC}–0.2	V
		V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4			2.4			
			I_{OH} = –12 mA	2			2			
	A port	V_{CC} = 5.5 V,	I_{OH} = –1 mA			4.5			4.5	
		V_{CC} = 4.5 V	I_{OH} = –32 mA	2.4			2.4			
			I_{OH} = –64 mA				2			
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA			0.4			0.4	V
			I_{OL} = 12 mA						0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA			0.55			0.55	
			I_{OL} = 90 mA						0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V	100			100			μA
			V_I = 2 V	–100			–100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V			±500			±500	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1			±1	μA
	A or B ports	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±20			±20	
I_{OZH}‡	A port	V_{CC} = 5.5 V,	V_O = 2.7 V			10			10	μA
I_{OZL}‡	A port	V_{CC} = 5.5 V,	V_O = 0.5 V			–10			–10	μA
I_O	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–120	–180	–50		–180	mA
	B port			–25	–52	–90	–25		–90	
I_{off}		V_{CC} = 0, V_I or V_O ≤ 4.5 V,	V_{CC}BIAS = 0			±100			±100	μA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		28	36		28	36	mA
			Outputs low		38	48		38	48	
			Outputs disabled		20	32		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V, C_L = 50 pF	$\overline{OE}$ high		0.02			0.02		mA/ MHz
			$\overline{OE}$ low		0.33			0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V				10		2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V				13		4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54ABTE16245			SN74ABTE16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V, V_{CC}BIAS = 4.5 V to 5.5 V, $I_{O(DC)}$ = 0			250	700		250	700	µA
		V_{CC} = 4.5 V to 5.5 V‡, V_{CC}BIAS = 4.5 V to 5.5 V, $I_{O(DC)}$ = 0				20			20	
V_O	A port	V_{CC} = 0	V_{CC}BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
			V_{CC}BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I_O	A port	V_{CC} = 0	V_O = 0, V_{CC}BIAS = 4.5 V	–20		–100	–20		–100	µA
			V_O = 3 V, V_{CC}BIAS = 4.5 V	20		100	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	3.3	4.2	1.5	5.4	1.5	5.2	ns
t_{PHL}			1.5	3.8	4.6	1.5	5.4	1.5	5.2	
t_{PLH}	B	A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}			1.5	3.1	4	1.5	4.7	1.5	4.5	
t_{PZH}	$\overline{OE}$	A	2	3.9	5.3	2	6.4	2	6.2	ns
t_{PZL}			2	4.4	5.9	2	7	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.5	6	2	7.3	2	7.1	ns
t_{PZL}			2	5	6.4	2	7.5	2	7.3	
t_{PHZ}	$\overline{OE}$	A	2	4.9	5.9	2	7	2	6.7	ns
t_{PLZ}			2	3.7	4.6	2	5.4	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2	5.2	6.2	2	7.2	2	7	ns
t_{PLZ}			2	4	5	2	5.8	2	5.5	

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

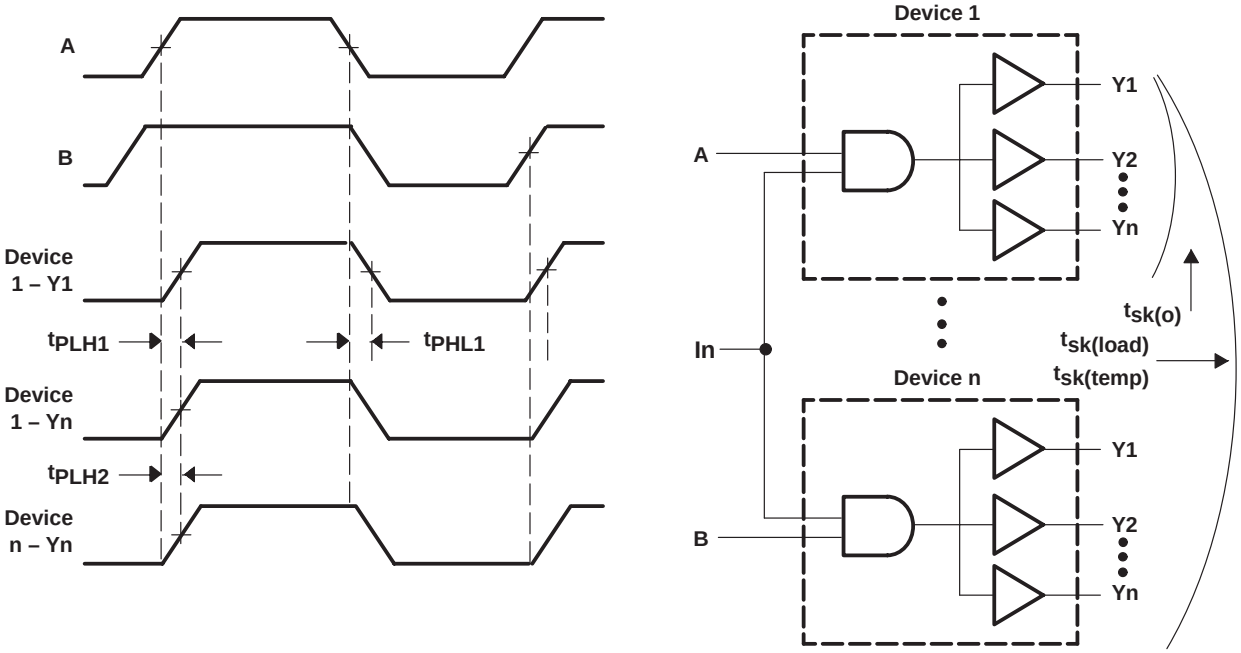
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	B	A	R_X = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PLH}	B	A	R_X = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PLH}	B	A	R_X = 56 Ω	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2		2	ns
	A	B			0.4	0.8		2		2	
	B	A	R_X = 26 Ω		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3		1.3	ns
	A	B			0.7	1.1		1.3		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

† t_t is measured between 1 V and 2 V of the output waveform.
‡ t_t is measured between 10% and 90% of the output waveform.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16245		SN74ABTE16245		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	V_{CC} = constant, ΔT_A = 20°C			3		2.5	ns
	B	A		R_X = 56 Ω		4.5		4	
$t_{sk(load)}$	B	B	V_{CC} = constant, Temperature = constant	R_X = 13, 26, or 56 Ω		4.5		4	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

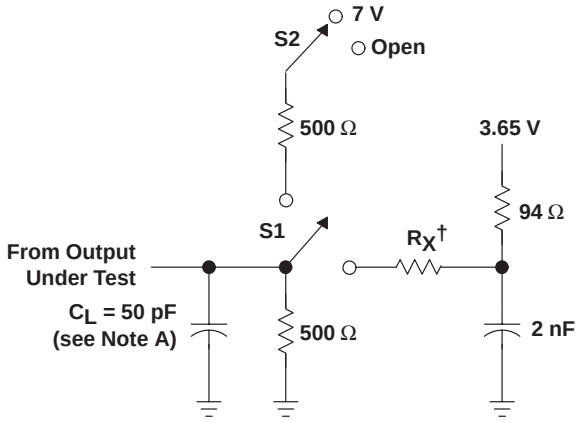
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of any two outputs of the same device switching in the same direction (e.g., $|t_{PLH1} - t_{PLH2}|$).

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of $V_{CC} \pm 1\%$ and with package temperature differences of 20°C.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

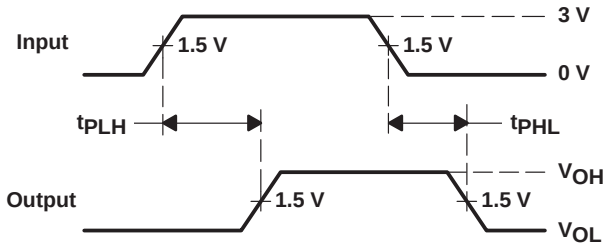


† R_X = 13, 26, or 56 Ω

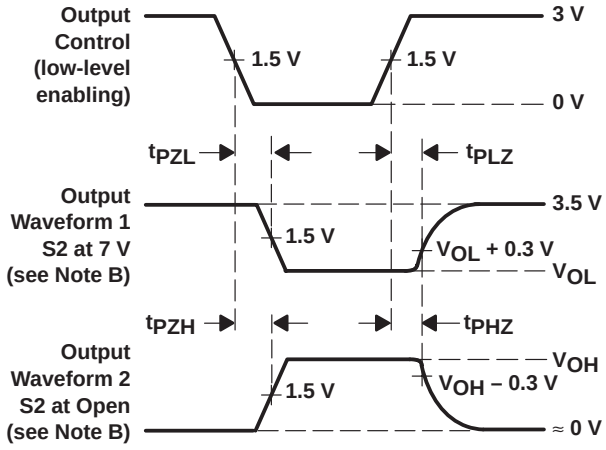
LOAD CIRCUIT FOR OUTPUTS

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (A and B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured between 1 V and 2 V of the output waveform.
F. t_t is measured between 10% and 90% of the output waveform.

Figure 2. Load Circuit and Voltage Waveforms

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