



# 74BCT125

## Quad Buffer with TRI-STATE® Outputs

### General Description

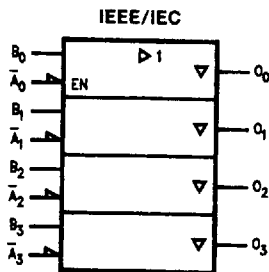
The 74BCT125 is a quad buffer with TRI-STATE outputs designed to be employed as a memory and address driver or bus-oriented transmitter/receiver. Each output is disabled by its own associated  $\bar{A}_n$ .

### Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Low  $I_{CCZ}$  through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 2000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down ( $I_{ZZ}$  and  $V_{ID}$ )

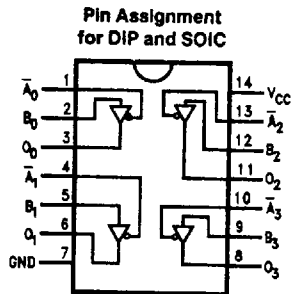
**Ordering Code:** See Section 11

### Logic Symbol



TL/F/10946-1

### Connection Diagram



TL/F/10946-2

Pin Names	Description
$\bar{A}_n, B_n$	Inputs
$O_n$	Outputs

### Function Table

Inputs		Output
$\bar{A}_n$	$B_n$	$O$
L	L	L
L	H	H
H	X	Z

H = High Voltage Level  
 L = LOW Voltage Level  
 Z = High Impedance  
 X = Immaterial

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Any Output in the Disable or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	2000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V <sub>CC</sub> + 4.5V

### Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

### DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4			V	Min	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -15 mA
		2.0					
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-50	μA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			100	μA		0V-2.7V V <sub>OUT</sub> = 2.7V
				20			2.7V-5.5V
I <sub>OZL</sub>	Output Leakage Current			-20	μA		V <sub>OUT</sub> = 0.5V
I <sub>OZ</sub>	Output Leakage Current			±100	μA		0V-2.7V $\bar{A}_n = 0.8V, V_{OUT} = 0.5V$ or 2.7V (Power Up)
				±20	μA		2.4V-0V $\bar{A}_n = 0.8V, V_{OUT} = 0.5V$ or 2.7V (Power Down)
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA (All Other Pins Grounded)
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		8	20	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		18	30	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		6	12	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT			74BCT		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	1.6 2.7	3.6 6.3	5.2 7.5	1.6 2.7	5.7 7.7	ns	8-3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	3.4 5.0	6.5 7.8	9.0 10.4	3.4 5.0	10.3 11.0	ns	8-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	3.0 2.8	5.4 6.0	7.4 7.9	3.0 2.8	8.6 8.6	ns	8-5
t <sub>OSSL</sub> (Note 1)	Pin to Pin Skew HL Data to Output			0.6		0.75	ns	
t <sub>OSLH</sub> (Note 1)	Pin to Pin Skew LH Data to Output			0.4		0.5	ns	
t <sub>OST</sub> (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.5		3.7	ns	
t <sub>PV</sub> (Note 2)	Device to Device Skew LH/HL Data to Output			3.8		4.0	ns	

**Extended AC Electrical Characteristics:** See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT		74BCT		74BCT		Units	Fig. No.
		T <sub>A</sub> = Com V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF 4 Outputs Switching (Note 3)		T <sub>A</sub> = Com V <sub>CC</sub> = Com C <sub>L</sub> = 250 pF 1 Output Switching (Note 4)		T <sub>A</sub> = Com V <sub>CC</sub> = Com C <sub>L</sub> = 250 pF 4 Outputs Switching (Notes 3, 4)			
		Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	3.0 3.0	6.5 8.5	3.0 3.0	8.0 10.0	4.0 4.0	9.0 11.5	ns	8-3
t <sub>OSSL</sub> (Note 1)	Pin to Pin Skew HL Data to Output		0.8		1.2		1.3	ns	
t <sub>OSLH</sub> (Note 1)	Pin to Pin Skew LH Data to Output		0.6		0.8		0.9	ns	
t <sub>OST</sub> (Note 1)	Pin to Pin Skew LH/HL Data to Output		3.8		4.4		4.8	ns	
t <sub>PV</sub> (Note 2)	Device to Device Skew LH/HL Data to Output		4.0		4.8		4.9	ns	

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t<sub>OSSL</sub>), LOW to HIGH (t<sub>OSLH</sub>), or any combination switching LOW to HIGH and/or HIGH to LOW (t<sub>OST</sub>).

**Note 2:** Propagation delay variation for a given set of conditions (i.e., temperature and V<sub>CC</sub>) from device to device.

**Note 3:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

**Note 4:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.



**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Control Inputs	4.0	pF	V <sub>CC</sub> = 5.0V
C <sub>OUT</sub>	Output Pin Capacitance	9.0	pF	V <sub>CC</sub> = 5.0V