SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2829, JANUARY 1986—REVISED MARCH 1988

- **Functionally Equivalent to AMD AM29825 and AM29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include "Small-Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effect**
- **Dependable Texas Instruments Quality and Reliability**

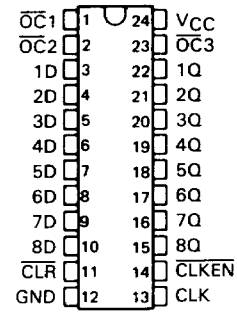
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

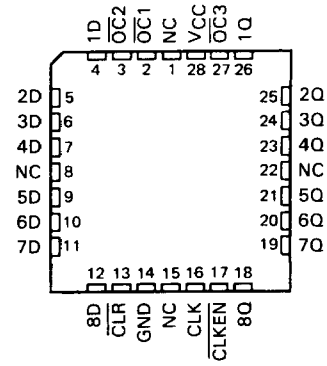
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29825 has non-inverting D inputs and the 'ALS29826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need

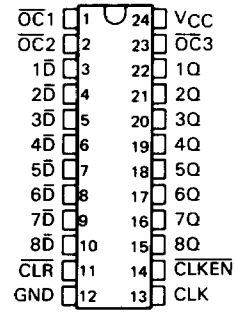
SN74ALS29825 . . . DW OR NT PACKAGE
(TOP VIEW)



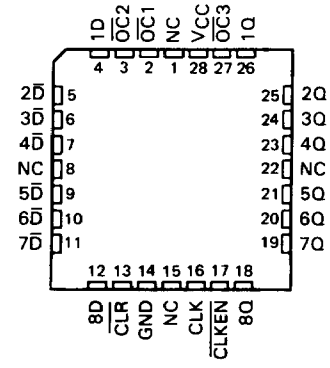
SN74ALS29825 . . . FN PACKAGE
(TOP VIEW)



SN74ALS29826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS29826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

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description (continued)

for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALS29825 and SN74ALS29826 are characterized for operation from 0°C to 70°C.

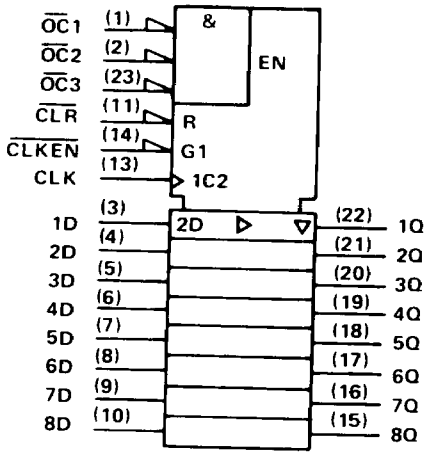
'ALS29825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or OC3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and OC3 are low

logic symbol†

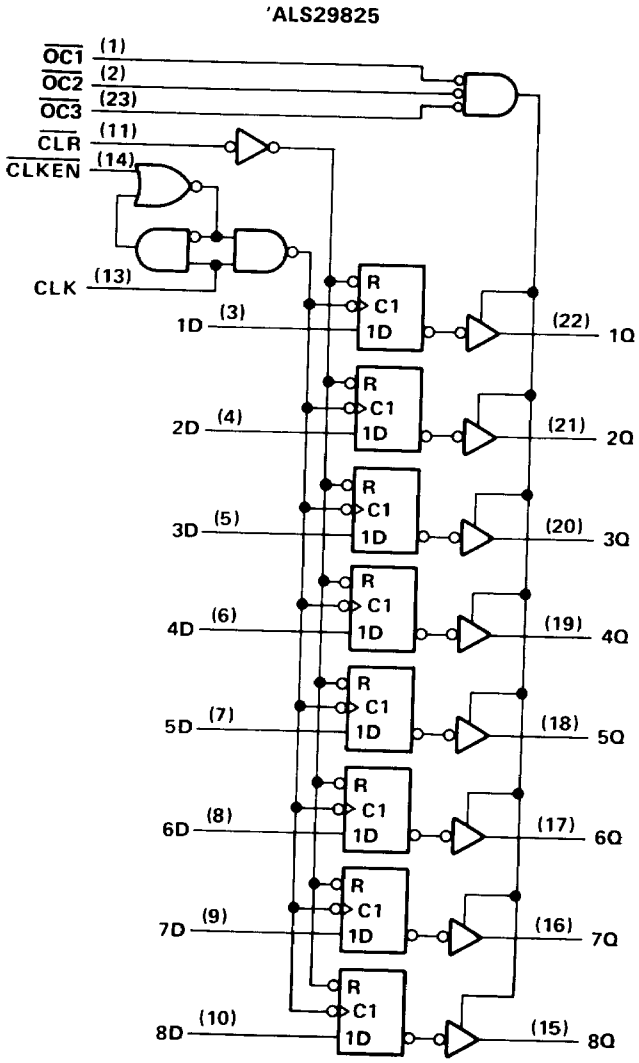
'ALS29825



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW and NT packages.

logic diagram (positive logic)

'ALS29825



Pin numbers are for DW and NT packages.

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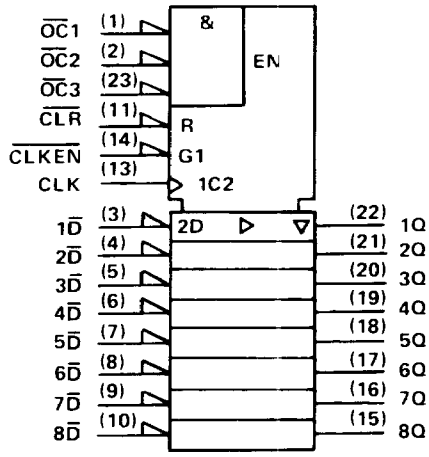
'ALS29826 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or OC3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and OC3 are low

logic symbol†

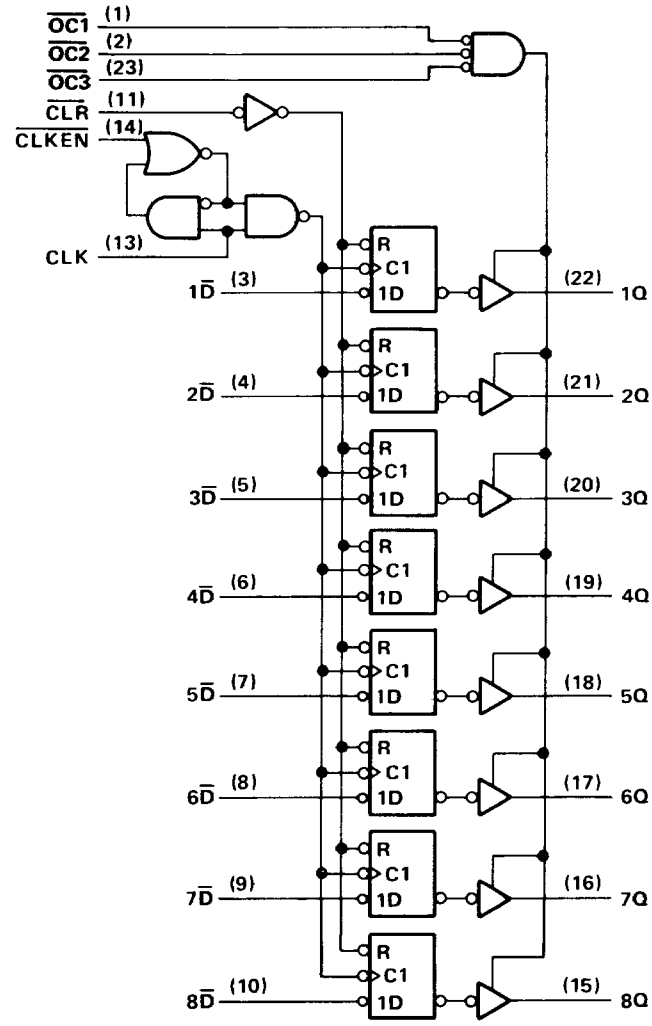
'ALS29826



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW and NT packages.

logic diagram (positive logic)

'ALS29826



Pin numbers are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			5		4.75	5	5.25	V
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
I_{OH}	High-level output current							−24	mA
I_{OL}	Low-level output current							48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			7			ns
		CLK high	5			7			
		CLK low	5			7			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	5			7			ns
		Data	2			4			
		$\overline{CLKEN}$ high or low	6			6			
t_h	Hold time, data after CLK↑	Data	2			2			ns
		$\overline{CLKEN}$	0			2			
T_A	Operating free-air temperature			25		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		V
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2	3.1		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.4 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0 V	−75		−250	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs open		70	100	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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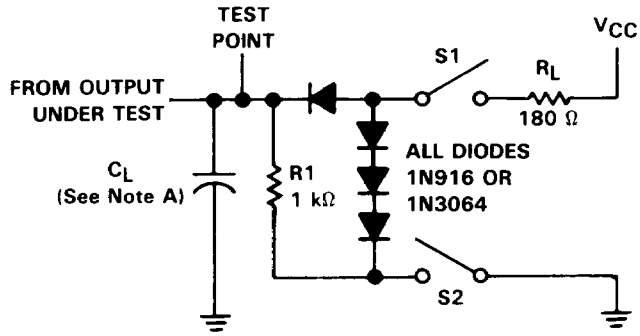
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX†		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2		8.5	2	10	ns
t_{PHL}				2		8.5	2	10	
t_{PLH}			C_L = 300 pF			14		16	
t_{PHL}						14		16	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		6	10		12	ns
t_{PZH}	$\overline{OC}$	Any Q	C_L = 50 pF		11.5	12		14	ns
t_{PZL}					11	12		14	
t_{PZH}			C_L = 300 pF			17		20	
t_{PZL}						21		23	
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF			11		14	ns
t_{PLZ}						9		12	
t_{PHZ}			C_L = 5 pF		5.2	8		9	
t_{PLZ}					5.2	8		9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

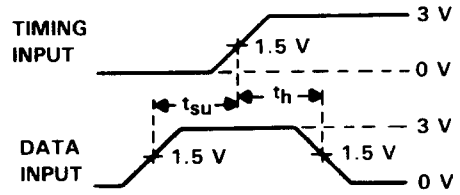
PARAMETER MEASUREMENT INFORMATION



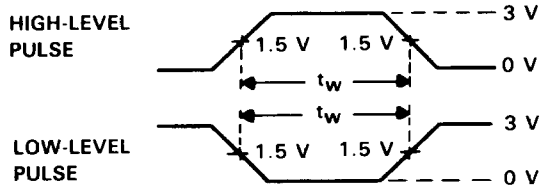
LOAD CIRCUIT

SWITCH POSITION TABLE

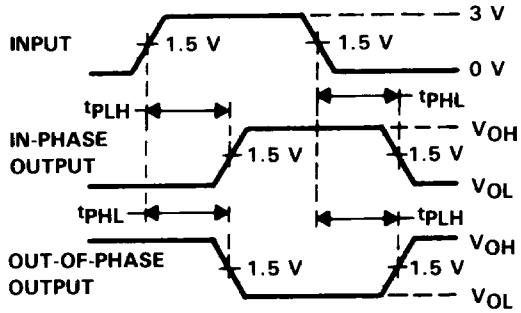
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



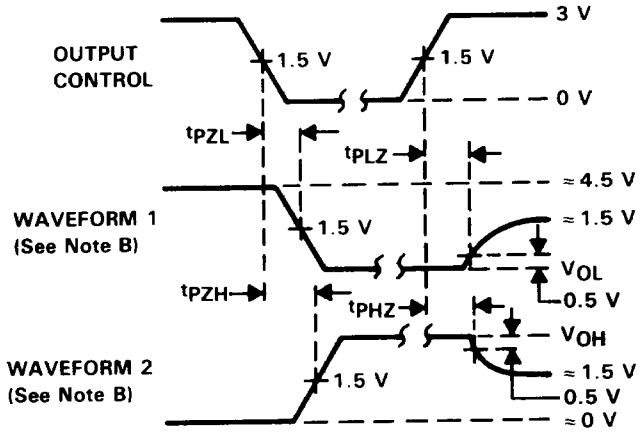
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

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