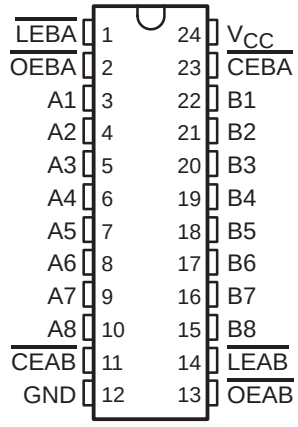
- **BiCMOS Technology With Low Quiescent Power**
- **Buffered Inputs**
- **Inverted Outputs**
- **Input/Output Isolation From V_{CC}**
- **Controlled Output Edge Rates**
- **64-mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7 V**
- **SCR Latch-Up-Resistant BiCMOS Process and Circuit Design**
- **Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (EN) DIP**

EN, M, OR SM PACKAGE
(TOP VIEW)



description

The CD74FCT543 is an octal register/transceiver with 3-state outputs that uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC}. This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A1 to A8 or to take data from B1 to B8. When $\overline{CEAB}$ is low, a low signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The CD74FCT543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

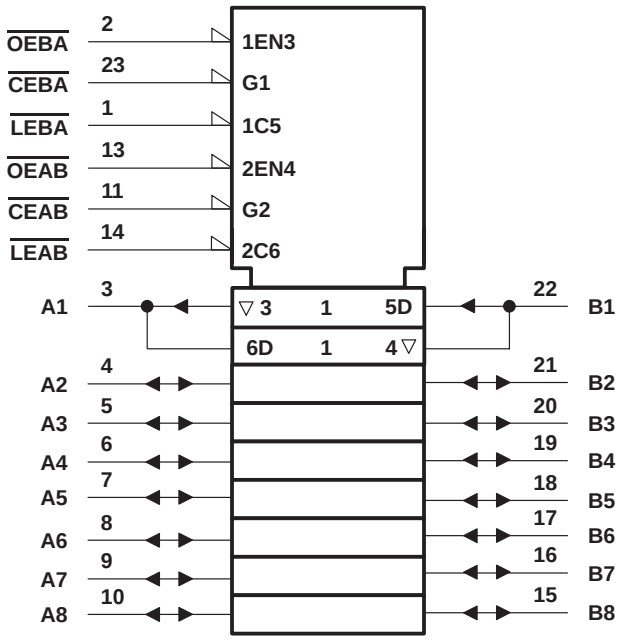
The CD74FCT543 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE†

INPUTS				LATCH STATUS	OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A		
H	X	X	X	Storing	Z
X	X	H	X	–	Z
L	H	L	X	Storing	B_0‡
L	L	L	L	Transparent	L
L	L	L	H	Transparent	H

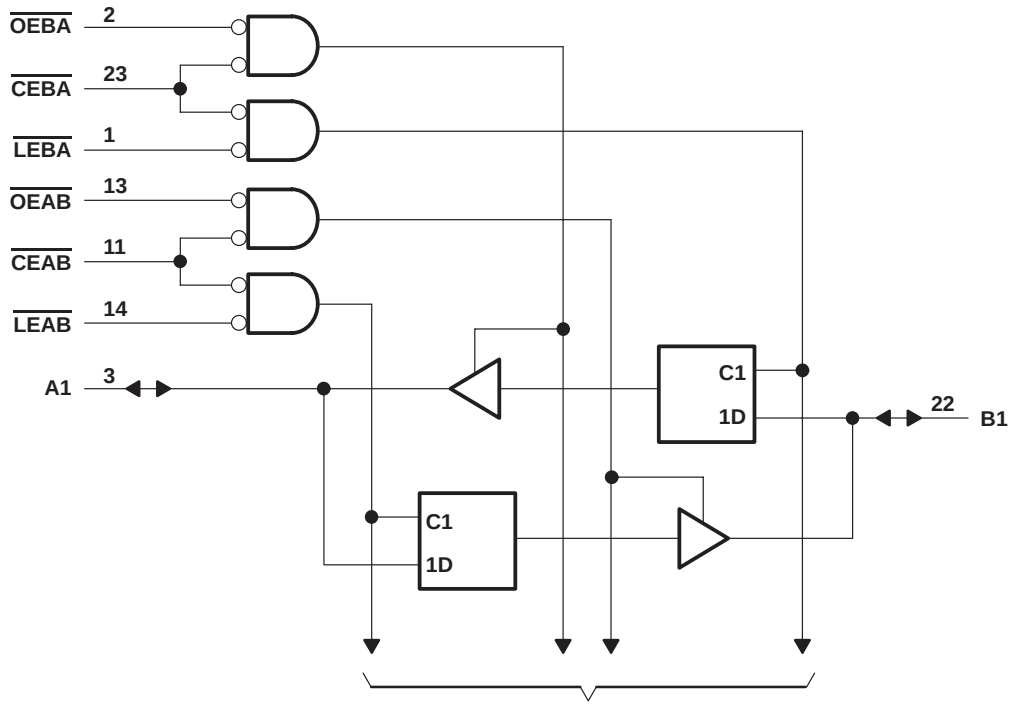
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
DC input clamp current, I_{IK} (V_I < –0.5 V) . . . . . –20 mA
DC output clamp current, I_{OK} (V_O < –0.5 V) . . . . . –50 mA
DC output sink current per output pin, I_{OL} . . . . . 70 mA
DC output source current per output pin, I_{OH} . . . . . –30 mA
Continuous current through V_{CC}, I_{CC} . . . . . 140 mA
Continuous current through GND . . . . . 528 mA
Package thermal impedance, θ_{JA} (see Note 1): EN package . . . . . 67°C/W
M package . . . . . 46°C/W
SM package . . . . . 61°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
					MIN	MAX			
	V_{IK}	I_I = –18 mA		4.75 V		–1.2		–1.2	V
	V_{OH}	I_{OH} = –15 mA		4.75 V	2.4		2.4		V
	V_{OL}	I_{OL} = 64 mA		4.75 V		0.55		0.55	V
	I_I	$V_I = V_{CC}$ or GND		5.25 V		±0.1		±1	μA
	I_{OZ}	$V_O = V_{CC}$ or GND		5.25 V		±0.5		±10	μA
	I_{OS}†	$V_I = V_{CC}$ or GND,	V_O = 0	5.25 V	–60		–60		mA
	I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.25 V		8		80	μA
	ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND		5.25 V		1.6		1.6	mA
	C_i	$V_I = V_{CC}$ or GND				10		10	pF
	C_o	$V_O = V_{CC}$ or GND				15		15	pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				MIN	MAX	UNIT
t_w	Pulse duration	$\overline{LEAB}$ or $\overline{LEBA}$ low		9		ns
t_{su}	Setup time	A or B before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	Data high	3		ns
			Data low	3		
		A or B before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	Data high	3		
			Data low	3		
t_h	Hold time	A or B after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$		2		ns
		A or B after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$		2		

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	B or A	6.4	2.5	8.5	ns
	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	9.4	2.5	12.5	
t_{en}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	9	2	12	ns
t_{dis}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	6.8	2	9	ns

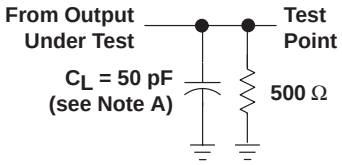
noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		0.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

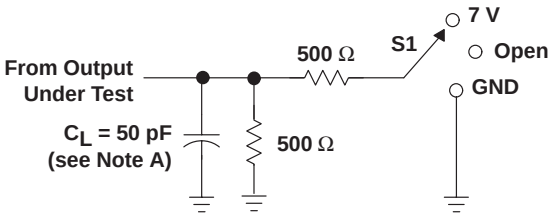
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	49	pF

PARAMETER MEASUREMENT INFORMATION

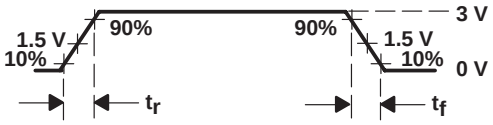


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

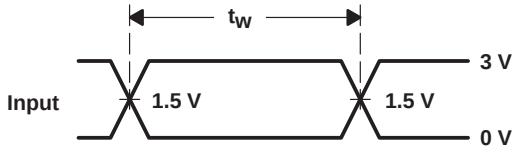


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

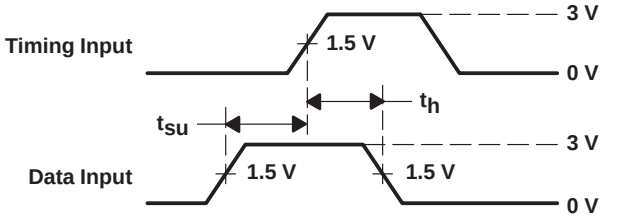
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Drain	7 V



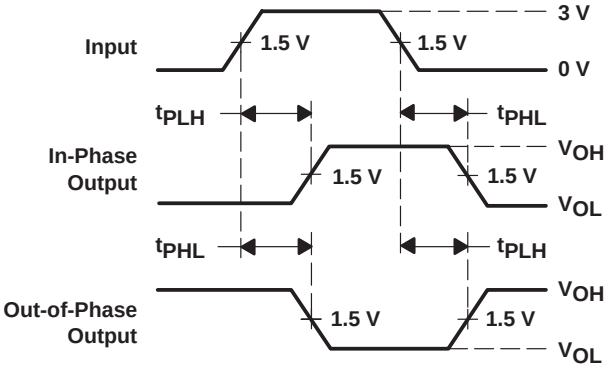
VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



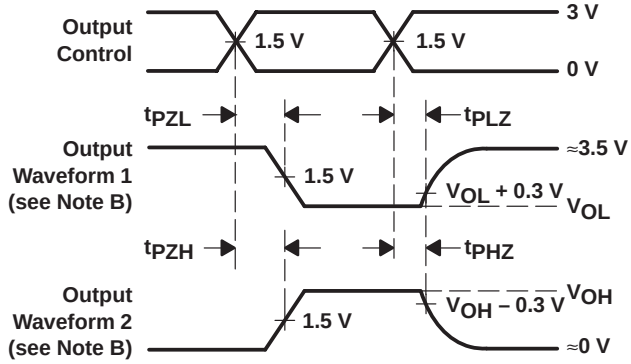
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r and t_f = 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74FCT543EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
CD74FCT543M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
CD74FCT543M96	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
CD74FCT543SM	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

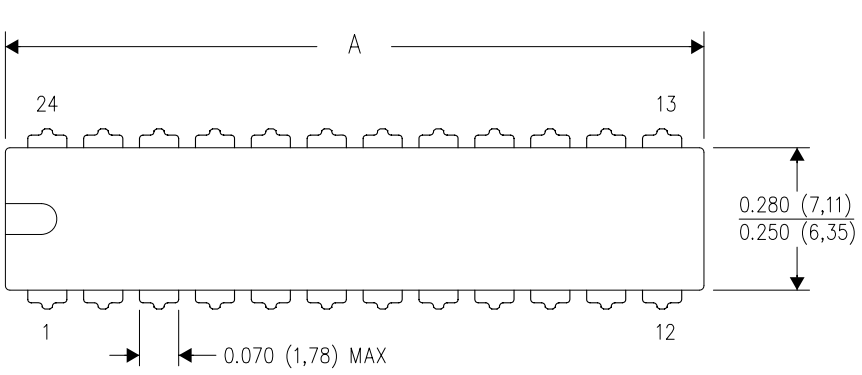
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

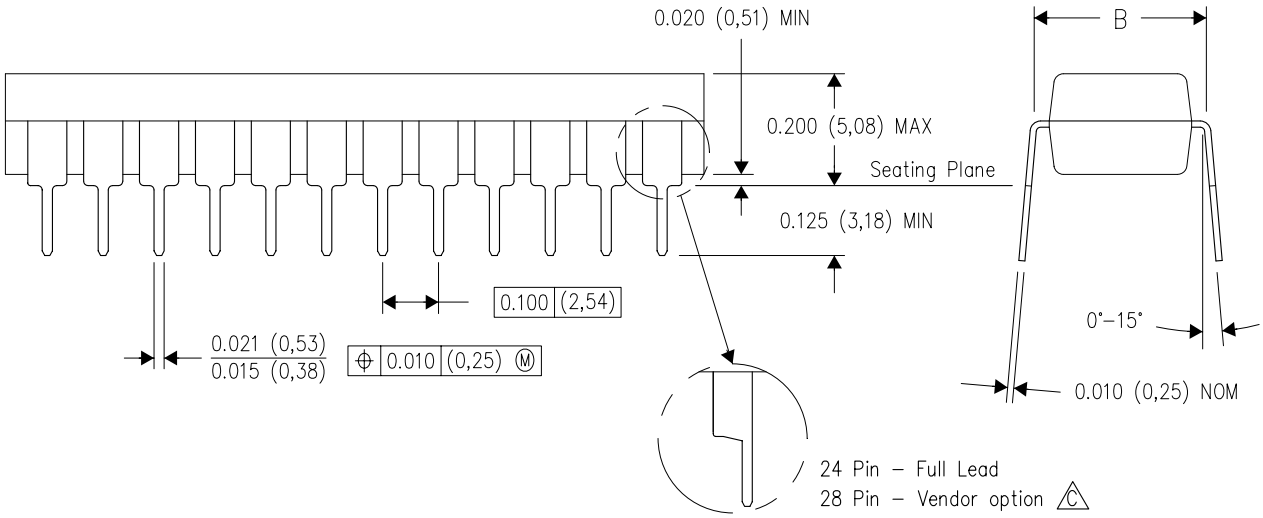
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



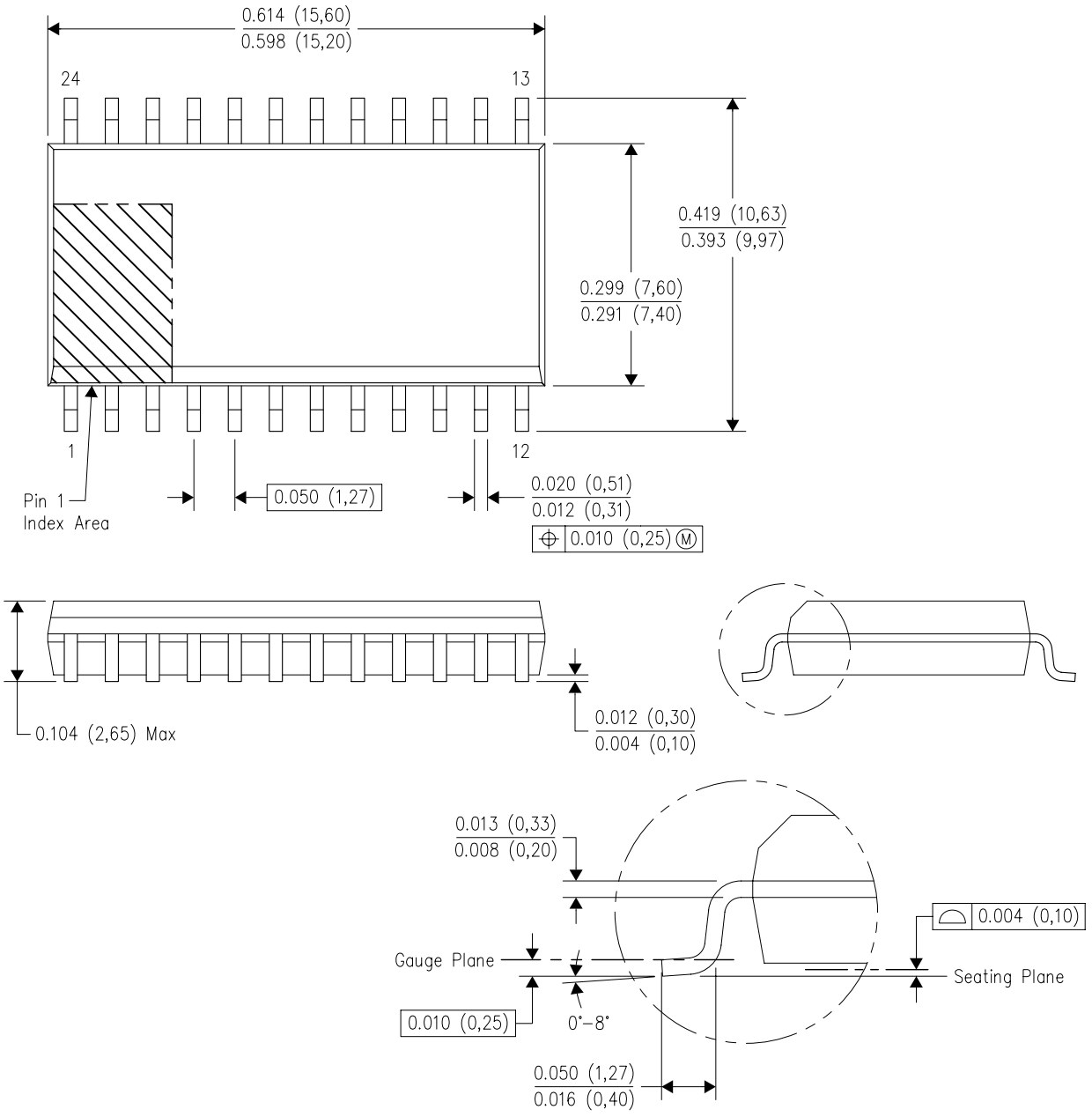
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

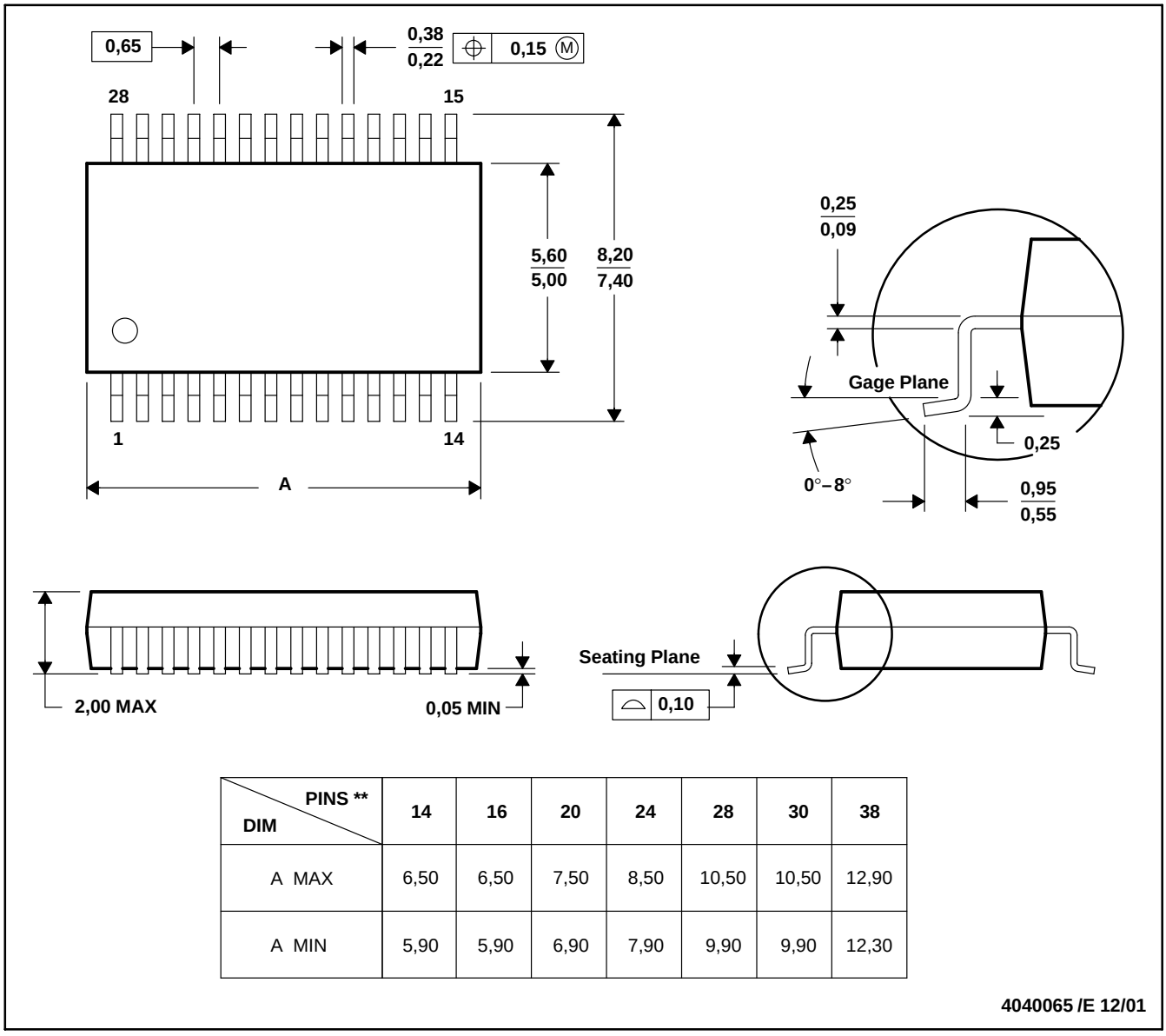


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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