



# CY54/74FCT543T

## 8-Bit Latched Registered Transceiver

### Features

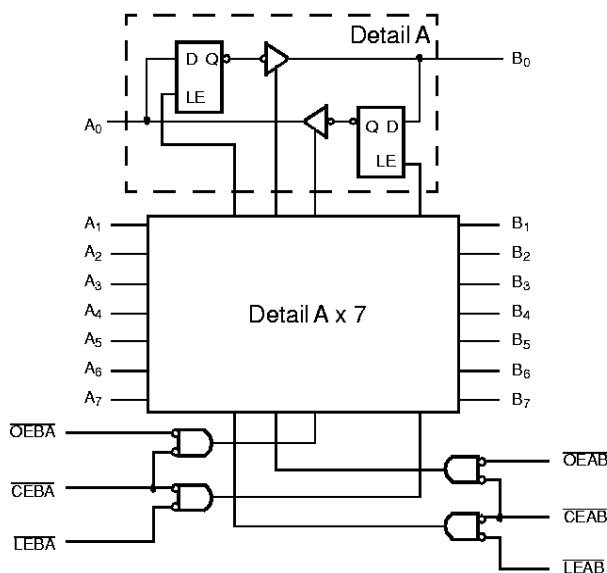
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.3 ns max. (Com'l)  
FCT-A speed at 6.5 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V
- Sink current            64 mA (Com'l), 48 mA (Mil)  
Source current        32 mA (Com'l), 12 mA (Mil)
- Separation controls for data flow in each direction
- Back to back latches for storage
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Functional Description

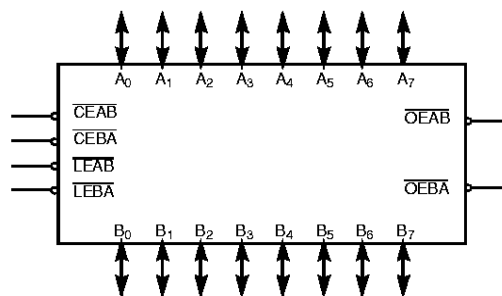
The FCT543T octal latched transceiver contains two sets of eight D-type latches with separate latch enable ( $\overline{\text{LEAB}}$ ,  $\overline{\text{LEBA}}$ ) and output enable ( $\overline{\text{OEAB}}$ ,  $\overline{\text{OEBA}}$ ) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B enable ( $\overline{\text{CEAB}}$ ) input must be LOW in order to enter data from A or to take data from B, as indicated in the truth table. With  $\overline{\text{CEAB}}$  LOW, a LOW signal on the A-to-B latch enable ( $\overline{\text{LEAB}}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{\text{LEAB}}$  signal puts the A latches in the storage mode and their output no longer change with the A inputs. With  $\overline{\text{CEAB}}$  and  $\overline{\text{OEAB}}$  both LOW, the three-stage B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$  inputs.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

### Functional Block Diagram

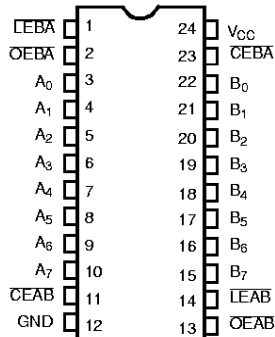


### Logic Block Diagram



### Pin Configurations

#### SOIC/QSOP Top View



**Pin Description**

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

**Function Table<sup>[1, 2]</sup>**

Inputs			Latch	Outputs
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B <sup>[3]</sup>	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs

**Notes:**

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .
- Before  $\overline{LEAB}$  LOW-to-HIGH Transition.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either  $V_{CC}$  or ground.
- $T_A$  is the "instant on" case temperature.

**Maximum Ratings<sup>[4, 5]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-65°C to +135°C
Supply Voltage to Ground Potential .....	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Voltage .....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin) .....	120 mA
Power Dissipation .....	0.5W
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	$V_{CC}$
Commercial	DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, CT	-40°C to +85°C	5V ± 5%
Military <sup>[6]</sup>	All	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. <sup>[7]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	Com'l	2.0			V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	Com'l	2.4	3.3		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =48mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage			2.0			V
V <sub>IL</sub>	Input LOW Voltage					0.8	V
V <sub>H</sub>	Hysteresis <sup>[8]</sup>	All inputs			0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA			-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>				5	μA
I <sub>IH</sub>	Input HIGH Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V				±1	μA
I <sub>IL</sub>	Input LOW Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V				±1	μA
I <sub>OZH</sub>	Off State HIGH-Level Output Current	V <sub>CC</sub> =Max., V <sub>OUT</sub> = 2.7V				10	μA
I <sub>OZL</sub>	Off State LOW-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V				-10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V		-60	-120	-225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V				±1	μA

**Capacitance<sup>[8]</sup>**

Parameter	Description	Typ. <sup>[7]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

7. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}, V_{IN}\leq 0.2V, V_{IN}\geq V_{CC}-0.2V$	0.1	0.2	mA
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs)	$V_{CC}=\text{Max.}, V_{IN}=3.4V,^{[10]}$ $f_1=0, \text{Outputs Open}$	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[11]</sup>	$V_{CC}=\text{Max.}, \text{One Input Toggling,}$ 50% Duty Cycle, Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}=\text{LOW}, \overline{CEBA}=\text{HIGH},$ $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
$I_C$	Total Power Supply Current <sup>[12]</sup>	$V_{CC}=\text{Max.}, f_0=10\text{ MHz,}$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5\text{ MHz,}$ $\overline{CEAB}$ and $\overline{OEAB}=\text{LOW}, \overline{CEBA}=\text{HIGH},$ $f_0=\overline{LEAB} = 10\text{ MHz,}$ $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC}=\text{Max.}, f_0=10\text{ MHz,}$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5\text{ MHz,}$ $\overline{CEAB}$ and $\overline{OEAB}=\text{LOW}, \overline{CEBA}=\text{HIGH},$ $f_0=\overline{LEAB} = 10\text{ MHz, } V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	1.2	3.4	mA
		$V_{CC}=\text{Max.}, f_0=10\text{ MHz,}$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=5\text{ MHz,}$ $\overline{CEAB}$ and $\overline{OEAB}=\text{LOW}, \overline{CEBA}=\text{HIGH},$ $f_0=\overline{LEAB} = 10\text{ MHz,}$ $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	2.8	5.6 <sup>[13]</sup>	mA
		$V_{CC}=\text{Max.}, f_0=10\text{ MHz,}$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=5\text{ MHz,}$ $\overline{CEAB}$ and $\overline{OEAB}=\text{LOW}, \overline{CEBA}=\text{HIGH},$ $f_0=\overline{LEAB} = 10\text{ MHz, } V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	5.1	14.6 <sup>[13]</sup>	mA

**Notes:**

10. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range<sup>[14]</sup>

Parameter	Description	FCT543T				FCT543AT		Unit	Fig. No. <sup>[15]</sup>
		Military		Commercial		Commercial			
		Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A to B or B to A	2.0	10.0	2.5	8.5	2.5	6.5	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to A, LEAB to B	2.5	14.0	2.5	12.5	2.5	8.0	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	14.0	2.0	12.0	2.0	9.0	ns	1, 7, 8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	13.0	2.0	9.0	2.0	7.5	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time HIGH or LOW, A or B to LEBA or LEAB	3.0		2.0		2.0		ns	9
t <sub>H</sub>	Hold Time HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		2.0		ns	9
t <sub>W</sub>	Pulse Width LOW <sup>[8]</sup> LEBA or LEAB	5.0		5.0		5.0		ns	5

Parameter	Description	FCT543CT		FCT543DT		Unit	Fig. No. <sup>[15]</sup>
		Commercial		Commercial			
		Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A to B or B to A	2.5	5.3	1.5	4.4	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to A, LEAB to B	2.5	7.0	1.5	5.0	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	8.0	1.5	5.4	ns	1, 7, 8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	6.5	1.5	4.3	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time, HIGH or LOW, A or B to LEBA or LEAB	2.0		1.5		ns	9
t <sub>H</sub>	Hold Time, HIGH or LOW, A or B to LEBA or LEAB	2.0		1.5		ns	9
t <sub>W</sub>	Pulse Width LOW LEBA or LEAB <sup>[8]</sup>	5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

- 14. Minimum limits are guaranteed but not tested on Propagation Delays.
- 15. See "Parameter Measurement Information" in the General Information Section.



Ordering Information

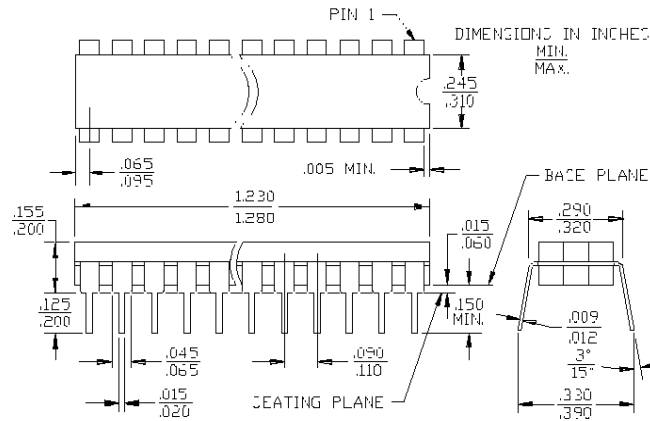
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT543DTSOC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT543DTQC	Q13	24-Lead (150-Mil) QSOP	
5.3	CY74FCT543CTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT543CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.5	CY74FCT543ATQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT543ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.5	CY74FCT543TQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT543TSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY54FCT543TDMB	D14	24-Lead (300-Mil) CerDIP	Military

Shaded areas contain preliminary information.

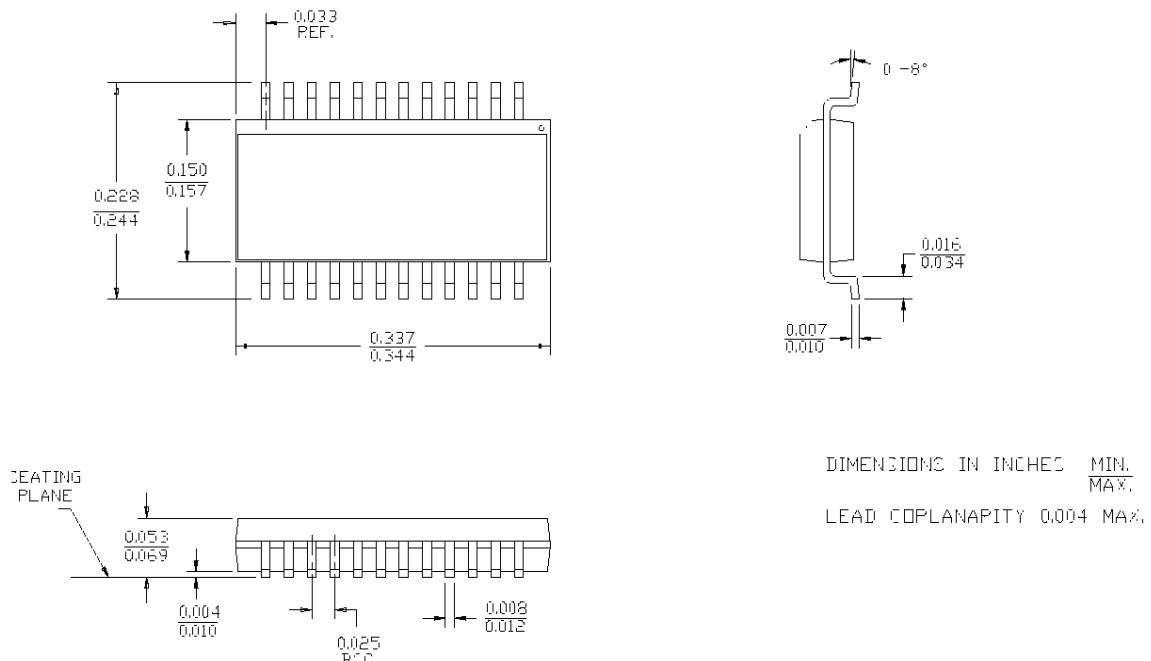
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**Package Diagrams**

**24-Lead (300-Mil) CerDIP D14**  
MIL-STD-1835 D-9 Config.A



**24-Lead Quarter Size Outline Q13**



**Package Diagrams (continued)**
**24-Lead (300-Mil) Molded SOIC S13**
