

F10161 • F10561

1-OF-8 DECODER

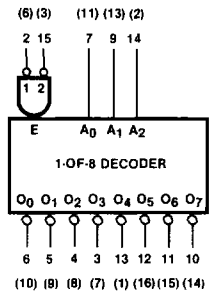
ACTIVE LOW OUTPUTS

DESCRIPTION— The F10161 and F10561 accept a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be LOW while all other outputs are HIGH. Two enable inputs force all outputs HIGH when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

PIN NAMES

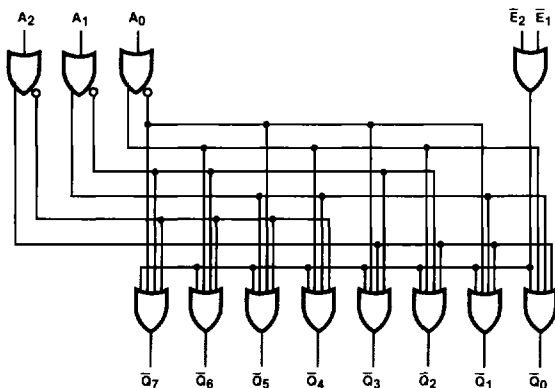
\bar{E}_N	Enable (Active LOW)
A_n	Address Inputs
\bar{O}_n	Output (Active LOW)

LOGIC SYMBOL



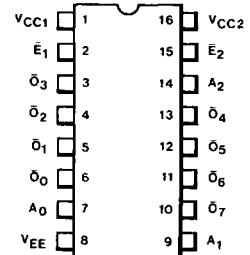
VCC1 = 1 (5)
 VCC2 = 16 (4)
 VEE = 8 (12)
 () = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)

PACKAGE OUTLINE 6B



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
\bar{E}_2	\bar{E}_1	A ₂	A ₁	A ₀	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Don't Care

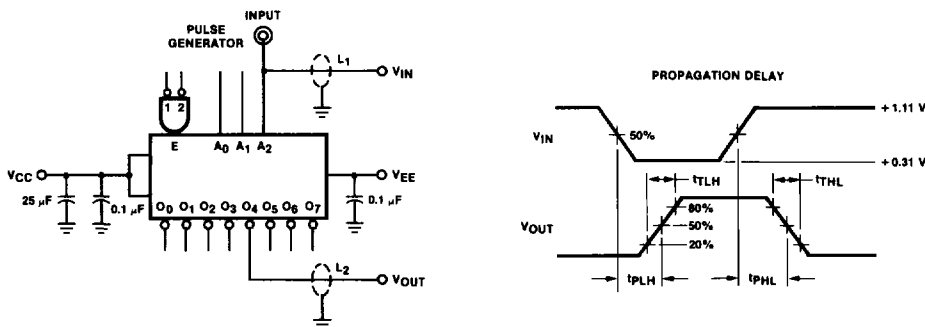
DC CHARACTERISTICS: $V_{EE} = -5.2\text{ V}$, $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T _A	CONDITIONS
		B	TYP	A			
I _{IH}	Input Current HIGH			220	μA	25 °C	V _{IN} = V _{IHA}
I _{EE}	Power Supply Current	-76	-55		mA	25 °C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2\text{ V}$, T_A = 25 °C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t _{PLH} , t _{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.5	4.5	6.0	ns	See Figure 1
t _{TLH} , t _{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L₁ and L₂ = equal length 50 Ω impedance lines
 R_T = 50 Ω termination of scope
 C_L = Jig and stray capacitance < 5.0 pF
 Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
 V_{CC1} = V_{CC2} = 2.0 V
 V_{EE} = -3.2 V

Fig. 1