

247/15

**54/74126**  
**54LS/74LS126**  
 QUAD BUS BUFFER GATE  
 (With 3-State Outputs)

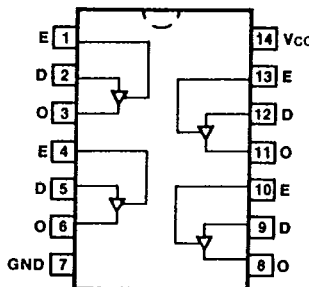
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74126PC, 74LS126PC		9A
Ceramic DIP (D)	A	74126DC, 74LS126DC	54126DM, 54LS126DM	6A
Flatpak (F)	A	74126FC, 74LS126FC	54126FM, 54LS126FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

CONNECTION DIAGRAM  
PINOUT A



TRUTH TABLE

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

DC AND AC CHARACTERISTICS: See Section 3\*

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
V <sub>OH</sub>	Output HIGH Voltage	XM	2.4		2.4	V	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	
			XC	2.4				
			XM					2.4
			XC					2.4
I <sub>OS</sub>	Output Short Circuit Current	XM	-30 -70	-30 -130		mA	V <sub>CC</sub> = Max	
XC	-28 -70	-30 -130						
I <sub>CC</sub>	Power Supply Current			24		mA	Outputs LOW, V <sub>E</sub> = 4.5 V	
		62	20		Outputs OFF, V <sub>E</sub> = 0 V			
t <sub>PLH</sub>	Propagation Delay		13	15	ns	Figs. 3-3, 3-5		
t <sub>PHL</sub>	Data to Output		18	18				
t <sub>pZH</sub>	Output Enable Time		18	20	ns	Figs. 3-3, 3-11, 3-12		
t <sub>pZL</sub>			25	30				
t <sub>PLZ</sub>	Output Disable Time		16	30	ns	Figs. 3-3, 3-11, 3-12		
t <sub>PHZ</sub>			18	30				

\*DC limits apply over operating temperature range; AC limits apply at T<sub>A</sub> = +25°C and V<sub>CC</sub> = +5.0 V.