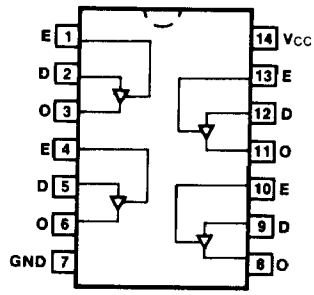
54/74126 010549
54LS/74LS126 010550

QUAD BUS BUFFER GATE
(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74126PC, 74LS126PC		9A
Ceramic DIP (D)	A	74126DC, 74LS126DC	54126DM, 54LS126DM	6A
Flatpak (F)	A	74126FC, 74LS126FC	54126FM, 54LS126FM	3I

TRUTH TABLE

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_{OH} = -2.0 mA	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XC	2.4					I_{OH} = -5.2 mA	
		XM			2.4			I_{OH} = -1.0 mA	
		XC			2.4			I_{OH} = -2.6 mA	
I_{OS}	Output Short Circuit Current	XM	-30	-70	-30	-130	mA	V_{CC} = Max	
		XC	-28	-70	-30	-130			
I_{CC}	Power Supply Current			62		24 20	mA	Outputs LOW, V_E = 4.5 V	V_{CC} = Max, V_{IN} = Gnd
								Outputs OFF, V_E = 0 V	
t_{PLH} t_{PHL}	Propagation Delay Data to Output			13 18		15 18	ns	Figs. 3-3, 3-5	
t_{PZH} t_{PZL}	Output Enable Time			18 25		20 30	ns	Figs. 3-3, 3-11, 3-12	
t_{PLZ} t_{PHZ}	Output Disable Time			16 18		30 30	ns	Figs. 3-3, 3-11, 3-12	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.