

SN54ABT841, SN74ABT841 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196A – FEBRUARY 1991 – REVISED JULY 1994

- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

The 'ABT841 10-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

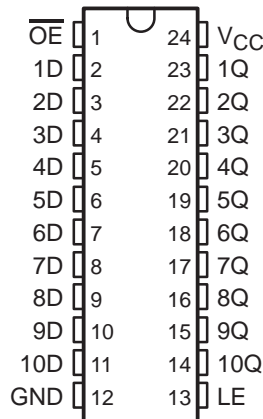
\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

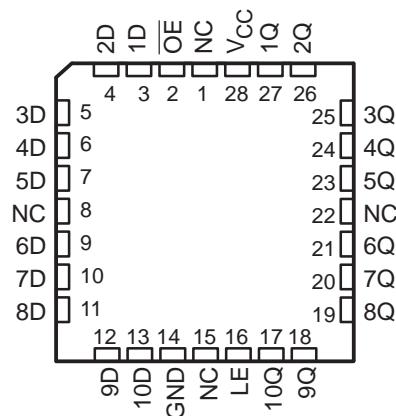
The SN74ABT841 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT841 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT841 is characterized for operation from -40°C to 85°C .

SN54ABT841 . . . JT PACKAGE
SN74ABT841 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT841 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

EPIC-II B is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

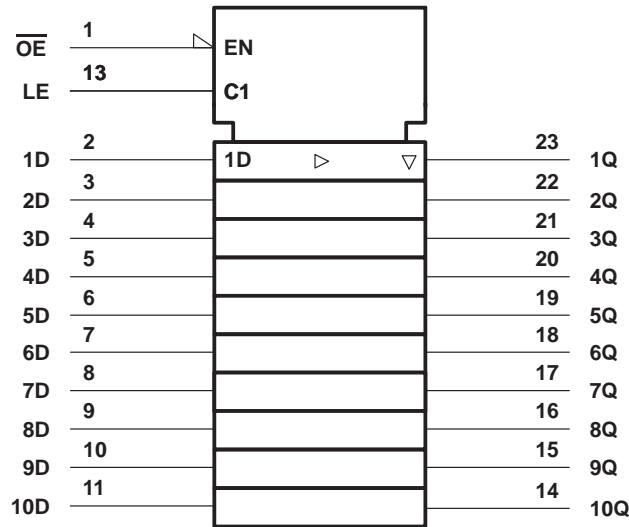
SN54ABT841, SN74ABT841 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196A – FEBRUARY 1991 – REVISED JULY 1994

FUNCTION TABLE

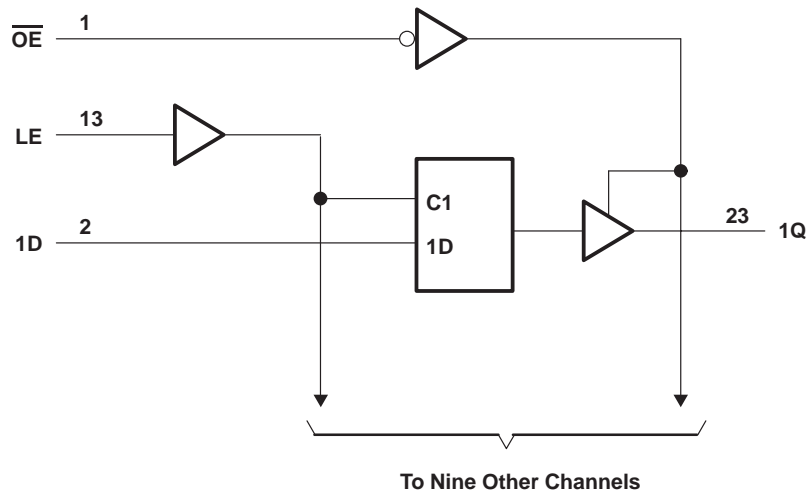
INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

SN54ABT841, SN74ABT841 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196A – FEBRUARY 1991 – REVISED JULY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT841	96 mA
SN74ABT841	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT841		SN74ABT841		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s}/\text{V}$
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

SN54ABT841, SN74ABT841 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196A – FEBRUARY 1991 – REVISED JULY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT841		SN74ABT841		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$			2.5		2.5		2.5	V	
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$			3		3		3		
	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$			2 2*		2		2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$				0.55		0.55	V	
		$I_{OL} = 64\text{ mA}$				0.55*		0.55		
I_I	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1		± 1		± 1	μA	
I_{OZPU}	$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ to }2.7\text{ V}$, $\overline{OE} = X$			± 50		± 50		± 50	μA	
I_{OZPD}	$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ to }2.7\text{ V}$, $\overline{OE} = X$			± 50		± 50		± 50	μA	
I_{OZH}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 2.7\text{ V}$, $\overline{OE} \geq 2\text{ V}$			10		10		10	μA	
I_{OZL}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 0.5\text{ V}$, $\overline{OE} \geq 2\text{ V}$			-10		-10		-10	μA	
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$			± 100				± 100	μA	
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$	Outputs high				50		50	μA	
I_{O}^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$			-50	-140	-180		-50	-180	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		1	250		250	250	μA	
		Outputs low		24	43§		43§	43§	mA	
		Outputs disabled		0.5	250		250	250	μA	
ΔI_{CC}^\parallel	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5	1.5	mA	
		Outputs disabled			250		250	250	μA	
		Control inputs			1.5		1.5	1.5	mA	
C_i	$V_I = 2.5\text{ V or }0.5\text{ V}$			4					pF	
C_o	$V_O = 2.5\text{ V or }0.5\text{ V}$			7					pF	

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This data sheet limit may vary among suppliers.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT841		SN74ABT841		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
t_w	Pulse duration, LE high or low			3.3		3.3		3.3	ns
t_{su}	Setup time, data before LE↓	High		2.5		2.5		2.5	ns
		Low		1.5		1.5		1.5	
t_h	Hold time, data after LE↓	High		1.5		1.5		1.5	ns
		Low		1		1		1	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT841, SN74ABT841
10-BIT BUS-INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS196A – FEBRUARY 1991 – REVISED JULY 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

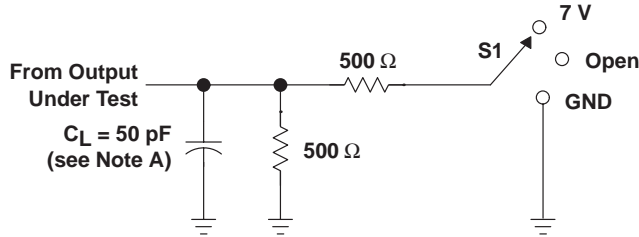
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT841		SN74ABT841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1†	4.1	5.5	1†	6.8	1†	6.7†	ns
t_{PHL}			1.5†	4	5.5	1.5†	6.3	1.5†	6.2	
t_{PLH}	LE	Q	1.6†	4.1	6.6†	1.6†	7.4	1.6†	7.2†	ns
t_{PHL}			2†	4.6	6.2	2†	6.8	2†	6.7	
t_{PZH}	\overline{OE}	Q	1	3	4.9†	1	5.8	1	5.7†	ns
t_{PZL}			2.2	4.1	5.7†	2.2	6.5	2.2	6.4†	
t_{PHZ}	\overline{OE}	Q	2†	4.7	6.2	2†	7.2	2†	7.1	ns
t_{PLZ}			1.5†	4.6	6.1	1.5†	6.6	1.5†	6.5	

† This data sheet limit may vary among suppliers.

SN54ABT841, SN74ABT841 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

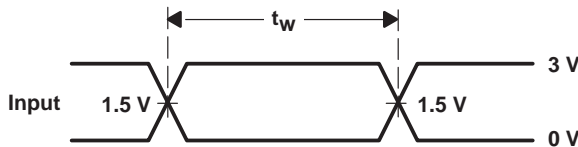
SCBS196A – FEBRUARY 1991 – REVISED JULY 1994

PARAMETER MEASUREMENT INFORMATION

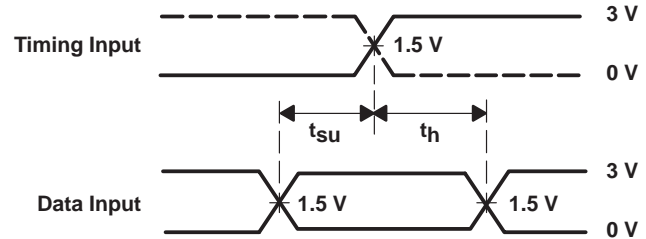


LOAD CIRCUIT FOR OUTPUTS

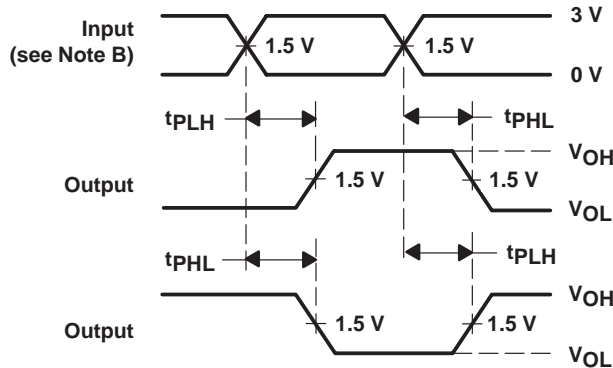
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



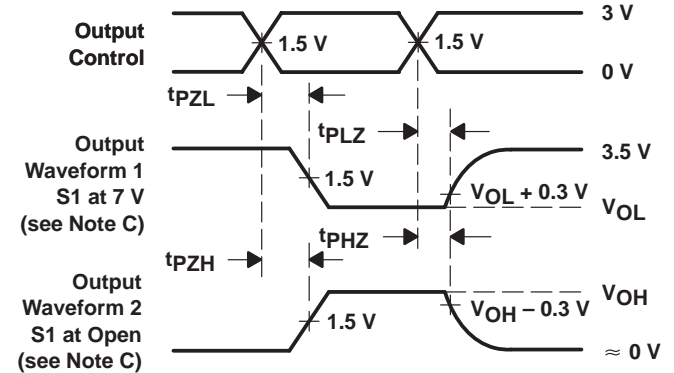
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9676901Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9676901QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9676901QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN74ABT841DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT841DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74ABT841DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74ABT841NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SNJ54ABT841FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ABT841JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SNJ54ABT841W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004


MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

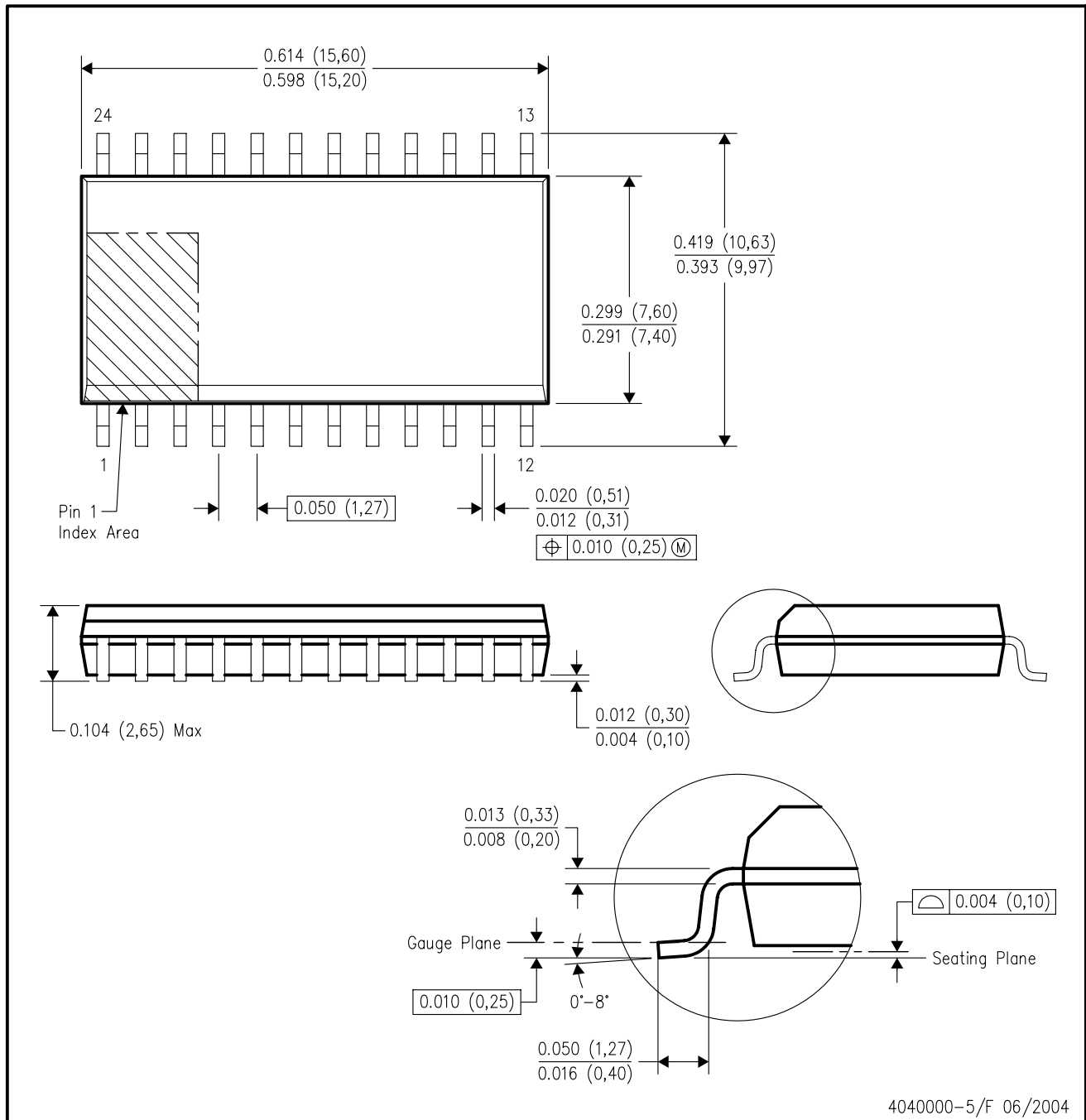


4040050/C 04/09

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE

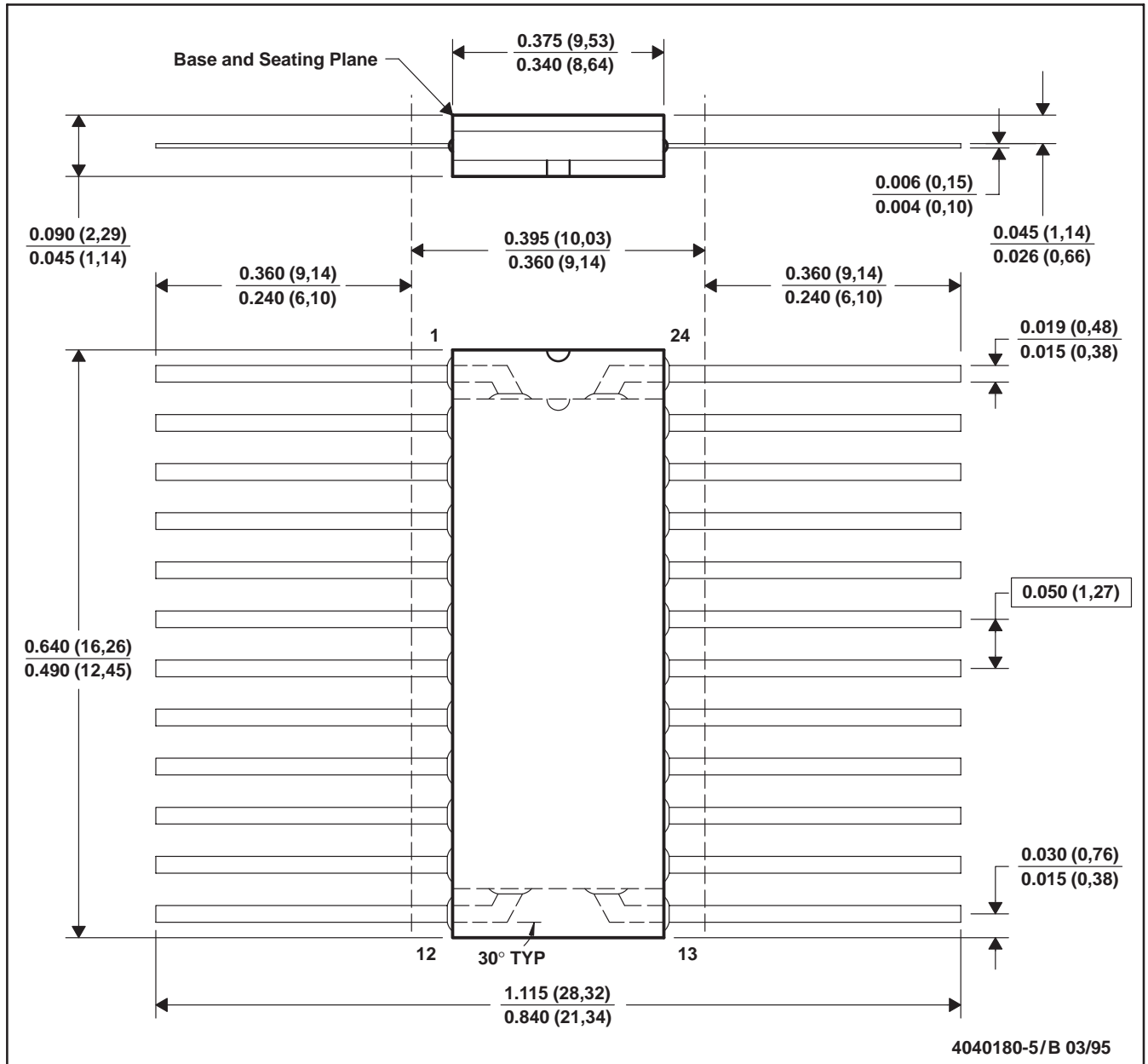


4040000-5/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - Index point is provided on cap for terminal identification only.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated