SPRS009C – JANUARY 1987 – REVISED JULY 1991

- **Performance Up to 8.77 MIPs**
- **All TMS320C1x Devices are Object Code Compatible**
- **144/256-Word On-Chip Data RAM**
- **1.5K/4K/8K-Word On-Chip Program ROM**
- **4K-Word On-Chip Program EPROM (TMS320E14/P14/E15/P15/E17/P17)**
- **One-Time Programmable (OTP) Versions Available (TMS320P14/P15/P17)**
- **EPROM Code Protection for Copyright Security**
- **4K / 64K-Word Total External Memory at Full Speed**
- **32-Bit ALU/Accumulator**
- **16 × 16-Bit Multiplier With a 32-Bit Product**
- **0 to 16-Bit Barrel Shifter**
- **Eight Input/Output Channels**
- **Dual-Channel Serial Port**
- **Simple Memory and I/O Interface**
- **5-V and 3.3-V Versions Available (TMS320LC15/LC17)**
- **Commercial and Military Versions Available**
- **Operating Free-Air Temperature . . . 0°C to 70°C**
- **Packaging: DIP, PLCC, Quad Flatpack, and CER-QUAD**
- **CMOS Technology:**

Device	Cycle Time
— TMS320C10	200-ns
— TMS320C10-14	280-ns
— TMS320C10-25	160-ns
— TMS320C14	160-ns
— TMS320E14	160-ns
— TMS320P14	160-ns
— TMS320C15	200-ns
— TMS320C15-25	160-ns
— TMS320E15	200-ns
— TMS320E15-25	160-ns
— TMS320LC15	250-ns
— TMS320P15	200-ns
— TMS320C16	114-ns
— TMS320C17	200-ns
— TMS320E17	200-ns
— TMS320LC17	278-ns
— TMS320P17	200-ns

introduction

The TMS32010 digital signal processor (DSP), introduced in 1983, was the first DSP in the TMS320 family. From it has evolved this TMS320C1x generation of 16-bit DSPs. All ′C1x DSPs are object code compatible with the TMS32010 DSP. The ′C1x DSPs combine the flexibility of a high-speed controller with the numerical capability of an array processor, thereby offering an inexpensive alternative to multichip bit-slice processors. The highly paralleled architecture and efficient instruction set provide speed and flexibility to produce a CMOS microprocessor generation capable of executing up to 8.77 MIPS (million instructions per second) (′C16). These ′C1x devices utilize a modified Harvard architecture to optimize speed and flexibility, implementing functions in hardware that other processors implement through microcode or software.

The ′C1x generation's powerful instruction set, inherent flexibility, high-speed number-handling capabilities, reduced power consumption, and innovative architecture have made these cost-effective DSPs the ideal solution for many telecommunications, computer, commercial, industrial, and military applications.

This data sheet provides detailed design documentation for the ′C1x DSPs. It facilitates the selection of devices best suited for various user applications by providing specifications and special features for each ′C1x DSP.

This data sheet is arranged as follows: introduction, quick reference table of device parameters and packages, summary overview of each device, architecture overview, and the ′C1x device instruction set summary. These are followed by data sheets for each ′C1x device providing available package styles, terminal function tables, block diagrams, and electrical and timing parameters. An index is provided to facilitate data sheet usage.

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Table 1 provides an overview of ′C1x processors with comparisons of memory, I/O, cycle timing, military support, and package types. For specific availability, contact the nearest TI Field Sales Office.

Table 1. TMS320C1x Device Overview

DEVICE	MEMORY				I/O		CYCLE	PACKAGE (1)		
	RAM	ROM	EPROM	PROG.	SERIAL	PARALLEL	(ns)	DIP	PLCC	CER-QUAD
TMS320C10 (2)	144	1.5K	—	4K	—	8 × 16	200	40	44	—
TMS320C10-14	144	1.5K	—	4K	—	8 × 16	280	40	44	—
TMS320C10-25	144	1.5K	—	4K	—	8 × 16	160	40	44	—
TMS320C14 (3)	256	4K	—	4K	1	7 × 16 (4)	160	—	68	—
TMS320E14 (3)	256	—	4K	4K	1	7 × 16 (4)	160	—	—	68 CER
TMS320P14†	256	—	4K	4K	1	7 × 16 (4)	160	—	68	—
TMS320C15 (3)	256	4K	—	4K	—	8 × 16	200	40	44	—
TMS320C15-25	256	4K	—	4K	—	8 × 16	160	40	44	—
TMS320E15 (3)	256	—	4K	4K	—	8 × 16	200	40	—	44 CER
TMS320E15-25	256	—	4K	4K	—	8 × 16	160	40	—	44 CER
TMS320LC15	256	4K	—	4K	—	8 × 16	250	40	44	—
TMS320P15†	256	—	4K	4K	—	8 × 16	200	40	44	—
TMS320C16	256	8K	—	64K	—	8 × 16	114	—	—	64 QFP
TMS320C17	256	4K	—	—	2	6 × 16 (5)	200	40	44	—
TMS320E17 (5)	256	—	4K	—	2	6 × 16 (5)	200	40	—	44 CER
TMS320LC17 (5)	256	4K	—	—	2	6 × 16 (5)	278	40	44	—
TMS320P17 (5)†	256	—	4K	—	2	6 × 16 (5)	200	40	44	

† One-time programmable (OTP) device is in a windowless plastic package and cannot be erased.

NOTES: 1. DIP = dual in-line package. PLCC = plastic-leaded chip carrier. CER = ceramic-leaded chip carrier. QFP = plastic quad flat pack.
2. Military version available.
3. Military versions planned; contact nearest TI Field Sales Office for availability.
4. On-chip 16-bit I/O, four capture inputs, and six compare outputs are available.
5. On-chip 16-bit coprocessor interface is optional by pin selection.

description

TMS320C10

The ′C10 provides the core CPU used in all other ′C1x devices. Its microprocessor operates at 5 MIPS. It provides a parallel I/O of 8 × 16 bits. Three versions with cycle times of 160, 200, and 280 ns are available as illustrated in Table 1. The ′C10 versions are offered in plastic 40-pin DIP or a 44-lead PLCC packages.

TMS320C14/E14/P14

The ′C14/E14/P14 devices, using the ′C10 core CPU, offer expanded on-chip RAM, and ROM or EPROM (′E14/P14), 16 pins of bit selectable parallel I/O, an I/O mapped asynchronous serial port, four 16-bit timers, and external/internal interrupts. The ′C14 devices can provide for microcomputer/microprocessor operating modes. Three versions with cycle times of 160-ns are available as illustrated in Table 1. These devices are offered in 68-pin plastic PLCC or ceramic CER-QUAD packages.

TMS320C15/E15/P15

The ′C15/E15/P15 devices are a version of the ′C10, offering expanded on-chip RAM, and ROM or EPROM (′E15/P15). The ′P15 is a one-time programmable (OTP), windowless EPROM version. These devices can operate in the microcomputer or microprocessor modes. Five versions are available with cycle times of 160 to 200 ns (see Table 1). These devices are offered in 40-pin DIP, 44-pin PLCC, or 44-pin ceramic packages.

TMS320LC15

The ′LC15 is a low-power version of the ′C15, utilizing a V_{DD} of only 3.3-V. This feature results in a 2.3: 1 power requirement reduction over the typical 5-V ′C1x device. It operates at a cycle time of 250 ns. The device is offered in 40-pin DIP or 44-lead PLCC packages.

TMS320C16

The ′C16 offers on-chip RAM of 256-words, an expanded program memory of 64K-words, and a fast instruction cycle time of 114 ns (8.77 MIPS). It is offered in a 64-pin quad flat-pack package.

TMS320C17/E17/P17

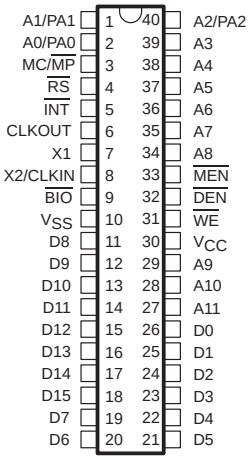
The ′C17/E17/P17 versions consist of five major functional units: the ′C15 microcomputer, a system control register, a full-duplex dual channel serial port, μ-law/A-law companding hardware, and a coprocessor port. The dual-channel serial port is capable of full-duplex serial communication and offers direct interface to two combo-codecs. The hardware companding logic can operate in either μ-law or A-law format with either sign-magnitude or twos complement numbers in either serial or parallel modes. The coprocessor port allows the ′C17/E17/P17 to act as a slave microcomputer or as a master to a peripheral microcomputer.

The ′P17 utilizes a one-time programmable (OTP) windowless EPROM version of the ′E17.

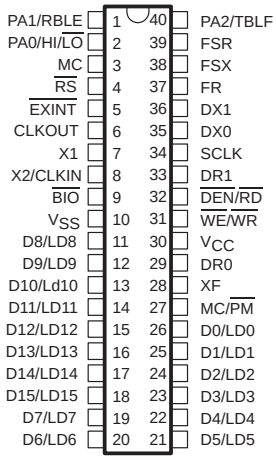
TMS320LC17

The ′LC17 is a low-power version of the ′C17, utilizing a V_{DD} of only 3.3-V. This feature results in a 2.3: 1 power requirement reduction over the typical 5-V ′C1x device. It operates at a cycle time of 278 ns.

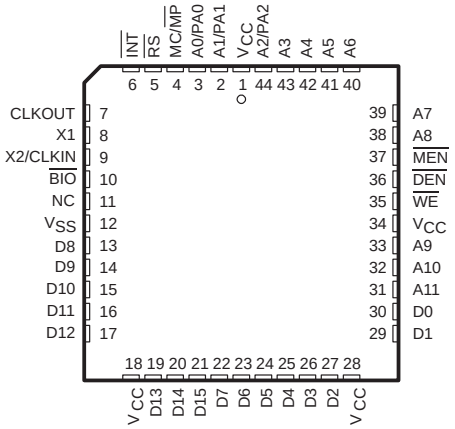
TMS320C10/C15/LC15/P15
N/JD Packages
(Top View)



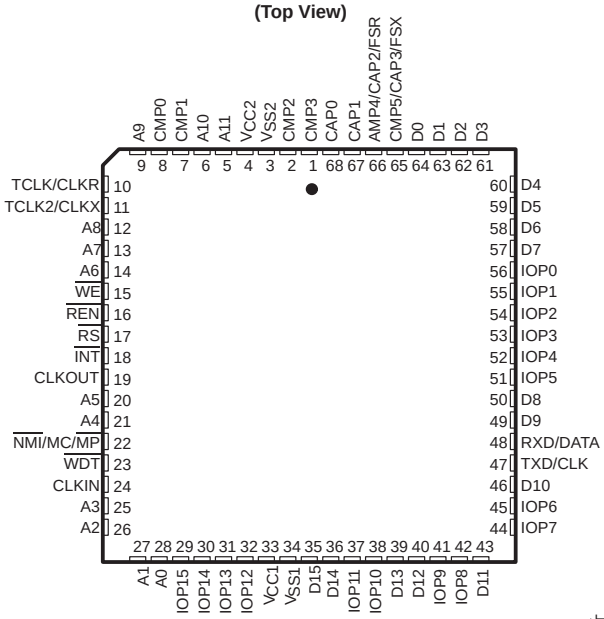
TMS320C17/E17/LC17/P17
N/JD Packages
(Top View)



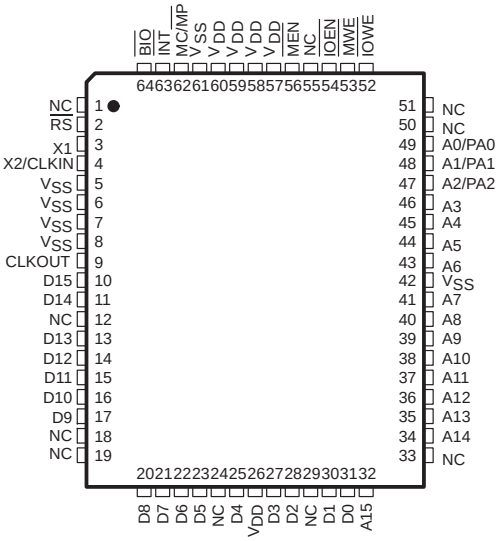
TMS320C10/C15/E15/LC15/P15
FN/FZ Packages
(Top View)



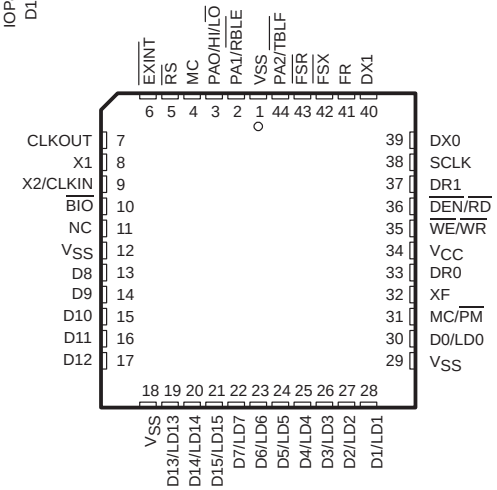
TMS320C14/E14/P14
FN/FZ Packages
(Top View)



TMS320C16
PG Package
(Top View)



TMS320C17/E17
FN/FZ Packages
(Top View)



architecture

The ′C1x DSPs use a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and one-cycle execution. The ′C1x DSPs modification allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM.

32-bit accumulator

All ′C1x devices contain a 32-bit ALU and accumulator for support of double-precision, twos-complement arithmetic. The ALU is a general-purpose arithmetic unit that operates on 16-bit words taken from the data RAM or derived from immediate instructions. In addition to the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller. The accumulator stores the output from the ALU and is often an input to the ALU. It operates with a 32-bit word length. The accumulator is divided into a high-order word (bits 31 through 16) and a low-order word (bits 15 through 0). Instructions are provided for storing the high- and low-order accumulator words in memory.

shifters

Two shifters are available for manipulating data. The ALU barrel shifter performs a left-shift of 0 to 16 places on data memory words loaded into the ALU. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for twos-complement arithmetic. The accumulator parallel shifter performs a left-shift of 0, 1 or 4 places on the entire accumulator and places the resulting high-order accumulator bits into data RAM. Both shifters are useful for scaling and bit extraction.

16 × 16-bit parallel multiplier

The multiplier performs a 16 × 16-bit twos-complement multiplication with a 32-bit result in a single instruction cycle. The multiplier consists of three units: the T Register, P Register, and a multiplier array. The 16-bit T Register stores the multiplicand, and the P Register stores the 32-bit product. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the device to perform fundamental operations such as convolution, correlation, and filtering.

data and program memory

Since the ′C1x devices use a Harvard type architecture, data and program memory reside in two separate spaces. These DSP devices have 144-or 256-words of on-chip data RAM and 1.5K- to 8K-words of on-chip program ROM. On-chip program EPROM of 4K-words is provided in the ′E14/E15/E17 devices. An on-chip one-time programmable 4K-word EPROM is provided in the ′P14/P15/P17 devices. The EPROM cell utilizes standard PROM programmers and is programmed identically to a 64K CMOS EPROM (TMS27C64). (Reference Table 1.)

program memory expansion

All ′C1x devices except the ′C17/E17/LC17/P17 devices are capable of executing from off-chip external memory at full speed for those applications requiring external program memory space. This allows for external RAM-based systems to provide multiple functionality. The ′C17/E17/LC17/P17 devices provide no external memory expansion. (Reference Table 1.)

microcomputer/microprocessor operating modes

All devices except the ′x17 offer two modes of operation defined by the state of the MC/$\overline{\text{MP}}$ pin: the microcomputer mode (MC/$\overline{\text{MP}}$ = 1) or the microprocessor mode (MC/$\overline{\text{MP}}$ = 0). In the microcomputer mode, on-chip ROM is mapped into the program memory space. In the microprocessor mode, all words of progam memory are external.

interrupts and subroutines

All devices except the ′C16 contain a four-level stack for saving the contents of the program counter during interrupts and subroutine calls. Because of the larger 64K program space, the ′C16's hardware stack has been increased to eight levels. Instructions are available for saving the device's complete context. PUSH and POP instructions permit a level of nesting restricted only by the amount of available RAM. The interrupts used in these devices are maskable.

input/output

The 16-bit parallel data bus can be utilized to perform I/O functions in two cycles. The I/O ports are addressed by the three LSBs on the address lines. In addition, a polling input for bit test and jump operations ($\overline{BIO}$) and an interrupt pin ($\overline{INT}$) have been incorporated for multitasking. The bit selectable I/O of the ′C14 is suitable for microcontroller applications.

serial port (TMS320C17/E17)

Two of the I/O ports on the ′C17/E17 are dedicated to the serial port and companding hardware. I/O port 0 is dedicated to control register 0, which controls the serial port, interrupts, and companding hardware. I/O port 1 accesses control register 1, as well as both serial port channels, and companding hardware. The six remaining I/O ports are available for external parallel interfaces.

serial port (TMS320C14/E14)

The ′C14/E14 devices include one I/O-mapped serial port that operates asynchronously. I/O-mapped control registers are used to configure port parameters such as inter-processor communication protocols and baud rate.

companding hardware (TMS320C17/E17)

On-chip hardware enables the ′C17/E17 to compand (COMpress/exPAND) data in either μ-law or A-law format. The companding logic operation is configured via the system control register. Data may be companded in either serial mode for operation on serial port data (converting between linear and logarithmic PCM) or a parallel mode for computation inside the device. The ′C17/E17 allows the hardware companding logic to operate with either sign-magnitude or twos-complement numbers.

coprocessor port (TMS320C17/E17)

The coprocessor port on the ′C17/E17 provides a direct connection to most microcomputers and microprocessors. The port is accessed through I/O port 5 using IN and OUT instructions. The coprocessor interface allows the device to act as a peripheral (slave) microcomputer to a microprocessor, or as a master to a peripheral microcomputer. In the microcomputer mode, the 16 data lines are used for the 6 parallel 16-bit I/O ports. In the coprocessor mode, the 16-bit parallel port is reconfigured to operate as a 16-bit latched bus interface. For peripheral transfer, an 8-bit or 16-bit length of the coprocessor port can be selected.

instruction set

A comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general-purpose operations, such as high-speed control. All of the ′C1x devices are object-code compatible and use the same 60 instructions. The instruction set consists primarily of single-cycle single-word instructions, permitting execution rates of more than six million instructions per second. Only infrequently used branch and I/O instructions are multicycle. Instructions that shift data as part of an arithmetic operation execute in a single cycle and are useful for scaling data in parallel with other operations.

NOTE

The $\overline{\text{BIO}}$ pin on other ′C1x devices is not available for use in the ′C14/E14/P14. An attempt to execute the BIOZ (Branch on $\overline{\text{BIO}}$ low) instruction will result in a two cycle NOP action.

Three main addressing modes are available with the instruction set: direct, indirect, and immediate addressing.

direct addressing

In direct addressing, seven bits of the instruction word concatenated with the 1-bit data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words, and the second page contains up to 128 words.

indirect addressing

Indirect addressing forms the data memory address from the least-significant eight bits of one of the two auxiliary registers, AR0-AR1. The Auxiliary Register Pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented and the ARP changed in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

immediate addressing

Immediate instructions derive data from part of the instruction word rather than from the data RAM. Some useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

instruction set summary

Table 2 lists the symbols and abbreviations used in Table 3, the instruction set summary. Table 3 contains a short description and the opcode for each ′C1x instruction. The summary is arranged according to function and alphabetized within each functional group.

Table 2. Instruction Symbols

SYMBOL	MEANING
ACC	Accumulator
D	Data memory address field
M	Addressing mode bit
K	Immediate operand field
PA	3-bit port address field
R	1-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

Table 3. TMS320C1x Instruction Set Summary

ACCUMULATOR INSTRUCTIONS																				
MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER																
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0
ADD	Add to accumulator with shift	1	1	0	0	0	0	← S →				M	← D →						
ADDH	Add to high-order accumulator bits	1	1	0	1	1	0	0	0	0	0	M	← D →						
ADDS	Add to accumulator with no sign extension	1	1	0	1	1	0	0	0	0	1	M	← D →						
AND	AND with accumulator	1	1	0	1	1	1	1	0	0	1	M	← D →						
LAC	Load accumulator with shift	1	1	0	0	1	0	← S →				M	← D →						
LACK	Load accumulator immediate	1	1	0	1	1	1	1	1	1	0	← K →							
OR	OR with accumulator	1	1	0	1	1	1	1	0	1	0	M	← D →						
SACH	Store high-order accumulator bits with shift	1	1	0	1	0	1	1	← X →			M	← D →						
SACL	Store low-order accumulator bits	1	1	0	1	0	1	0	0	0	0	M	← D →						
SUB	Subtract from accumulator with shift	1	1	0	0	0	1	← S →				M	← D →						
SUBC	Conditional subtract (for divide)	1	1	0	1	1	0	0	1	0	0	M	← D →						
SUBH	Subtract from high-order accumulator bits	1	1	0	1	1	0	0	0	1	0	M	← D →						
SUBS	Subtract from accumulator with no sign extension	1	1	0	1	1	0	0	0	1	1	M	← D →						
XOR	Exclusive OR with accumulator	1	1	0	1	1	1	1	0	0	0	M	← D →						
ZAC	Zero accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1
ZALH	Zero accumulator and load high-order bits	1	1	0	1	1	0	0	1	0	1	M	← D →						
ZALS	Zero accumulator and load low-order bits with no sign extension	1	1	0	1	1	0	0	1	1	0	M	← D →						

AUXILIARY REGISTER AND DATA PAGE POINTER INSTRUCTIONS																				
MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER																
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAR	Load auxiliary register	1	1	0	0	1	1	1	0	0	R	M	← D →						
LARK	Load auxiliary register immediate	1	1	0	1	1	1	0	0	0	R	← K →							
LARP	Load auxiliary register pointer immediate	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	K
LDP	Load data memory page pointer	1	1	0	1	1	0	1	1	1	1	M	← D →						
LDPK	Load data memory page pointer immediate	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	K
MAR	Modify auxiliary register and pointer	1	1	0	1	1	0	1	0	0	0	M	← D →						
SAR	Store auxiliary register	1	1	0	0	1	1	0	0	0	R	M	← D →						

Table 3. TMS320C1x Instruction Set Summary (continued)

BRANCH INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	2	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BANZ	Branch on auxiliary register not zero	2	2	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BGEZ	Branch if accumulator ≥ 0	2	2	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BGZ	Branch if accumulator > 0	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BIOZ	Branch on $\overline{BIO}$ = 0 †	2	2	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BLEZ	Branch if accumulator ≤ 0	2	2	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BLZ	Branch if accumulator < 0	2	2	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BNZ	Branch if accumulator ≠ 0	2	2	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BV	Branch on overflow	2	2	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
BZ	Branch if accumulator = 0	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
CALA	Call subroutine from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
CALL	Call subroutine immediately	2	2	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →											
RET	Return from subroutine or interrupt routine	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1

T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APAC	Add P register to accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
LT	Load T Register	1	1	0	1	1	0	1	0	1	0	M	←			D	→		
LTA	LTA combines LT and APAC into one instruction	1	1	0	1	1	0	1	1	0	0	M	←			D	→		
LTD	LTD combines LT, APAC, and DMOV into one instruction	1	1	0	1	1	0	1	0	1	1	M	←			D	→		
MPY	Multiply with T register, store product in P register	1	1	0	1	1	0	1	1	0	1	M	←			D	→		
MPYK	Multiply T register with immediate operand; store product in P register	1	1	1	0	0	←							K				→	
PAC	Load accumulator from P register	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0
SPAC	Subtract P register from accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0

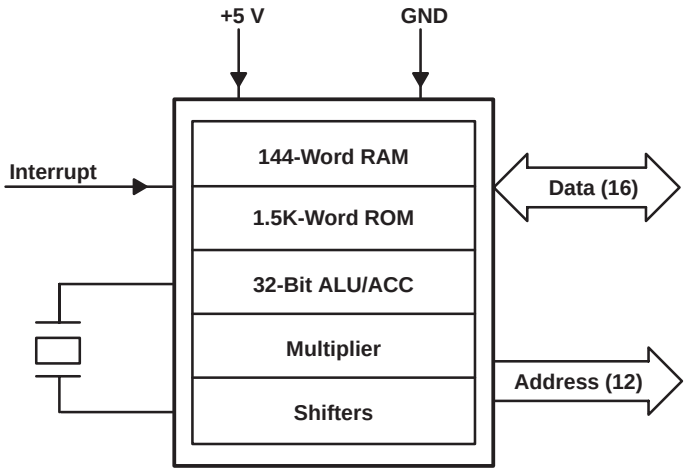
† This instruction is a NOP on the ′320C14/E14/P14.

Table 3. TMS320C1x Instruction Set Summary (concluded)

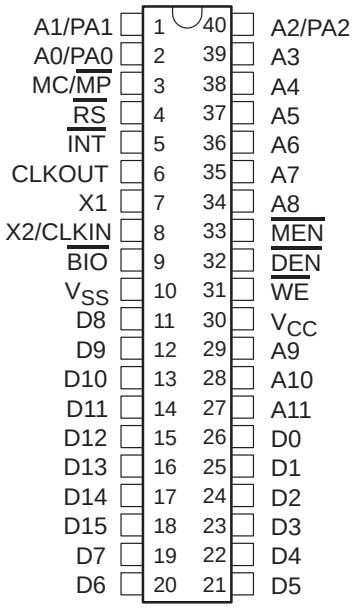
CONTROL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER														
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DINT	Disable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0
LST	Load status register	1	1	0	1	1	1	1	0	1	1	M	←			D			→
NOP	No operation	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
POP	POP stack to accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	1
PUSH	PUSH stack from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	0
ROVM	Reset overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0
SOVM	Set overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1
SST	Store status register	1	1	0	1	1	1	1	1	0	0	M	←			D			→
I/O AND DATA MEMORY OPERATIONS																			
MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMOV	Copy contents of data memory location into next higher location	1	1	0	1	1	0	1	0	0	1	M	←			D			→
IN	Input data from port	2	1	0	1	0	0	0	←	PA	→		M	←		D			→
OUT	Output data to port	2	1	0	1	0	0	1	←	PA	→		M	←		D			→
TBLR	Table read from program memory to data RAM	3	1	0	1	1	0	0	1	1	1	M	←			D			→
TBLW	Table write from data RAM to program memory	3	1	0	1	1	1	1	1	0	1	M	←			D			→

Key Features: TMS320C10

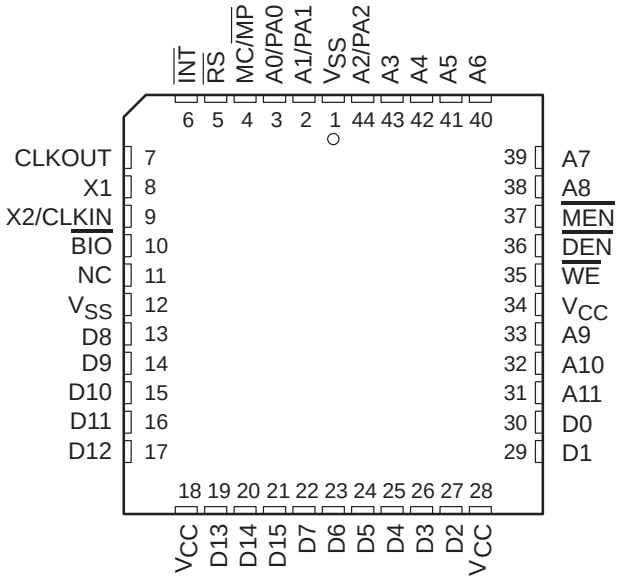
- **Instruction Cycle Timing**
  - **160-ns (TMS320C10-25)**
  - **200-ns (TMS32010)**
  - **280-ns (TMS320C10-14)**
- **144 Words of On-Chip Data RAM**
- **1.5K Words On-Chip Program ROM**
- **External Memory Expansion up to 4K Words at Full Speed**
- **16 × 16-Bit Multiplier With 32-Bit Product**
- **0 to 16-Bit Barrel Shifter**
- **On-Chip Clock Oscillator**
- **Device Packaging:**
  - **40-Pin DIP**
  - **44-Lead PLCC**
- **Single 5-V Supply**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**



TMS320C10
N/JD Package
(Top View)



TMS320C10
FN/FZ Package
(Top View)

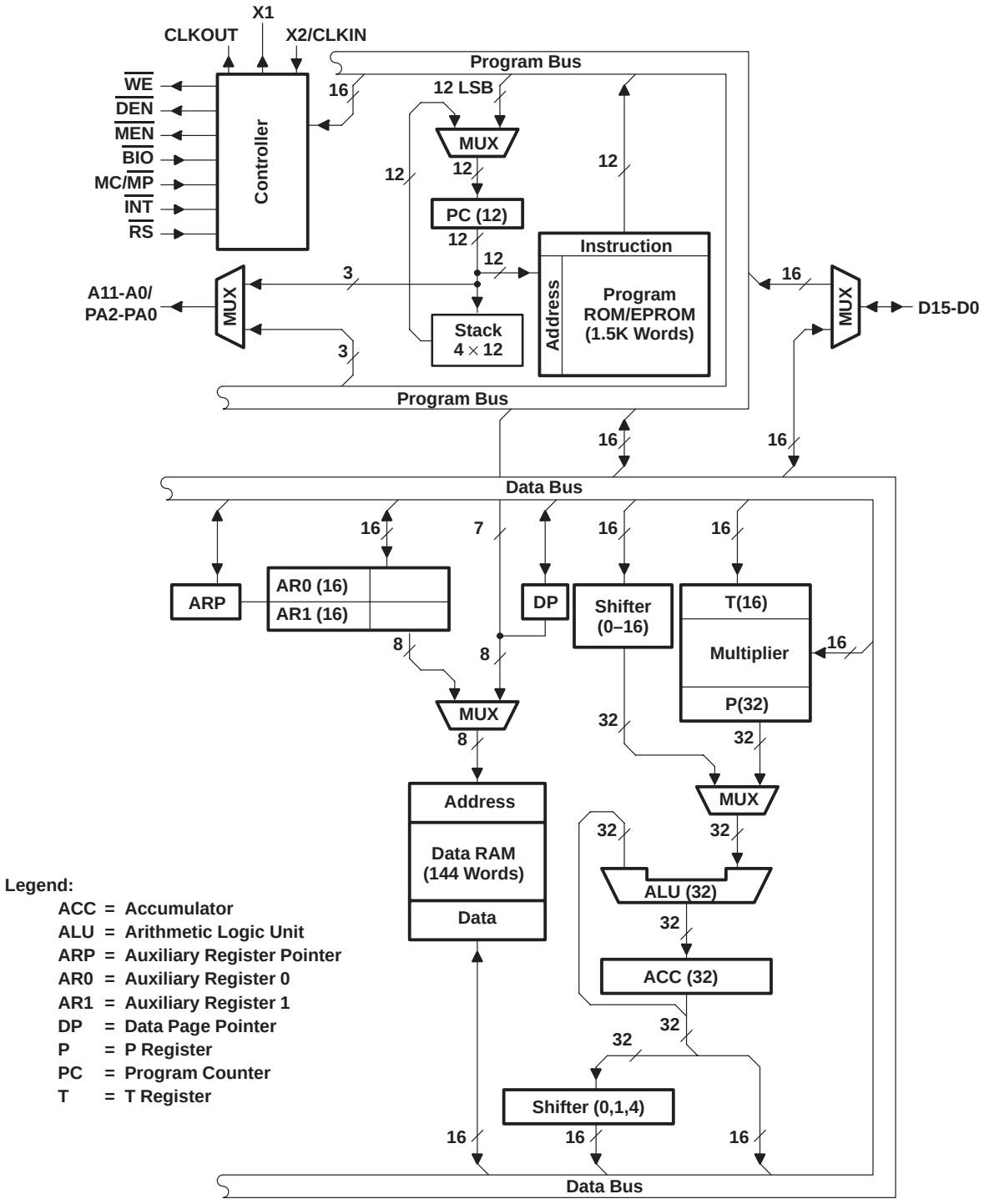


TERMINAL FUNCTIONS

NAME	I/O†	DEFINITION
A11-A0/PA2-PA0	O	External address bus. I/O port address multiplexed over PA2-PA0.
$\overline{\text{BIO}}$	I	External polling input
CLKOUT	O	System clock output, 1/4 crystal/CLKIN frequency
D15-D0	I/O	16-bit parallel data bus
$\overline{\text{DEN}}$	O	Data enable for device input data on D15-D0
$\overline{\text{INT}}$	I	External interrupt input
MC/$\overline{\text{MP}}$	I	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
$\overline{\text{MEN}}$	O	Memory enable indicates that D15-D0 will accept external memory instruction.
NC	O	No connection
$\overline{\text{RS}}$	I	Reset for initializing the device
V_{CC}	I	+ 5 V supply
V_{SS}	I	Ground
$\overline{\text{WE}}$	O	Write enable for device output data on D15-D0
X1	O	Crystal output for internal oscillator
X2/CLKIN	I	Crystal input internal oscillator or external system clock input

† Input/Output/High-impedance state.

functional block diagram



Legend:

ACC = Accumulator
ALU = Arithmetic Logic Unit
ARP = Auxiliary Register Pointer
AR0 = Auxiliary Register 0
AR1 = Auxiliary Register 1
DP = Data Page Pointer
P = P Register
PC = Program Counter
T = T Register

electrical specifications

This section contains the electrical specifications for all speed versions of the ′C10 Digital Signal Processors, including test parameter measurement information.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range V_{CC} (see Note 6) . . . . . –0.3 V to 7 V
Input voltage range . . . . . –0.3 V to 7 V
Output voltage range . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . 0.5 mW
Operating free-air temperature: L suffix . . . . . 0°C to 70°C
A suffix . . . . . – 40°C to 85°C
Storage temperature . . . . . –55 °C to 150 °C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN	3			V
		All remaining inputs	2			V
V_{IL}	Low-level input voltage	MC/$\overline{\text{MP}}$			0.6	V
		All remaining inputs			0.8	V
I_{OH}	High-level output current, all outputs				–300	µA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature	L suffix	0		70	°C
		A suffix	– 40		85	°C

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 µA (see Note 7)		V_{CC} – 0.4‡			
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{OZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	µA
				V_O = 0.4 V			–20	
I_I	Input current		V_{CC} = V_{SS} to V_{CC}	All inputs except CLKIN			±20	µA
				CLKIN			±50	
C_i	Input capacitance	Data bus	f = 1 MHz, all other pins 0 V			25‡		pF
		All others				15‡		
C_o	Output capacitance	Data bus				25‡		pF
		All others				10‡		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Values derived from characterization data and not tested.
NOTE 7: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

INTERNAL CLOCK OPTION

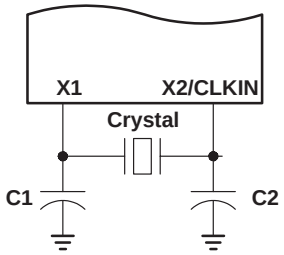


Figure 1. Internal Clock Option

PARAMETER MEASUREMENT INFORMATION

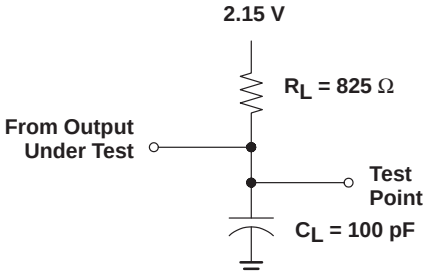


Figure 2. Test Load Circuit

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS (SEE FIGURE 2)	MIN	TYP†	MAX	UNIT
I_{CC}‡ Supply current	TMS320C10	f = 20.5 MHz, V_{CC} = 5.5 V, T_A = – 40°C to 85°C		33	55	mA
	TMS320C10-25	f = 25.6 MHz, V_{CC} = 5.5 V T_A = – 0°C to 70°C		40	65	

† All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡ I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependence on temperature, frequency, and loading.

CLOCK CHARACTERISTICS AND TIMING

The ′C10/C10-25 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and should be specified at a load capacitance of 20 pF.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_X	TMS320C10	T_A = – 40°C to 85°C	6.7		20.5	MHz
	TMS320C10-25	T_A = 0°C to 70°C	6.7		25.6	
C1, C2		T_A = – 40°C to 85°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C10			TMS320C10-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(C)}$	CLKOUT cycle time§	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	195.12	200		156.25	160		ns
$t_{r(C)}$	CLKOUT rise time			10¶			10¶		ns
$t_{f(C)}$	CLKOUT fall time			8¶			8¶		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92¶			72¶		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90¶			70¶		ns
$t_{d(MCC)}$	Delay time, CLKIN↑ to CLKOUT↓		25¶		60¶	25		50¶	ns

§ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
¶ Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	39.06	40	150¶	ns
$t_{r(MC)}$	Rise time, master clock input		5¶	10¶		5¶	10¶	ns
$t_{f(MC)}$	Fall time, master clock input		5¶	10¶		5¶	10¶	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.4t_{c(MC)}$¶		$0.6t_{c(MC)}$¶	$0.45t_{c(MC)}$¶		$0.55t_{c(MC)}$¶	ns
$t_{w(MCL)}$	Pulse duration, master clock low		20¶			15¶		ns
$t_{w(MCH)}$	Pulse duration, master clock high		20¶			15¶		ns

¶ Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C10			TMS320C10-25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{d1}	Delay time, CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	10†		50	10†		40	ns
t_{d2}	Delay time, CLKOUT↓ to $\overline{MEN}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 15$	$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 12$	ns
t_{d3}	Delay time, CLKOUT↓ to $\overline{MEN}$↑		–10†		15	–10†		12	ns
t_{d4}	Delay time, CLKOUT↓ to $\overline{DEN}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 15$	$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 12$	ns
t_{d5}	Delay time, CLKOUT↓ to $\overline{DEN}$↑		–10†		15	–10†		12	ns
t_{d6}	Delay time, CLKOUT↓ to $\overline{WE}$↓		$1/2t_{c(C)} - 5$†		$1/2t_{c(C)} + 15$	$1/2t_{c(C)} - 5$†		$1/2t_{c(C)} + 12$	ns
t_{d7}	Delay time, CLKOUT↓ to $\overline{WE}$↑		–10†		15	–10†		12	ns
t_{d8}	Delay time, CLKOUT↓ to data bus OUT valid				$1/4t_{c(C)} + 65$			$1/4t_{c(C)} + 52$†	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$1/4t_{c(C)} - 5$†			$1/4t_{c(C)} - 5$†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven				$1/4t_{c(C)} + 40$†			$1/4t_{c(C)} + 40$†	ns
t_v	Data bus OUT valid after CLKOUT↓		$1/4t_{c(C)} - 10$			$1/4t_{c(C)} - 10$			ns
$t_{h(A\text{-}WMD)}$	Address hold time after $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 8)		–10†			–10†			ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{MEN}$↓ or $\overline{DEN}$↓		$1/4t_{c(C)} - 45$			$1/4t_{c(C)} - 35$			ns

† Values derived from characterization data and not tested.
NOTE 8: For interfacing I/O devices, see Figure 3.

timing requirements over recommended operating conditions

		TEST CONDITION	TMS320C10			TMS320C10-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(D)}$	Setup time, data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	50			40			ns
$t_{h(D)}$	Hold time, data bus held valid after CLKOUT↓ (see Note 9)		0			0			ns

NOTE 9: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

SUGGESTED I/O DECODE CIRCUIT

The circuit shown in Figure 3 is a design example for interfacing I/O devices to the ′C10/C10-25. This circuit decodes the address for output operations using the OUT instruction. The same circuit can be used to decode input and output operations if the inverter (’ALS04) is replaced with a NAND gate and both $\overline{DEN}$ and $\overline{WE}$ are connected. Inputs and outputs can be decoded at the same port provided the output of the decoder (’AS137) is gated with the appropriate signal ($\overline{DEN}$ or $\overline{WE}$) to select read or write (using an ’ALS32). Access times can be increased when the circuit shown in Figure 3 is repeated to support IN instructions with $\overline{DEN}$ connected rather than $\overline{WE}$.

The table write (TBLW) function requires a different circuit. A detailed discussion of an example circuit for this function is described in the application report, “Interfacing External Memory to the TMS32010”, published in the book, *Digital Signal Processing Applications with the TMS320 Family* (SPRA012A).

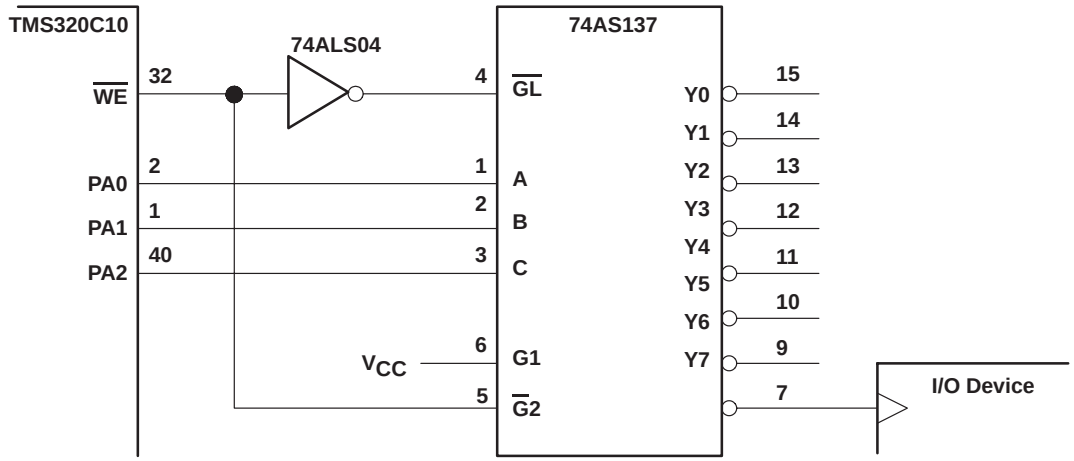


Figure 3. I/O Decode Circuit

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time, $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}$	R_L 825 Ω, C_L = 100 pF, (see Figure 2)			$1/2t_{c(C)}+50$†	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$1/4t_{c(C)}+50$†	ns

† Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

PARAMETER		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 10)	50			40			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			$5t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(INT)}$	Fall time, $\overline{INT}$			15			15	ns
$t_{w(INT)}$	Pulse duration, $\overline{INT}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time, $\overline{INT}\downarrow$ before CLKOUT$\downarrow$	50			40			ns

IO ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(IO)}$	Fall time, $\overline{BIO}$			15			15	ns
$t_{w(IO)}$	Pulse duration, $\overline{BIO}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time, $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	50			40			ns

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡	Supply current	f = 14.4, MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		28	65	mA

† All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡ I_{CC} characteristics are inversely proportional to temperature; i.e., I_{CC} decreases approximately linearly with temperature.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C10-14 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_X	T_A = 0°C to 70°C	6.7		14.4	MHz
C1, C2	T_A = 0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time§	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	277.78			ns
$t_{r(C)}$	CLKOUT rise time			10		ns
$t_{f(C)}$	CLKOUT fall time			8		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			131		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			129		ns
$t_{d(MCC)}$	Delay time, CLKIN↑ to CLKOUT↓		25¶		60¶	ns

§ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
¶ Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	69.5		150	ns
$t_{r(MC)}$	Rise time, master clock input		5¶	10¶	ns
$t_{f(MC)}$	Fall time, master clock input		5¶	10¶	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.4t_{c(MC)}$¶		$0.6t_{c(MC)}$¶	ns
$t_{w(MCL)}$	Pulse duration, master clock low, $t_{c(MC)}$ = 50 ns		20¶		ns
$t_{w(MCH)}$	Pulse duration, master clock high, $t_{c(MC)}$ = 50 ns		20¶		ns

¶ Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{d1}	Delay time, CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	10†		50	ns
t_{d2}	Delay time, CLKOUT↓ to $\overline{\text{MEN}}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 15$	ns
t_{d3}	Delay time, CLKOUT↓ to $\overline{\text{MEN}}$↑		–10†		15	ns
t_{d4}	Delay time, CLKOUT↓ to $\overline{\text{DEN}}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 15$	ns
t_{d5}	Delay time, CLKOUT↓ to $\overline{\text{DEN}}$↑		–10†		15	ns
t_{d6}	Delay time, CLKOUT↓ to $\overline{\text{WE}}$↓		$1/2t_{c(C)} - 5$†		$1/2t_{c(C)} + 15$	ns
t_{d7}	Delay time, CLKOUT↓ to $\overline{\text{WE}}$↑		–10†		15	ns
t_{d8}	Delay time, CLKOUT↓ to data bus OUT valid				$1/4t_{c(C)} + 65$	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$1/4t_{c(C)} - 5$†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven				$1/4t_{c(C)} + 40$†	ns
t_v	Data bus OUT valid after CLKOUT↓		$1/4t_{c(C)} - 10$			ns
$t_{h(A\text{-}WMD)}$	Address hold time after $\overline{\text{WE}}$↑, $\overline{\text{MEN}}$↑, or $\overline{\text{DEN}}$↑ (see Note 8)		–10†			ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{\text{MEN}}$↓ or $\overline{\text{DEN}}$↓		$1/4t_{c(C)} - 45$			ns

† Values derived from characterization data and not tested.
NOTE 8: For interfacing I/O devices, see Figure 3.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)}$	Setup time, data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	50			ns
$t_{h(D)}$	Hold time, data bus held valid after CLKOUT↓ (see Note 9)		0			ns

NOTE 9: Data may be removed from the data bus upon $\overline{\text{MEN}}$↑ or $\overline{\text{DEN}}$↑ preceding CLKOUT↓.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time, $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF (see Figure 2)			$1/2t_{c(C)} + 50^\dagger$	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$1/4t_{c(C)} + 50^\dagger$	ns

† Values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 10)	50			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(INT)}$	Fall time, $\overline{INT}$			15	ns
$t_{w(INT)}$	Pulse duration, $\overline{INT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time, $\overline{INT}\downarrow$ before CLKOUT$\downarrow$	50			ns

IO ($\overline{BIO}$) TIMING

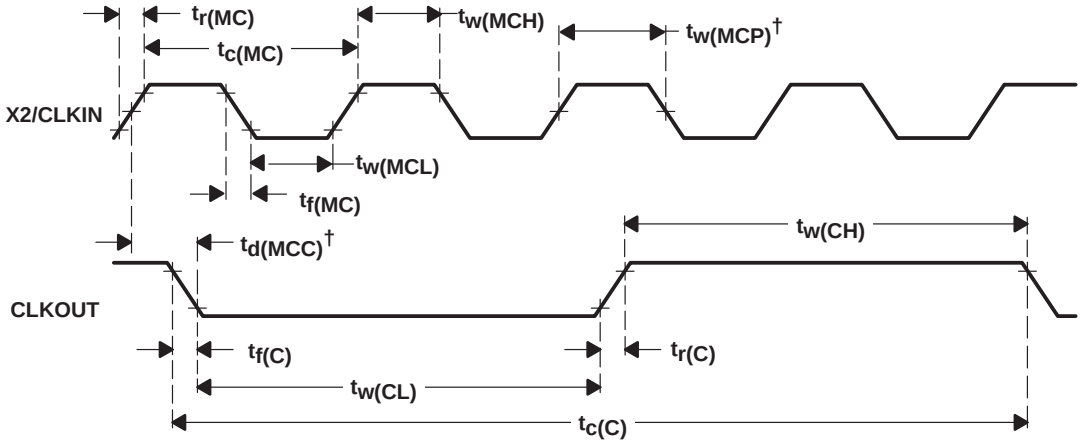
timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(IO)}$	Fall time, $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration, $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time, $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	50			ns

TIMING DIAGRAMS

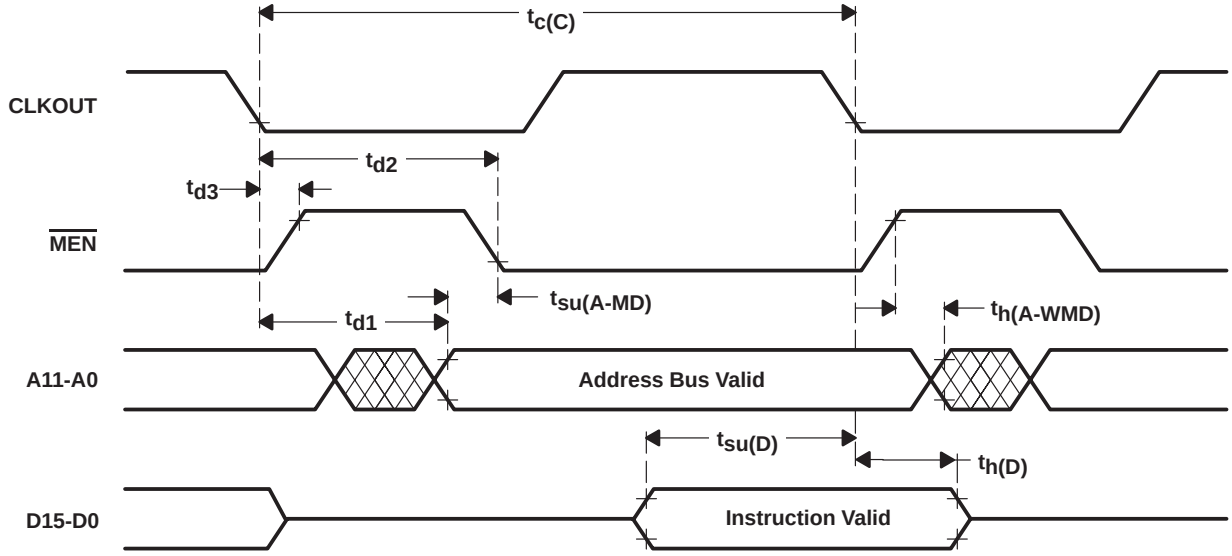
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2 volts, unless otherwise noted.

clock timing

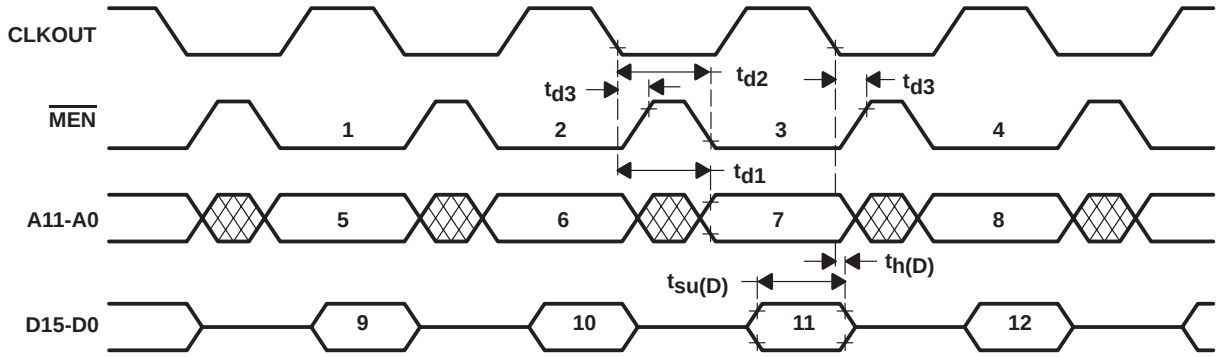


† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

memory read timing



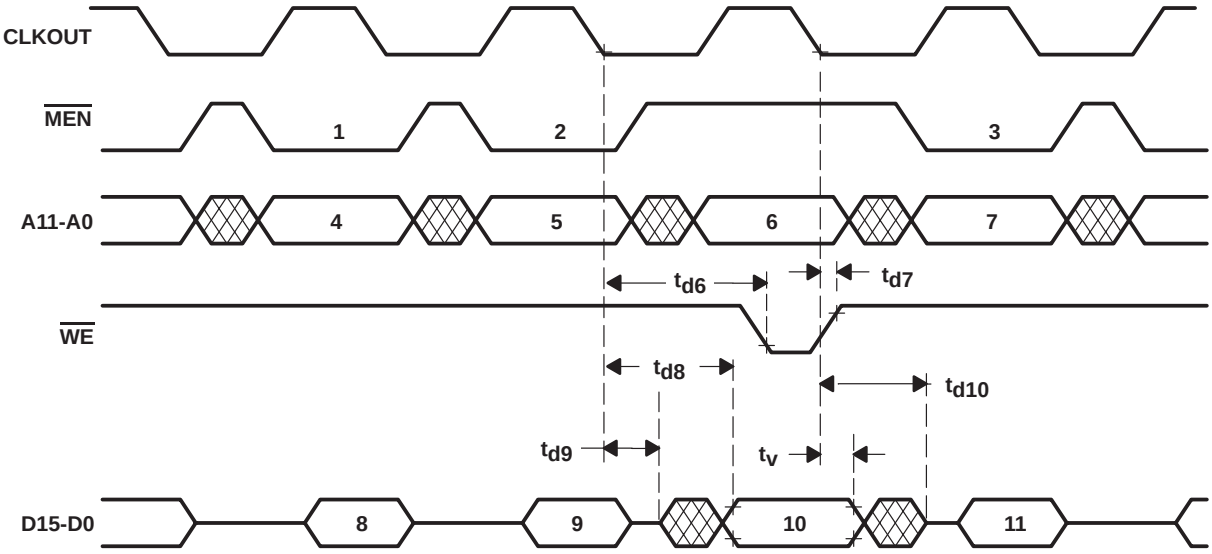
TBLR instruction timing



Legend:

1. TBLR Instruction Prefetch
2. Dummy Prefetch
3. Data Fetch
4. Next Instruction Prefetch
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Address Bus Valid
9. Instruction Valid
10. Instruction Valid
11. Data Input Valid
12. Instruction Valid

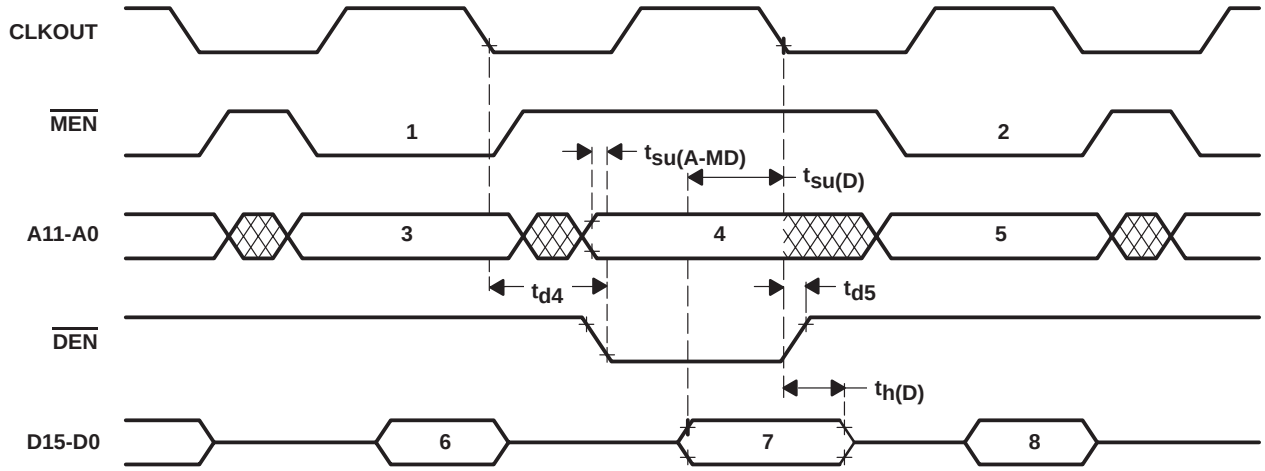
TBLW instruction timing



Legend:

1. TBLW Instruction Prefetch
2. Dummy Prefetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Instruction Valid
9. Instruction Valid
10. Data Output Valid
11. Instruction Valid

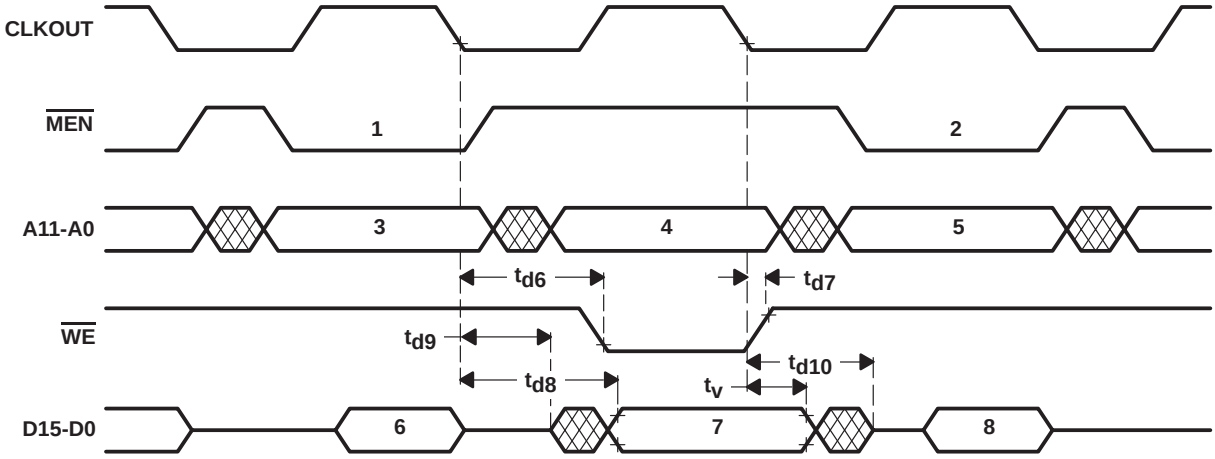
IN instruction timing



Legend:

1. IN Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Input Valid
8. Instruction Valid

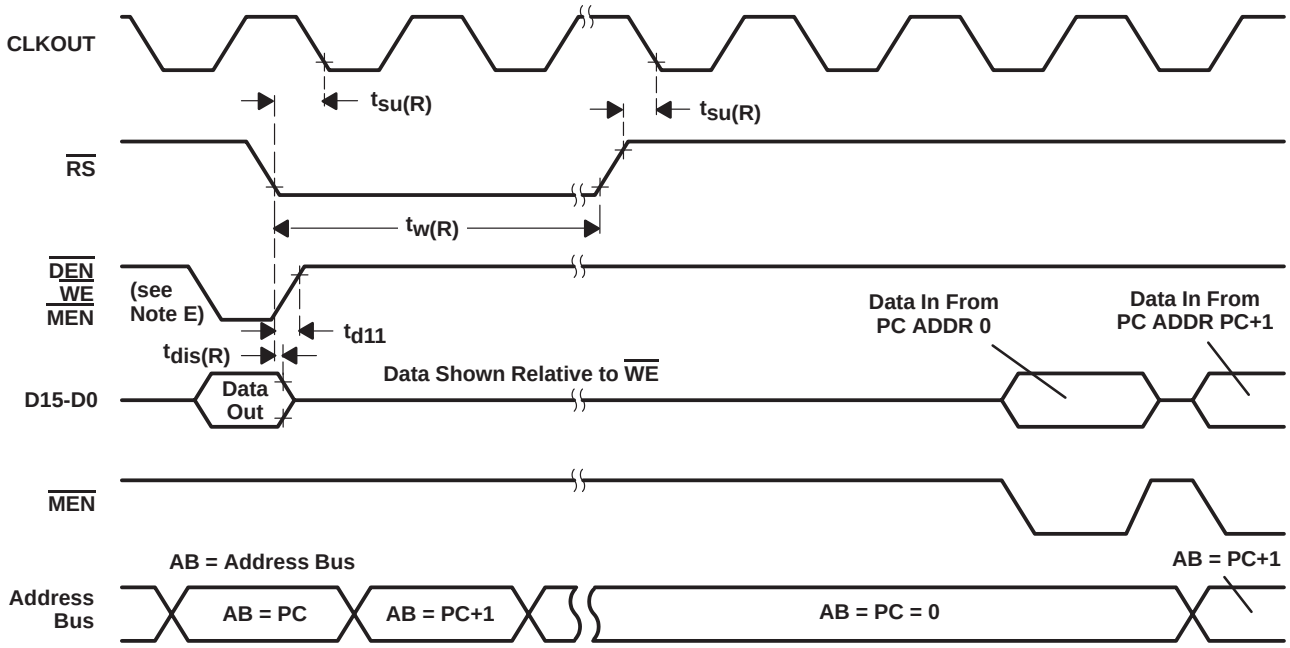
OUT instruction timing



Legend:

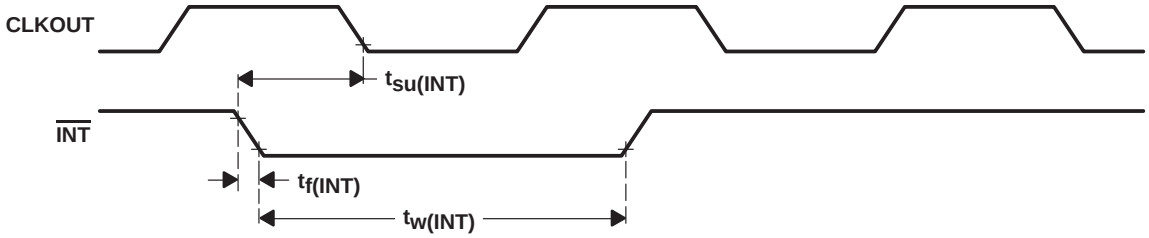
1. OUT Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Output Valid
8. Instruction Valid

reset timing

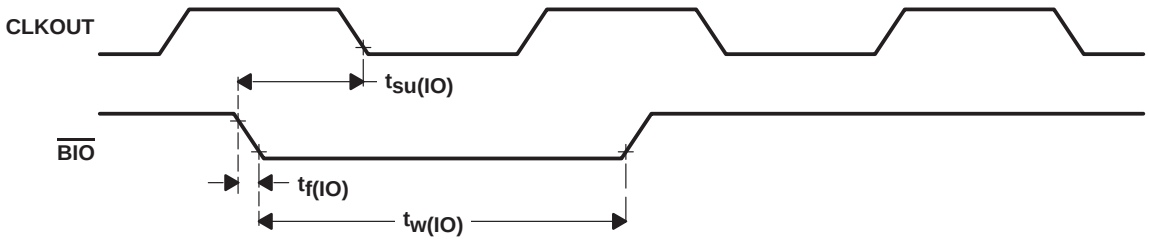


NOTES: A. RS forces DEN, WE, and MEN high and places data bus D0 through D15 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from RS↓.
B. RS must be maintained for a minimum of five clock cycles.
C. Resumption of normal program will commence after one complete CLK cycle from RS↑.
D. Due to the synchronization action on RS, time to execute the function can vary dependent upon when RS↑ or RS↓ occur in the CLK cycle.
E. Diagram shown is for definition purpose only. DEN, WE, and MEN are mutually exclusive.
F. During a write cycle, RS may produce an invalid write address.

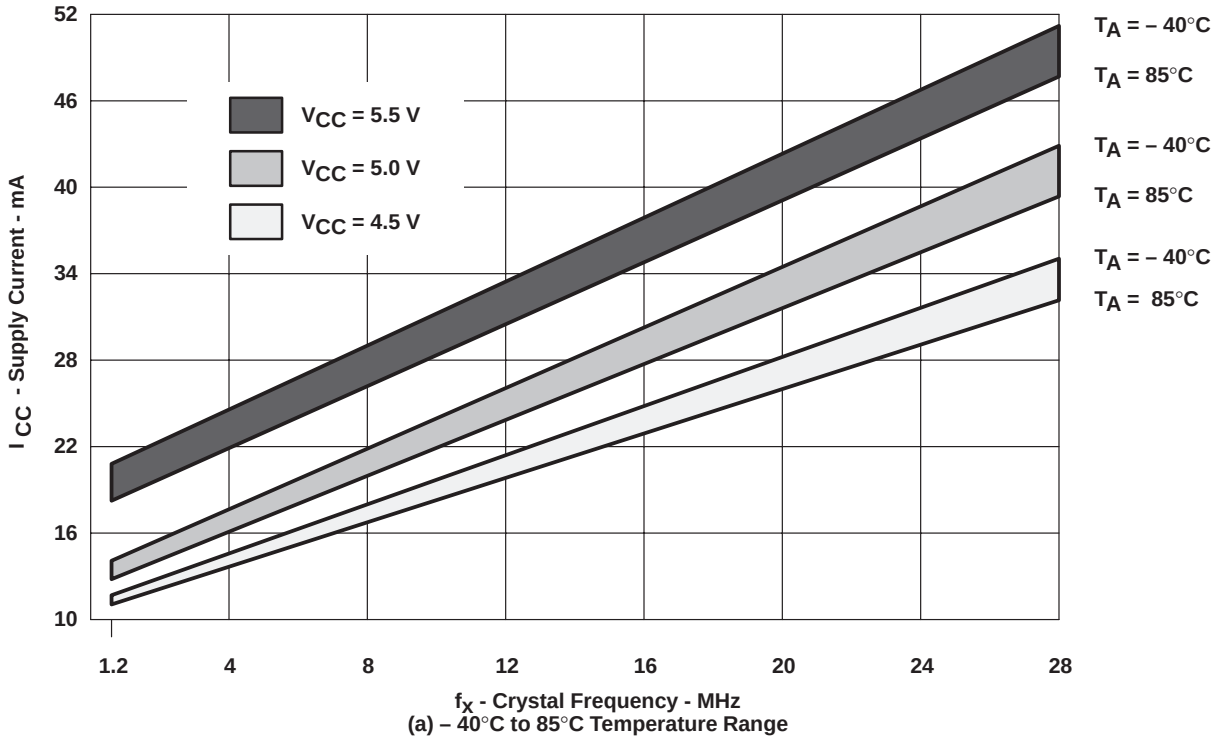
interrupt timing



BIO timing



TYPICAL POWER VS. FREQUENCY GRAPHS



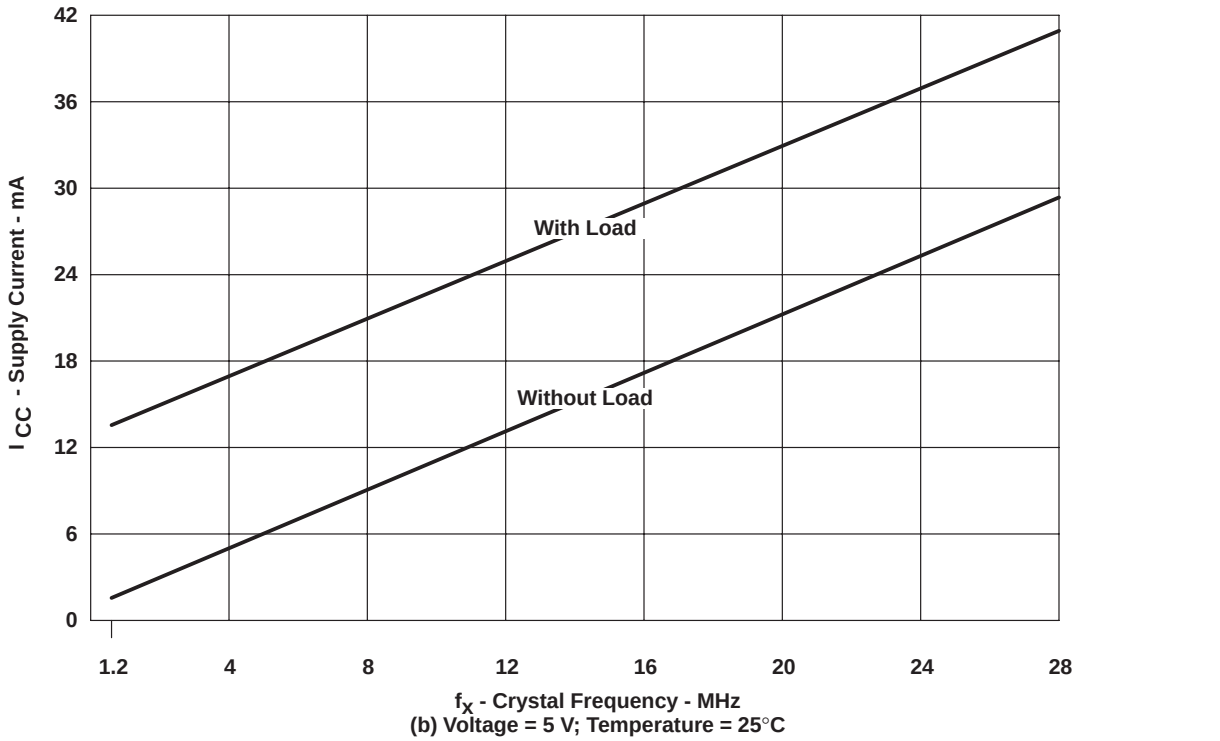
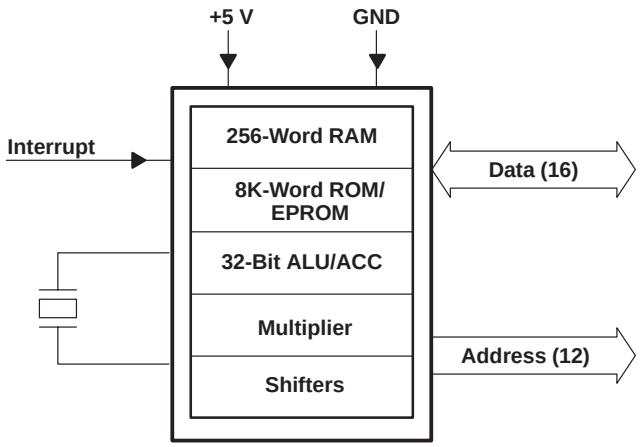


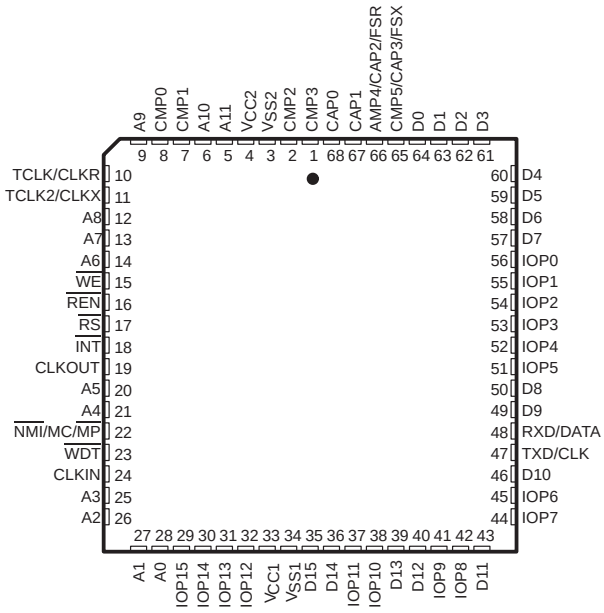
Figure 4. Typical CMOS I_{CC} vs Frequency

Key Features: TMS320C14/E14/P14

- 160-ns Instruction Cycle
- 256 Words of On-Chip Data RAM
- 4K Words of On-Chip Program ROM (TMS320C14)
- 4K Words of On-Chip Program EPROM (TMS320E14/P14)
- One-Time Programmable (OTP) Windowless EPROM Version Available (′320P14)
- EPROM Code Protection for Copyright Security
- External Memory Expansion up to 4K-Words at Full Speed (Microprocessor Mode)
- 16 × 16-Bit Multipler With 32-Bit Product
- 0 to 16-Bit Barrel Shifter
- Seven Input and Seven Output External Ports
- Bit Selectable I/O Port (16 Pins)
- 16-Bit Bidirectional Data Bus With Greater than 50-Mbps Transfer Rate
- Asynchronous Serial Port
- 15 Internal/External Interrupts
- Event Manager With Capture Inputs and Compare Outputs
- Four Independent Timers [Watchdog, General Purpose (2), Serial Port]
- Four-Level Hardware Stack
- Packaging: 68-Pin PLCC (FN Suffix) or CLCC (FZ Suffix)
- Single 5-V Supply
- Operating Free-Air Temperature . . . 0°C to 70°C



TMS320C14, TMS320E14/P14
FN/FZ Packages
(Top View)



introduction

The ′C14/E14/P14 are 16/32-bit single-chip digital signal processing (DSP) microcontrollers that combine the high performance of a DSP with on-chip peripherals. With a 160-ns instruction cycle, these devices are capable of executing up to 6.4 million instructions per second (MIPS). The ′C14/E14/P14 DSPs are ideal for applications such as automotive control systems, computer peripherals, industrial controls, and military command/control system applications.

Control-specific on-chip peripherals include: An event manager with 6 channel PWM D/A/, 6-bit I/O pins, an asynchronous serial port, four 16-bit timers, and internal/external interrupts.

With 4K-words of on-chip ROM, the ′C14 is a mask programmable device. Code is provided by the customer, and TI incorporates the customer's code into the photomask. It is offered in a 68-pin plastic chip carrier package (FN suffix), rated for operation from 0°C to 70°C.

The ′E14 is provided with a 4K-word on-chip EPROM. This EPROM version is excellent for prototyping and for customized applications. It is programmable with standard EPROM programmers. It is offered in a 68-pin (windowed) cerquad package (FZ suffix), rated for operation from 0°C to 70°C.

The ′P14 features a one-time programmable 4K-word on-chip EPROM. The ′P14 is provided in an unprogrammed state and is programmed as if it were a blank ′E14. It is offered in a low-cost, volume-production-oriented, 68-pin plastic leaded chip carrier (PLCC) package (FN suffix), rated for operation from 0°C to 70°C.

Each device can execute programs form either internal (MC/$\overline{MP}$=0) or external program memory (MC/$\overline{MP}$=1).

For proprietary code security, the ′E14 and ′P14 incorporate an EPROM protect bit (RBIT). If this bit is programmed, the device's internal program memory cannot be accessed by any external means.

TERMINAL FUNCTIONS

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			ADDRESS/DATA BUSES
A11	5	O/Z	Program memory address bus A11 (MSB) through A0 (LSB) and port addresses PA2 (MSB) through PA0 (LSB). Addresses A11 through A0 are always active and never go to high impedance except during reset. During execution of the IN and OUT instructions, pins 26, 27, and 28 carry the port addresses. Pins A3 through A11 are held high when port accesses are made on pins PA0 through PA2.
A10	6		
A9	9		
A8	12		
A7	13		
A6	14		
A5	20		
A4	21		
A3	25		
A2/PA2	26		
A1/PA1	27		
A0/PA0	28		
D15 MSB	35	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The data bus is always in the high-impedance state except when $\overline{WE}$ is active (low). The data bus is also active when internal peripherals are written to.
D14	36		
D13	39		
D12	40		
D11	43		
D10	46		
D9	49		
D8	50		
D7	57		
D6	58		
D5	59		
D4	60		
D3	61		
D2	62		
D1	63		
D0 LSB	64		
			INTERRUPT AND MISCELLANEOUS SIGNALS
$\overline{INT}$	18	I	External interrupt input. The interrupt signal is generated by a high-to-low transition on this pin.
$\overline{NMI}$/MC/$\overline{MP}$	22	I	Non-maskable interrupt. When this pin is brought low, the device is interrupted irrespective of the state of the INTM bit in status register ST. Microcomputer/microprocessor select. This pin is also sampled when $\overline{RS}$ is low. If high during reset, internal program memory is selected. If low during reset, external memory will be selected.
$\overline{WE}$	15	O	Write enable. When active low, $\overline{WE}$ indicates that device will output data on the bus.
$\overline{REN}$	16	O	Read enable. When active low, $\overline{REN}$ indicates that device will accept data from the bus.
$\overline{RS}$	17	I	Reset. When this pin is low, the device is reset and PC is set to zero.

Continued next page.

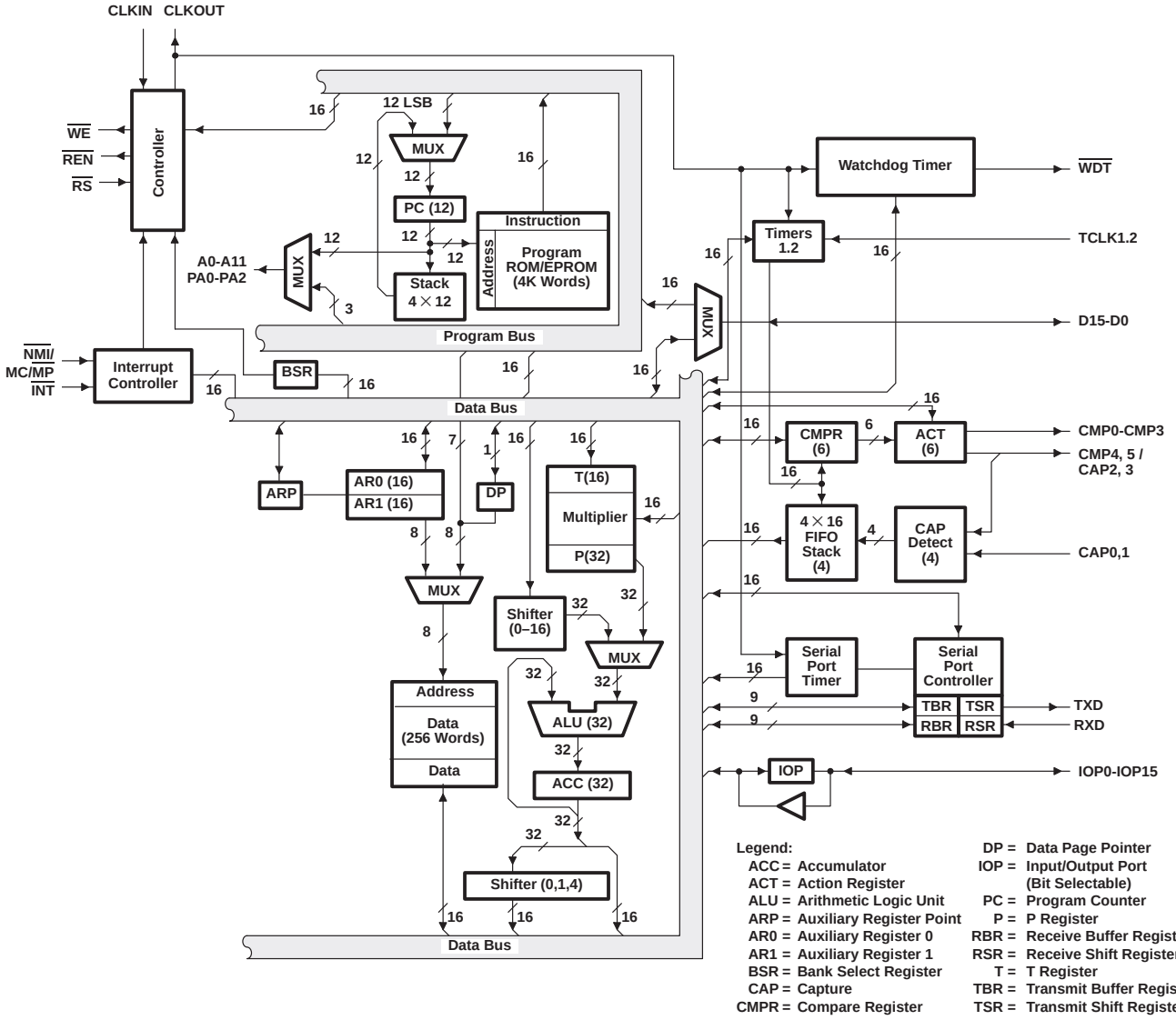
† Input/Output/High-impedance state.

TERMINAL FUNCTIONS (concluded)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			SUPPLY/OSCILLATOR SIGNALS
CLKOUT	19	O	System clock output (one fourth CLKIN frequency).
V_{CC}	4,33	I	5-V supply pins.
V_{SS}	3,34	I	Ground pins.
CLKIN	24	I	Master clock input from external clock source.
			SERIAL PORT AND TIMER SIGNALS
RXD	48	I	Asynchronous mode receive input.
TXD	47	O/Z	Asynchronous mode transmit output.
TCLK1	10	I	Timer 1 clock. If external clock is selected, it serves as clock input to Timer 1.
TCLK2	11	I	Timer 2 clock. If external clock is selected, it serves as clock input to Timer 2.
$\overline{WDT}$	23	O	Watchdog timer output. An active low is generated on this pin when the watchdog timer times out.
			BIT I/O PINS
IOP15 MSB	29	I/O	16 bit I/O lines that can be individually configured as inputs or outputs and also individually set or reset when configured as outputs.
IOP14	30		
IOP13	31		
IOP12	32		
IOP11	37		
IOP10	38		
IOP9	41		
IOP8	42		
IOP7	44		
IOP6	45		
IOP5	51		
IOP4	52		
IOP3	53		
IOP2	54		
IOP1	55		
IOP0 LSB	56		
			COMPARE AND CAPTURE SIGNALS
CMP0	8	O	Compare outputs. The states of these pins are determined by the combination of compare and action registers.
CMP1	7		
CMP2	2		
CMP3	1		
CAP0	68	I	Capture inputs. A transition on these pins causes the timer register to be captured in FIFO stack.
CAP1	67		
CMP4/CAP2	66	I/O	This pin can be configured as compare output or capture input.
CMP5/CAP3	65	I/O	This pin can be configured as compare output or capture input.

† Input/Output/High-impedance state.

functional block diagram



Legend:

ACC =	Accumulator	DP =	Data Page Pointer
ACT =	Action Register	IOP =	Input/Output Port (Bit Selectable)
ALU =	Arithmetic Logic Unit	PC =	Program Counter
ARP =	Auxiliary Register Point	P =	P Register
AR0 =	Auxiliary Register 0	RBR =	Receive Buffer Register
AR1 =	Auxiliary Register 1	RSR =	Receive Shift Register
BSR =	Bank Select Register	T =	T Register
CAP =	Capture	TBR =	Transmit Buffer Register
CMPR =	Compare Register	TSR =	Transmit Shift Register

architecture

The ′C1x family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and execution. The ′C1x family's modification of a Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

32-bit ALU/accumulator

The ′C14/E14/P14 devices contain a 32-bit ALU and accumulator for support of double-precision, twos-complement arithmetic. The ALU is a general-purpose arithmetic unit that operates on 16-bit words taken from the data RAM or derived from immediate instructions. In addition to the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

The accumulator stores the output from the ALU and is often an input to the ALU. It operates with a 32-bit wordlength. The accumulator is divided into a high-order word (bits 31 through 16) and a low-order word (bits 15 through 0). Instructions are provided for storing the high- and low- order accumulator words in memory.

shifters

Two shifters are available for manipulating data. The ALU barrel shifter performs a left-shift of 0 to16 places on data memory words loaded into the ALU. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for twos-complement arithmetic. The accumulator parallel shifter performs a left-shift of 0, 1, or 4 places on the entire accumulator and places the resulting high-order accumulator bits into data RAM. Both shifters are useful for scaling and bit extraction

16 × 16-bit parallel multiplier

The multiplier performs a 16 × 16-bit twos-complement multiplication with a 32-bit result in a single instruction cycle. The multiplier consists of three units: the T Register, P Register, and the multiplier array. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit product. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the device to perform fundamental operations such as convolution, correlation, and filtering.

data and program memory

Since the ′C14/E14/P14 devices use a Harvard architecture, data and program memory reside in two separate spaces. These devices have 256 words of on-chip data RAM and 4K words of on-chip program ROM (′C14) or EPROM (′E14 and the OTP ′P14). The EPROM cell utilizes standard PROM programmers and is programmed identically to a 64K-bit CMOS EPROM (TMS27C64).

program memory expansion

The ′C1x devices are capable of executing up to 4K words of external memory at full speed for those applications requiring external program memory space. This allows for external RAM-based systems to provide multiple functionality.

microcomputer/microprocessor operating modes

The ′C14/E14/P14 devices offer two modes of operation defined by the state of the $\overline{\text{NMI}}$/MC/$\overline{\text{MP}}$ pin during reset: the microcomputer mode ($\overline{\text{NMI}}$/MC/$\overline{\text{MP}}$ is high) or the microprocessor mode ($\overline{\text{NMI}}$/MC/$\overline{\text{MP}}$ is low). In the microcomputer mode, the on-chip ROM is mapped into the program memory space. In the microprocessor mode, all 4K words of memory are external.

interrupts and subroutines

The ′C14/E14/P14 devices contain a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the complete context of the device. PUSH and POP instructions permit a level of nesting restricted only by the amount of available RAM. The ′C14/E14/P14 have a total of 15 internal/external interrupts. Fourteen of these are maskable; $\overline{\text{NMI}}$ is the fifteenth.

input/output

The 16-bit parallel data bus can be utilized to access external peripherals. However, only the lower three address lines are active. The upper nine address lines are driven high.

bit I/O

The ′C14/E14/P14 has 16 pins of bit I/O that can be individually configured as inputs or outputs. Each of the pins can be set or cleared without affecting the others. The input pins can also detect and match patterns and generate a maskable interrupt signal to the CPU.

serial port

The ′C14/E14/P14 includes an I/O-mapped asynchronous serial port.

event manager

An event manager is included that provides up to four capture inputs and up to six compare outputs. This peripheral operates with the timers to provide a form of programmable event logging/detection. The six compare outputs can also be configured to produce six channels of high precision PWM.

timers 1 and 2

Two identical 16-bit timers are provided for general purpose applications. Both timers include a 16-bit period register and buffer latch, and can generate a maskable interrupt.

serial port timer

The serial port timer is a 16-bit timer primarily intended for baud rate generation for the serial port. Its architecture is the same as timers 1 and 2, therefore it can serve as a general purpose timer if not needed for serial communication.

watchdog timer

The ′C14/E14/P14 contain a 16-bit watchdog timer that can produce a timeout ($\overline{\text{WDT}}$) signal for various applications such as software development and event monitoring. The watchdog timer also generates, at the point of the timeout, a maskable interrupt signal to the CPU.

instruction set

A comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general-purpose operations, such as high-speed control. All of the first-generation devices are object-code compatible and use the same 60 instructions. The instruction set consists primarily of single-cycle single-word instructions, permitting execution rates of more than six million instructions per second. Only infrequently used branch and I/O instructions are multicycle. Instructions that shift data as part of an arithmetic operation execute in a single cycle and are useful for scaling data in parallel with other operations.

NOTE

The $\overline{\text{BIO}}$ pin on other ′C1x devices is not available for use in the ′C14/E14/P14 devices. An attempt to execute the BIOZ (Branch on $\overline{\text{BIO}}$ low) instruction will result in a two cycle NOP action.

Three main addressing modes are available with the instruction set: direct, indirect, and immediate addressing.

direct addressing

In direct addressing, seven bits of the instruction word concatenated with the 1-bit data page pointer from the data memory address. This implements a paging scheme in which each page contains 128 words.

indirect addressing

Indirect addressing forms the data memory address from the least-significant eight bits of one of the two auxiliary registers, AR0 and AR1. The Auxiliary Register Pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented and the ARP changed in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

immediate addressing

Immediate instructions derive data from part of the instruction word rather than from part of the data RAM. Some useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

electrical specifications

This section contains all the electrical specifications for the ′C14/E14/P14 devices, including test parameter measurement information. Parameters with $_{PP}$ subscripts apply only to the ′E14 and ′P14 in the EPROM programming mode.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 6) . . . . . –0.3 V to 7 V
Supply voltage range, V_{PP} (see Note 6) . . . . . –0.6 V to 14 V
Input voltage range . . . . . –0.3 V to 14 V
Output voltage range . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . 0.5 W
Air temperature range above operating device: L version . . . . . 0 °C to 70 °C
Storage temperature . . . . . –55 °C + 150 °C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Operating voltage	4.75	5	5.25	V
		Fast programming	5.75	6	6.25	V
		SNAP! Pulse programming	6.25	6.5	6.75	V
V_{PP}	Supply voltage for Fast programming (see Note 11)		12.25	12.5	12.75	V
V_{PP}	Supply voltage for SNAP! Pulse programming (see Note 11)		12.75	13	13.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN, CAP0, CAP1, CMP4/CAP2, CMP5/CAP3, $\overline{RS}$	3			V
		All remaining inputs	2			
V_{IL}	Low-level input voltage, all inputs				0.8	V
I_{OH}	High-level output current, all outputs				–300	µA
I_{OL}	Low-level output current, all outputs				2	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 11: V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 μA (see Note 7)		V_{CC} – 0.4†			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{OZ}	Off-state output voltage		V_{CC} = MAX	V_O = 2.4 V			20	μA
				V_O = 0.4 V			–20	
I_I	Input current		V_I = V_{SS} to V_{CC}	All other inputs except CLKIN			±20	μA
				CLKIN			±50	
I_{CC}§	Supply current		f = 25.6 MHz, V_{CC} = 5.25 V, T_A = 0°C to 70°C			70	90	mA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V				100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V			30	50	mA
C_I	Input capacitance	Data bus	f = 1 MHz, All other pins 0 V			25‡		pF
		All others				15‡		
C_O	Output capacitance	Data bus				25‡		pF
		All others				10‡		

† All typical values are at V_{CC} = 5 V, T_A = 25°C, except I_{CC} at 70°C.
‡ Values derived from characterization data and not tested.
§ I_{CC} characteristics are inversely proportional to temperature.
NOTE 7: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

PARAMETER MEASUREMENT INFORMATION

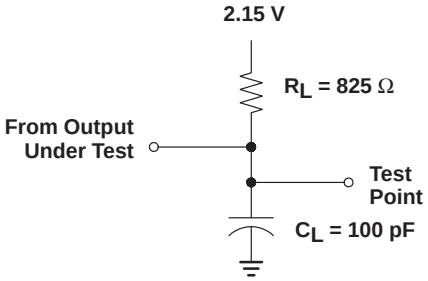


Figure 5. Test Load Circuit

EXTERNAL CLOCK REQUIREMENTS

The TMS320C14/E14/P14 use an external frequency source for a clock. This source is applied to the CLKIN pin, and must conform to the specifications in the table below.

PARAMETERS		TEST CONDITIONS	MIN	NOM	MAX	UNIT
CLKIN	Input clock frequency	T_A = 0°C to 70°C	6.7		25.6	MHz

CLOCK TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time‡	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	156.25		600	ns
$t_{r(C)}$	CLKOUT rise time			10†		ns
$t_{f(C)}$	CLKOUT fall time			8†		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			72†		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			70†		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓			45†		ns

† Values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time‡	39.06	40	150	ns
$t_{r(MC)}$	Rise time, master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time, master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.45t_{c(MC)}$†		$0.55t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration, master clock low		15†	130	ns
$t_{w(MCH)}$	Pulse duration, master clock high		15†	130	ns

† Values were derived from characterization data and not tested.
‡ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).

MEMORY READ AND INSTRUCTION TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(A)R}$	Address bus valid before $\overline{REN}\downarrow$	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	0.25 $t_{c(C)}$ – 39			ns
$t_{su(A)W}$	Address bus valid before $\overline{WE}\downarrow$		0.50 $t_{c(C)}$ – 45			ns
$t_{h(A)}$	Address bus valid after $\overline{REN}\uparrow$ or $\overline{WE}\uparrow$		5†			ns
$t_{en(D)W}$	Data starts being driven before $\overline{WE}\downarrow$				0.25 $t_{c(C)}$†	ns
$t_{su(D)W}$	Data valid prior to $\overline{WE}\downarrow$		0.25 $t_{c(C)}$ – 45			ns
$t_{h(D)W}$	Data valid after $\overline{WE}\uparrow$		0.25 $t_{c(C)}$ – 10			ns
$t_{dis(D)W}$	Data in high impedance after $\overline{WE}\uparrow$				0.25 $t_{c(C)}$ + 25†	ns
$t_{w(WEL)}$	$\overline{WE}$-low duration		0.50 $t_{c(C)}$ – 15			ns
$t_{w(RENL)}$	$\overline{REN}$-low duration		0.75 $t_{c(C)}$ – 15			ns
$t_{rec(WE)}$	Write recovery time, time between $\overline{WE}\uparrow$ and $\overline{REN}\downarrow$		0.25 $t_{c(C)}$ – 5			ns
$t_{rec(REN)}$	Read recovery time, time between $\overline{REN}\uparrow$ and $\overline{WE}\downarrow$		0.50 $t_{c(C)}$ – 10			ns
$t_{d(WE-CLK)}$	Time from $\overline{WE}\uparrow$ to CLKOUT↑		0.50 $t_{c(C)}$ – 15			ns

† Values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)R}$	Data set-up prior to $\overline{REN}\uparrow$	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	52			ns
$t_{h(D)R}$	Data hold after $\overline{REN}\uparrow$		0			ns
$t_{a(A)}$	Access time for read cycle data valid after valid address				$t_{c(C)}$ – 90	ns
$t_{oe(REN)}$	Access time for read cycle from $\overline{REN}\downarrow$				0.75 $t_{c(C)}$ – 60	ns
$t_{dis(D)R}$	Data in high impedance after $\overline{REN}\uparrow$				0.25 $t_{c(C)}$†	ns

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{d(RS-RW)}$	Delay from $\overline{RS}\downarrow$ to $\overline{REN}\uparrow$ and $\overline{WE}\uparrow$	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			0.75 $t_{c(C)}$ + 20†	ns
$t_{dis(RS-RW)}$	Delay from $\overline{RS}\downarrow$ to $\overline{REN}$ and $\overline{WE}$ into high impedance				1.25 $t_{c(C)}$†	ns
$t_{dis(RS-DB)}$	Data bus disable after $\overline{RS}\downarrow$				1.25 $t_{c(C)}$†	ns
$t_{dis(RS-AB)}$	Address bus disable after $\overline{RS}\downarrow$				$t_{c(C)}$†	ns
$t_{en(RS-AB)}$	Address bus enable after $\overline{RS}\uparrow$				$t_{c(C)}$†	ns

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(RS)}$	$\overline{RS}$ setup prior to CLKOUT↓ (see Note 10)	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	60			ns
$t_{w(RS)}$	$\overline{RS}$ pulse duration		5$t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during the clock cycle. Time given is minimum to ensure synchronous operation.

MICROCOMPUTER/MICROPROCESSOR MODE ($\overline{NMI}$/MC/$\overline{MP}$)

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{h(MC/MP)}$‡	Hold time after $\overline{RS}$ high	$t_{c(C)}$			ns

† Values were derived from characterization data and not tested.
‡ Hold time to put device in microprocessor mode.

INTERRUPT ($\overline{INT}$)/NONMASKABLE INTERRUPT ($\overline{NMI}$)

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(INT)}$	Fall time, $\overline{INT}$			15†	ns
$t_{f(NMI)}$	Fall time, $\overline{NMI}$			15†	ns
$t_{w(INT)}$	Pulse duration, $\overline{INT}$	$t_{c(C)}$			ns
$t_{w(NMI)}$	Pulse duration, $\overline{NMI}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time, $\overline{INT}$ before CLKOUT low (see Note 12)	60			ns
$t_{su(NMI)}$	Setup time, $\overline{NMI}$ before CLKOUT low (see Note 12)	60			ns

NOTE 12: $\overline{INT}$ and $\overline{NMI}$ are synchronous inputs and can occur at any time during the cycle. $\overline{NMI}$ and $\overline{INT}$ are edge triggered only.

BIT I/O TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{rfo(IOP)}$	Rise and fall time outputs	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			20†	ns
$t_{d(IOP)}$	CLKOUT low to data valid outputs				0.75 $t_{c(C)}$ + 80	ns

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{rfl(IOP)}$	Rise and fall time inputs	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			20†	ns
$t_{su(IOP)}$	Data setup time before CLKOUT time		40			ns
$t_{w(IOP)}$	Input pulse duration		$t_{c(C)}$			ns

GENERAL PURPOSE TIMERS

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{r(TIM)}$	TCLK1, TCLK2 rise time	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			20†	ns
$t_{f(TIM)}$	TCLK1, TCLK2 fall time				20†	ns
$t_{wl(TIM)}$	TCLK1, TCLK2 low time		$t_{c(C)}$ + 20			ns
$t_{wh(TIM)}$	TCLK1, TCLK2 high time		$t_{c(C)}$ + 20			ns
$t_{clk(TIM)}$	Input pulse duration		$2t_{c(C)}$ + 40			ns

† Values were derived from characterization data and not tested.

WATCHDOG TIMER TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{f(WDT)}$	Fall time, $\overline{WDT}$	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			20†	ns
$t_{d(WDT)}$	CLKOUT to $\overline{WDT}$ valid		0.25 $t_{c(C)}$ + 20			ns
$t_{w(WDT)}$	WDT output pulse duration		7 $t_{c(C)}$			ns

EVENT MANAGER TIMER

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{f(CMP)}$	Fall time, CMP0-CMP5	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			20†	ns
$t_{r(CMP)}$	Rise time, CMP0-CMP5				20†	ns

timing requirements over recommended operating conditions

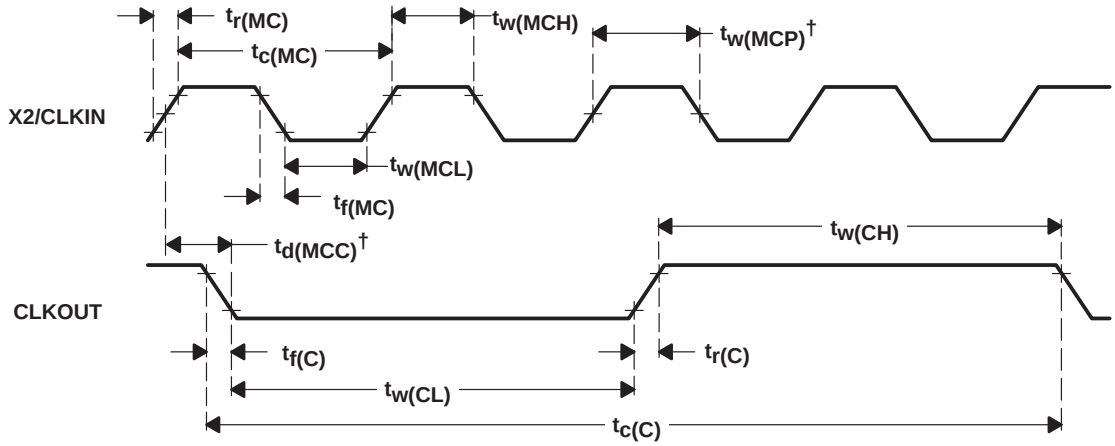
		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	CAP0-CAP3 input pulse duration	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	$t_{c(C)}$ + 20			ns
$t_{su(CAP)}$	Capture input setup time before CLKOUT low		20†			ns

† Values were derived from characterization data and not tested.

TIMING DIAGRAMS

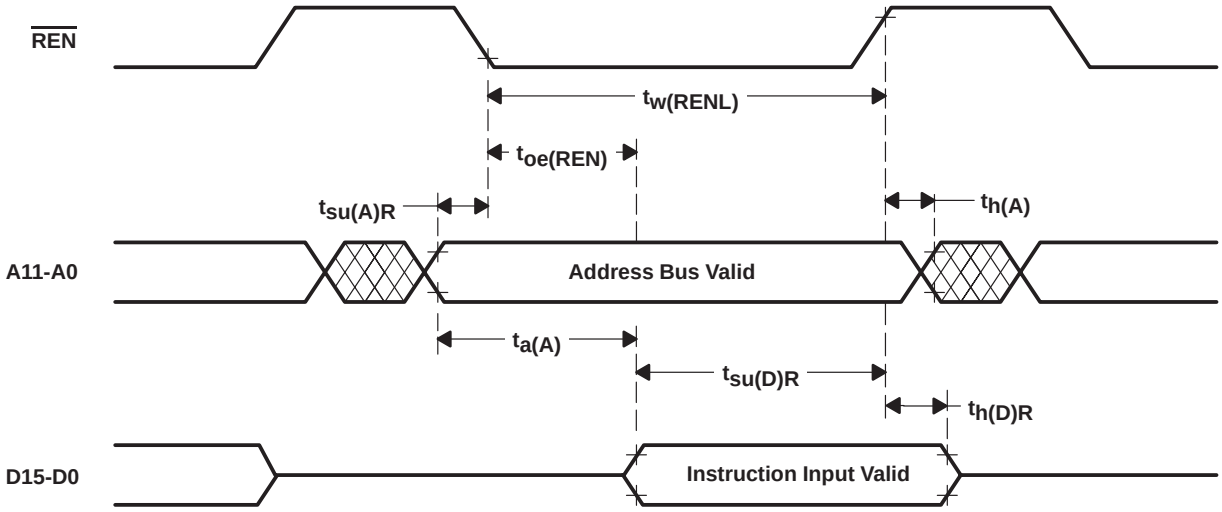
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2 volts, unless otherwise noted.

clock timing

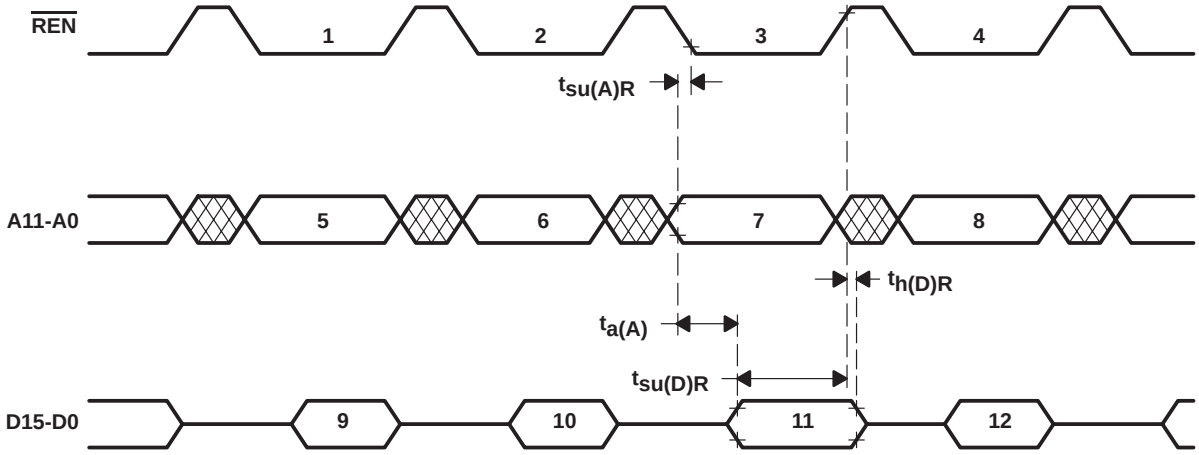


† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

memory read timing



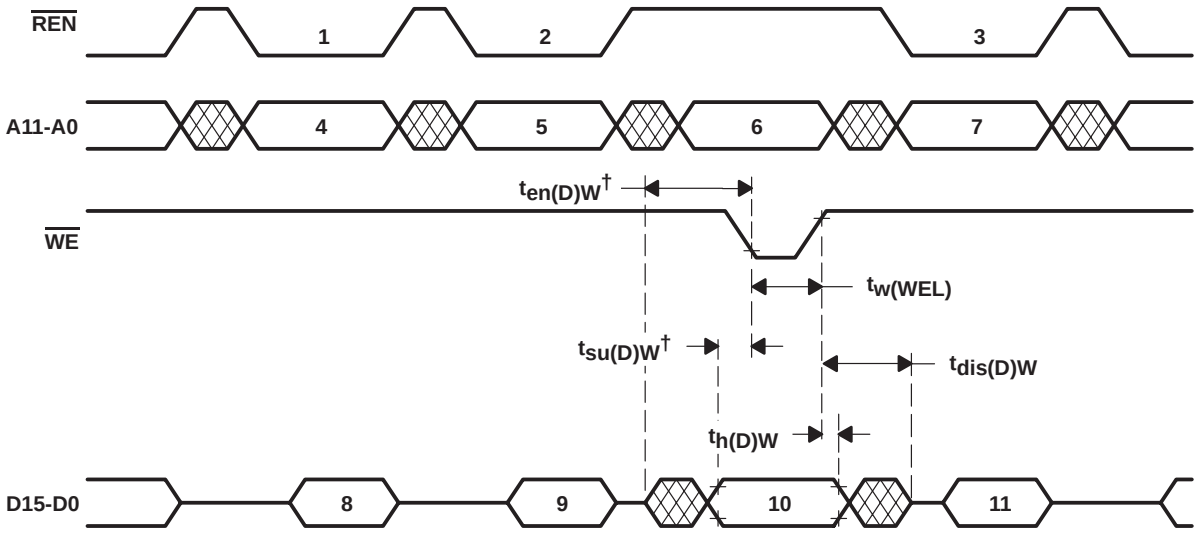
TBLR instruction timing



Legend:

1. TBLR Instruction Prefetch
2. Dummy Prefetch
3. Data Fetch
4. Next Instruction Prefetch
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Address Bus Valid
9. Instruction Input Valid
10. Instruction Input Valid
11. Data Input Valid
12. Instruction Input Valid

TBLW instruction timing

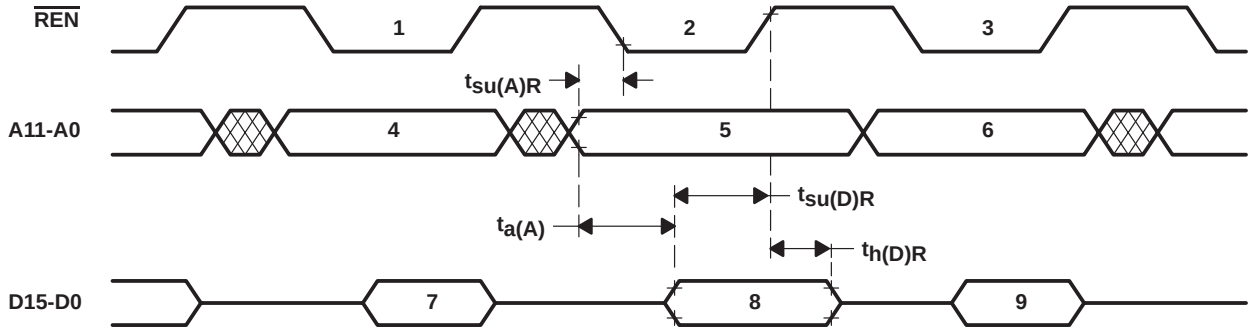


† Data valid prior to $\overline{WE}\downarrow$

Legend:

1. TBLW Instruction Prefetch
2. Dummy Prefetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Instruction Input Valid
9. Instruction Input Valid
10. Data Output Valid
11. Instruction Input Valid

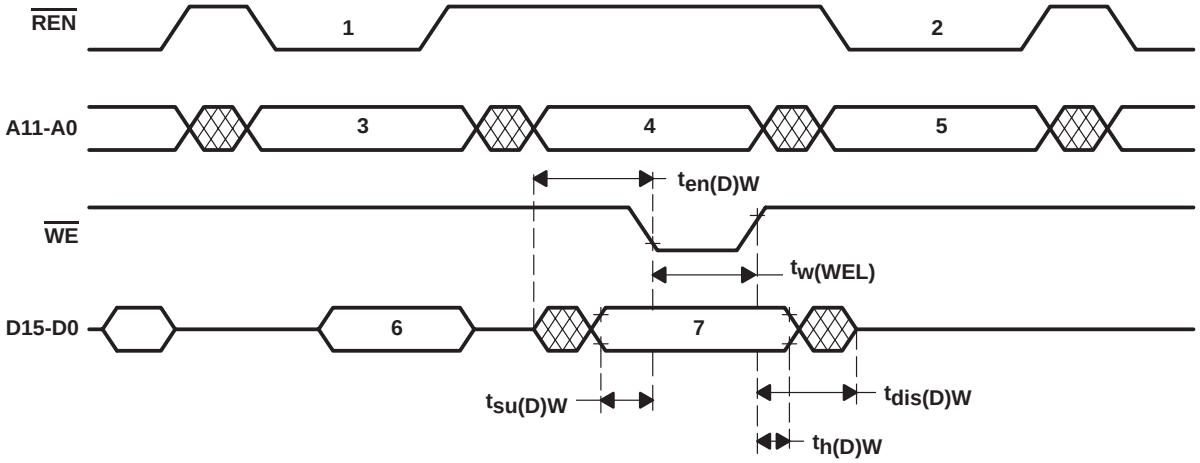
IN instruction timing



Legend:

1. IN Instruction Prefetch
2. Data Fetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Peripheral Address Valid
6. Address Bus Valid
7. Instruction Input Valid
8. Data Input Valid
9. Instruction Input Valid

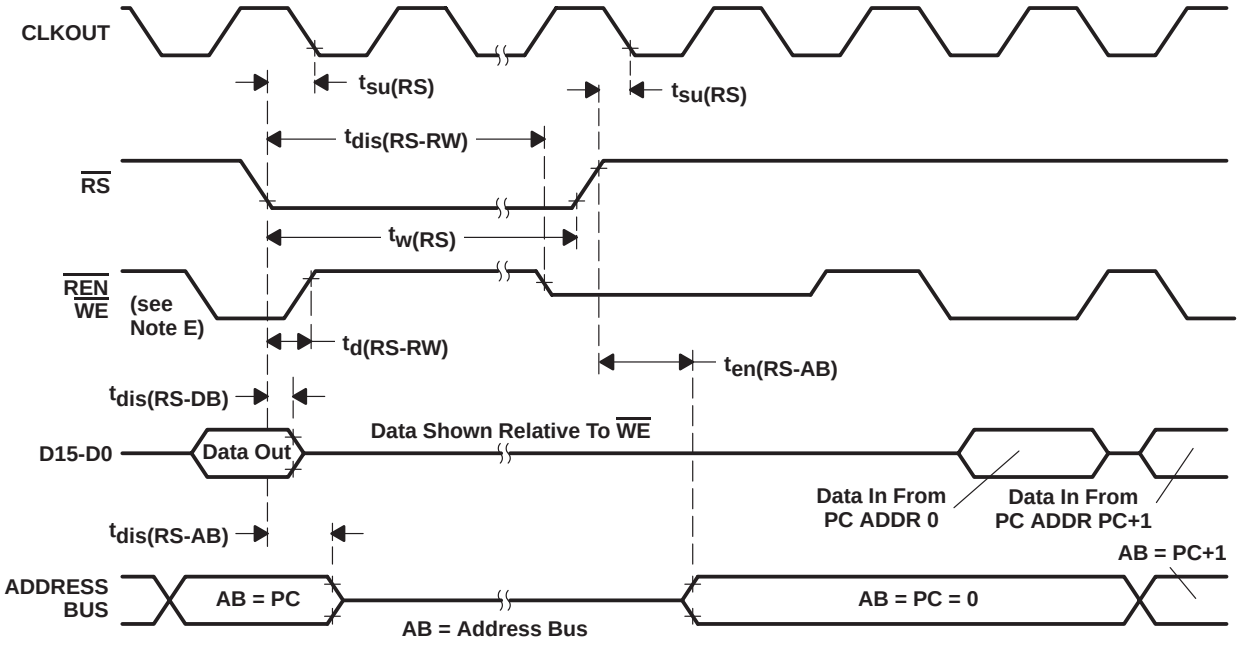
OUT instruction timing



Legend:

1. OUT Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Input Valid
7. Data Output Valid

reset timing



NOTES: A. $\overline{RS}$ forces $\overline{REN}$, and $\overline{WE}$ high and then places data bus D0-D15, $\overline{REN}$, $\overline{WE}$, and address bus A0-A11 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}\uparrow$.

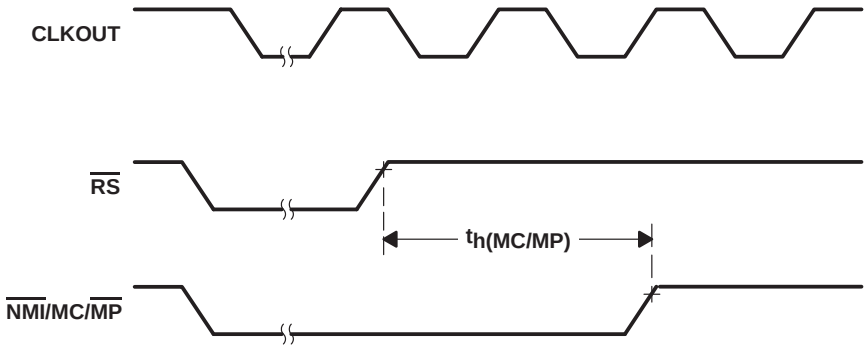
B. $\overline{RS}$ must be maintained for a minimum of five clock cycles.

C. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}\uparrow$.

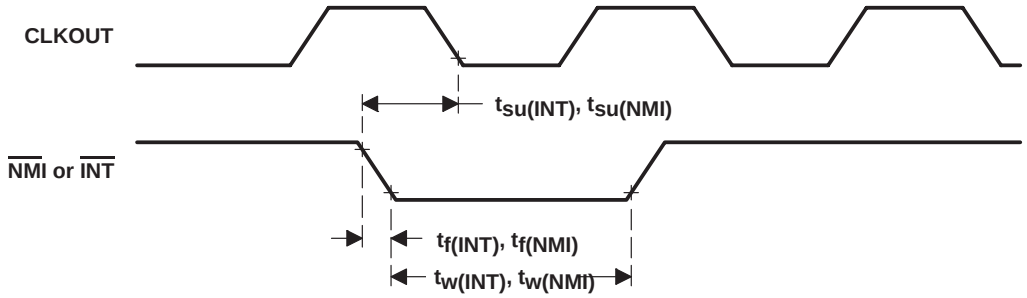
D. Due to the synchronization action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}\uparrow$ or $\overline{RS}\downarrow$ occur in the CLK cycle.

E. Diagram shown is for definition purpose only. $\overline{WE}$ and $\overline{REN}$ are mutually exclusive.

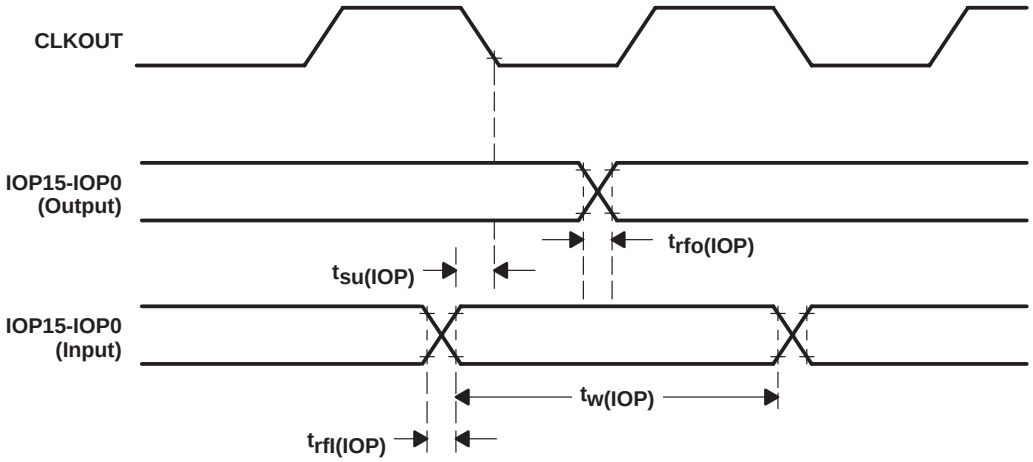
microcomputer/microprocessor mode timing



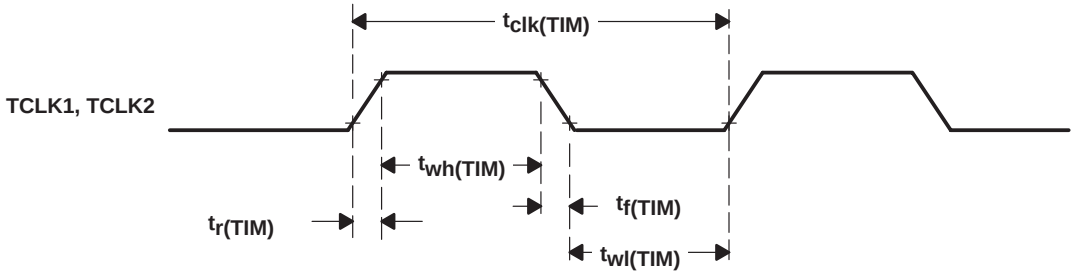
interrupt timing



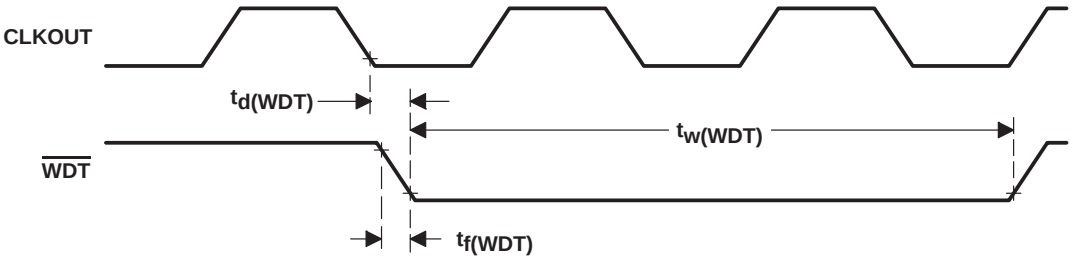
bit I/O timing



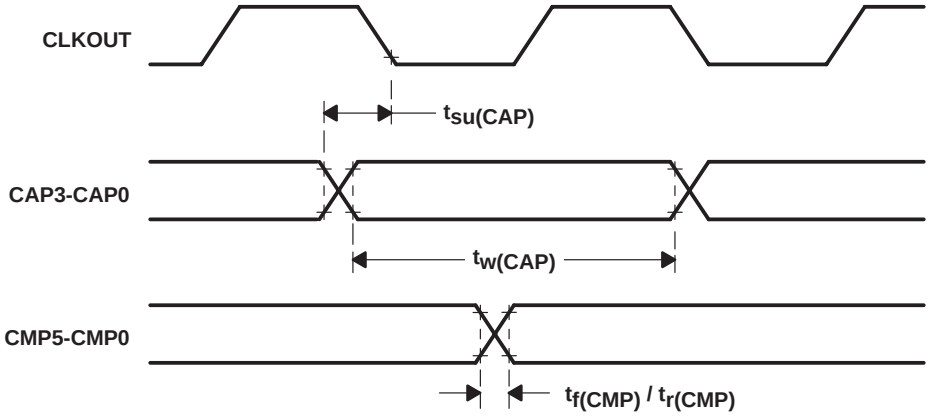
general purpose timers



watchdog timer



event manager



PROGRAMMING THE TMS320E14/P14 EPROM CELL

The ′E14 and ′P14 include a 4K × 16-bit industry-standard EPROM cell for prototyping and low-volume production. The ′C14 with a 4K-word masked ROM then provides a migration path for cost-effective production. An EPROM adapter socket (part # TMDX3270110), shown in Figure 5, is available to provide 68-pin to 28-pin conversion for programming the ′E14 and ′P14.

Key features of the EPROM cell include the normal programming operation as well as verification. The EPROM cell also includes a code protection feature that allows code to be protected against copyright violations.

The ′E14/P14 EPROM cells are programmed using the same family and device codes as the TMS27C64 8K × 8-bit EPROM. The TMS27C64 EPROM series are ultraviolet-light erasable, electrically programmable, read-only memories, fabricated using HVCMOS technology. They are pin compatible with existing 28-pin ROMs and EPROMs. These EPROMs operate from a 5-V supply in the read mode; however, a 12.5-V supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

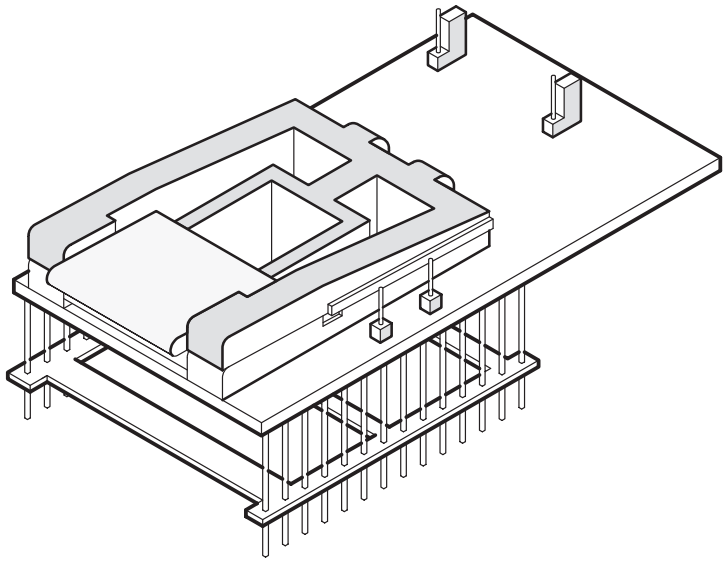


Figure 5. EPROM Adapter Socket

The ′E14/P14 devices use 13 address lines to address the 4K-word memory in byte format (8K-byte memory). In word format, the most-significant byte of each word is assigned an even address and the least-significant byte an odd address in the byte format. Programming information should be downloaded to EPROM programmer memory in a high-byte to low-byte order for proper programming of the devices (see Figure 6).

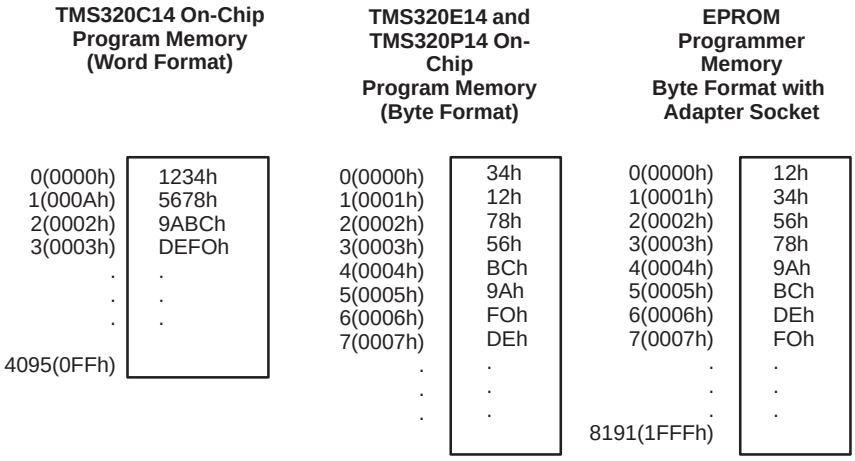


Figure 6. Programming Data Format

Figure 7 shows the wiring conversion to program the ′E14 and ′P14 using the 28-pin pinout of the TMS27C64. The table of pin nomenclature provides a description of the TMS27C64 pins.

CAUTION

The ′E14 and ′P14 do not support the signature mode available with some EPROM programmers. The signature mode places high voltage (12.5 V_{dc}) on pin A9. The ′E14 and ′P14 EPROM cells are not designed for this feature and will be damaged if subjected to it. A 3.9 kΩ resistor is standard on the TI programmer socket between pin A9 and programmer. This protects the device from unintentional use of the signature mode.

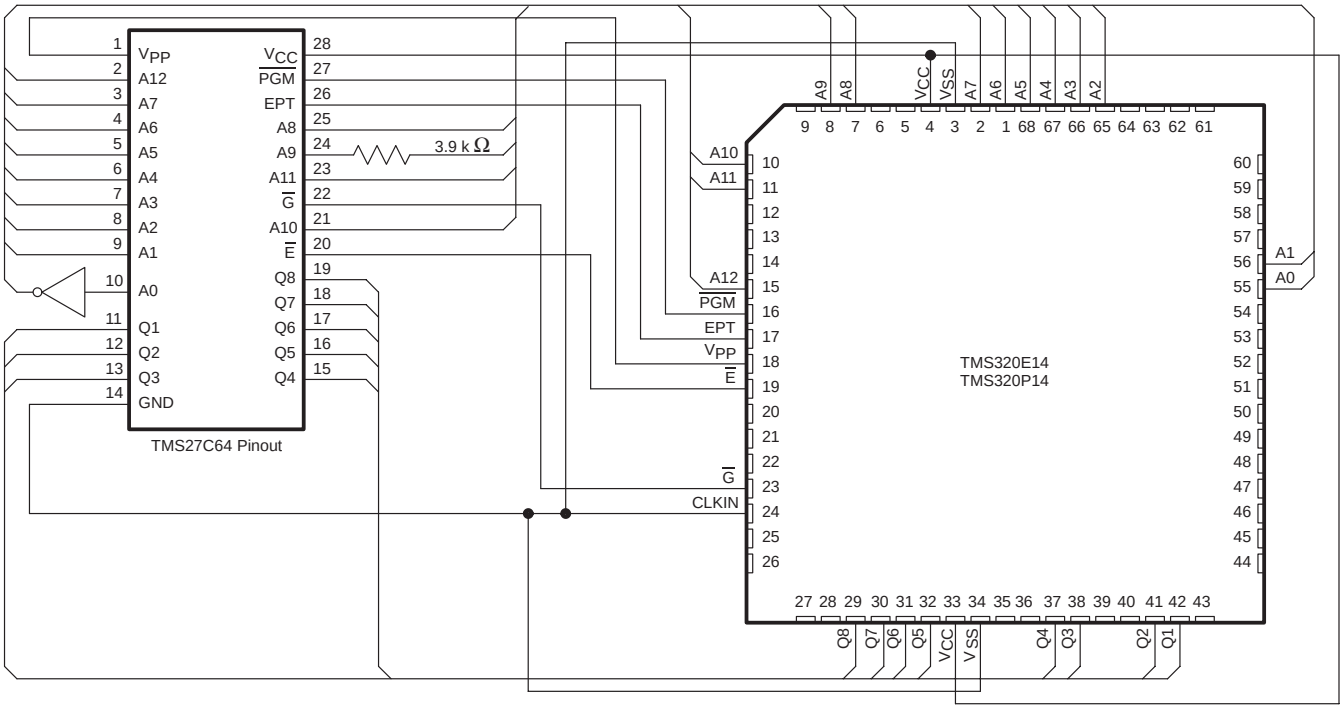


Figure 7. TMS320E14/P14 EPROM Programming Conversion to TMS27C64 EPROM Pinout

TERMINAL FUNCTIONS (TMS320E14/P14)

NAME	I/O	DEFINITION
A12(MSB)-A0(LSB)	I	On-chip EPROM programming address lines
CLKIN	I	Clock oscillator input
$\overline{E}$	I	EPROM chip enable
EPT	I	EPROM test mode select
$\overline{G}$	I	EPROM output enable
GND	I	Ground
$\overline{PGM}$	I	EPROM write/program select
Q8(MSB)-Q1(LSB)	I/O	Data lines for byte-wide programming of on-chip 8K bytes of EPROM
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	5-V to 6.5-V power supply
V_{PP}	I	12.5-V to 13-V power supply

Table 4 shows the programming levels required for programming, verifying, reading, and protecting the EPROM cell.

Table 4. TMS320E14/P14 Programming Mode Levels

SIGNAL NAME†	TMS320E14/P14 PIN	TMS27C64 PIN	PROGRAM	PROGRAM VERIFY	READ	EPROM PROTECT	PROTECT VERIFY
$\overline{E}$	19	20	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}
$\overline{G}$	23	22	V_{IH}	$\overline{PULSE}$	$\overline{PULSE}$	V_{IH}	V_{IL}
$\overline{PGM}$	16	27	$\overline{PULSE}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}
V_{PP}	18	1	V_{PP}	V_{PP}	V_{CC}	V_{PP}	V_{CCP}
V_{CC}	4,33	28	V_{CCP}	V_{CCP}	V_{CC}	V_{CCP}	V_{CCP}
V_{SS}	3,34	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
CLKIN	24	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
EPT	17	26	V_{SS}	V_{SS}	V_{SS}	V_{PP}	V_{PP}
Q1-Q8	42, 41, 38, 37, 32-29	11–13, 15-19,	Data In	Data Out	Data Out	$Q_8 = \overline{PULSE}$	Q_8 = RBIT
A12-A7	15, 11, 10, 8, 7, 2	2, 23, 21, 24, 25, 3	ADDR	ADDR	ADDR	X	X
A6	1	4	ADDR	ADDR	ADDR	X	V_{IL}
A5	68	5	ADDR	ADDR	ADDR	X	X
A4	67	6	ADDR	ADDR	ADDR	V_{IH}	X
A3-A0	66, 65, 56, 55	7-10	ADDR	ADDR	ADDR	X	X

† Signal names shown for ′E14/P14 EPROM programming mode only.

Legend:

V_{IH} = TTL high level; V_{IL} = TTL low level; ADDR = byte address bit; V_{PP} = 12.5 V ± 0.25 V (FAST) or 13 V ± 0.25 V (SNAP! Pulse).
V_{CC} = 5 V ± 0.25 V; X = don't care; $\overline{PULSE}$ = low-going TTL pulse.
D_{IN} = byte to be programmed at ADDR; Q_{OUT} = byte stored at ADDR.; RBIT = ROM protect bit
V_{CCP} = 6 V ± 0.25 V (FAST) or 6.5 V ± 0.25 V (SNAP! Pulse).

programming

Since every memory in the cell is at a logic high, the programming operation reprograms selected bits to low. Once the ′320E14 is programmed, these bits can only be erased using ultraviolet light. The correct byte is placed on the data bus with V_{PP} set to the 12.5-V level. The $\overline{PGM}$ pin is then pulsed low to program in the zeros.

erasure

Before programming, the ′E14 must be erased by exposing it to ultraviolet light. The recommended minimum exposure dose (UV-intensity × exposure-time) is 15 W•s/cm^2. A typical 12-mW•s/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After exposure, all bits are in the high state.

verify/read

To verify correct programming, the EPROM cell can be read using either the verify or read line definitions shown in Table 5, assuming the inhibit bit (RBIT) has not been programmed.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

standard programming procedure

Before programming, the ′E14 must first be completely erased. The device can then be programmed with the correct code. It is advisable to program unused sections with zeros as a further security measure. After the programming is complete, the code programmed into the cell should be verified. If the cell passes verification, the next step is to program the ROM protect bit (RBIT). Once the RBIT programming is verified, an opaque label should be placed over the window to protect the EPROM cell from inadvertent erasure by ambient light. At this point, the programming is complete, and the device is ready to be placed into its destination circuit.

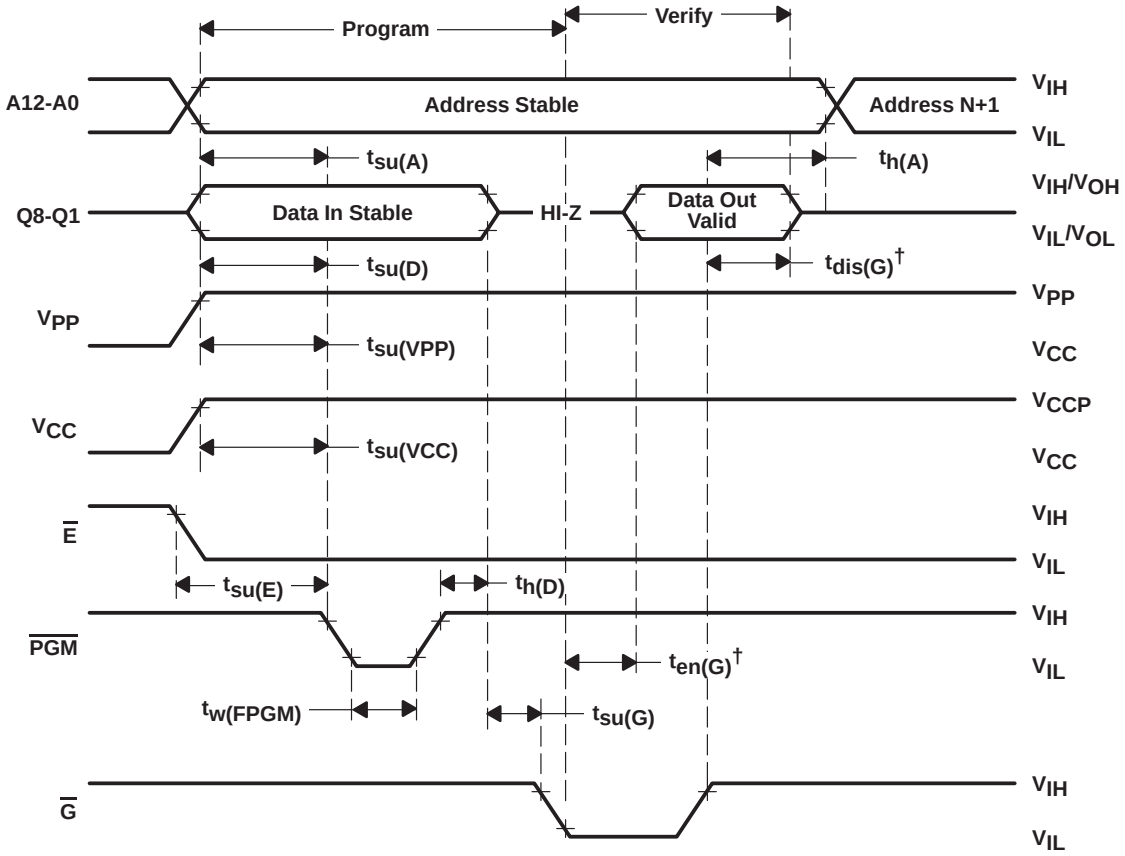
Refer to other appendices of the *TMS320C1x User's Guide* for additional information on EPROM programming.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (FAST) or V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! PULSE), T_A = 25°C (see Note 13)

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 13: For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V and V_{PP} = 12.5 V ± 0.5 V during programming.

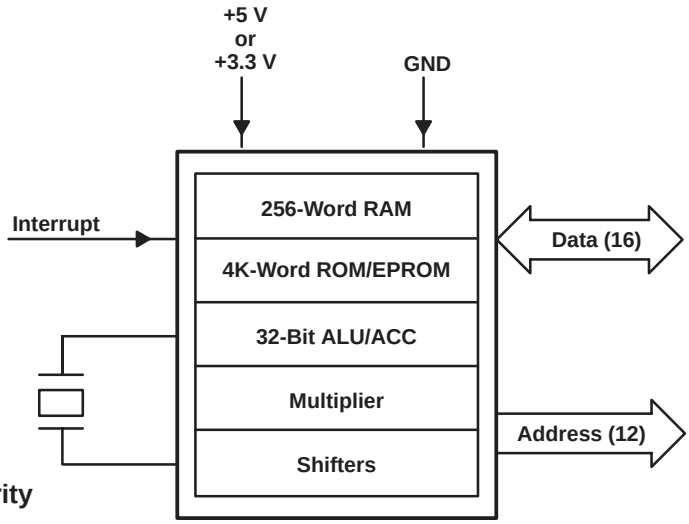
program cycle timing



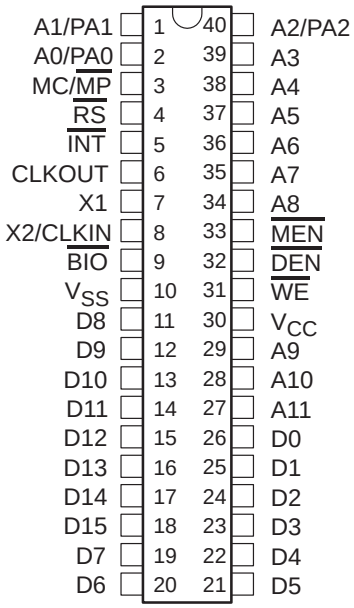
† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.

Key Features: TM320C15/E15/LC15/P15

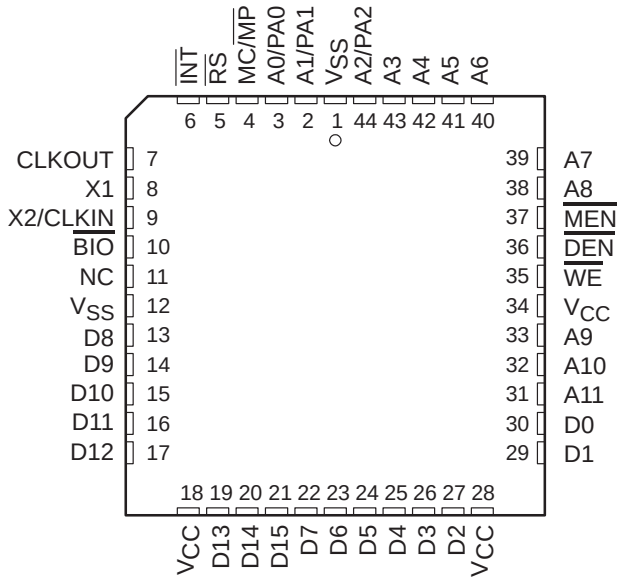
- **Instruction Cycle Timing:**
  - **160-ns (TMS320C15-25/E15-25)**
  - **200-ns (TMS320C15/E15/P15)**
  - **250-ns (TMS320LC15)**
- **256 Words of On-Chip Data RAM**
- **4K Words of On-Chip Program ROM (TMS320C15/C15-25/LC15)**
- **4K Words of On-Chip Program EPROM (TMS320E15/E15-25)**
- **One-Time Programmable (OTP) Windowless EPROM Version Available (TMS320P15)**
- **EPROM Code Protection for Copyright Security**
- **External Memory up to 4K-Words at Full Speed**
- **16 × 16-Bit Multiplier With 32-Bit Product**
- **0 to 16-Bit Barrel Shifter**
- **On-Chip Clock Oscillator**
- **3.3-V Low-Power Version Available (TMS320LC15)**
- **Device Packaging:**
  - **40-Pin Dip (All Devices)**
  - **44-Lead PLCC (TMS320C15/C15-25/LC15/P15)**
  - **44-Lead-QUAD (TMS320E15/E15-25)**



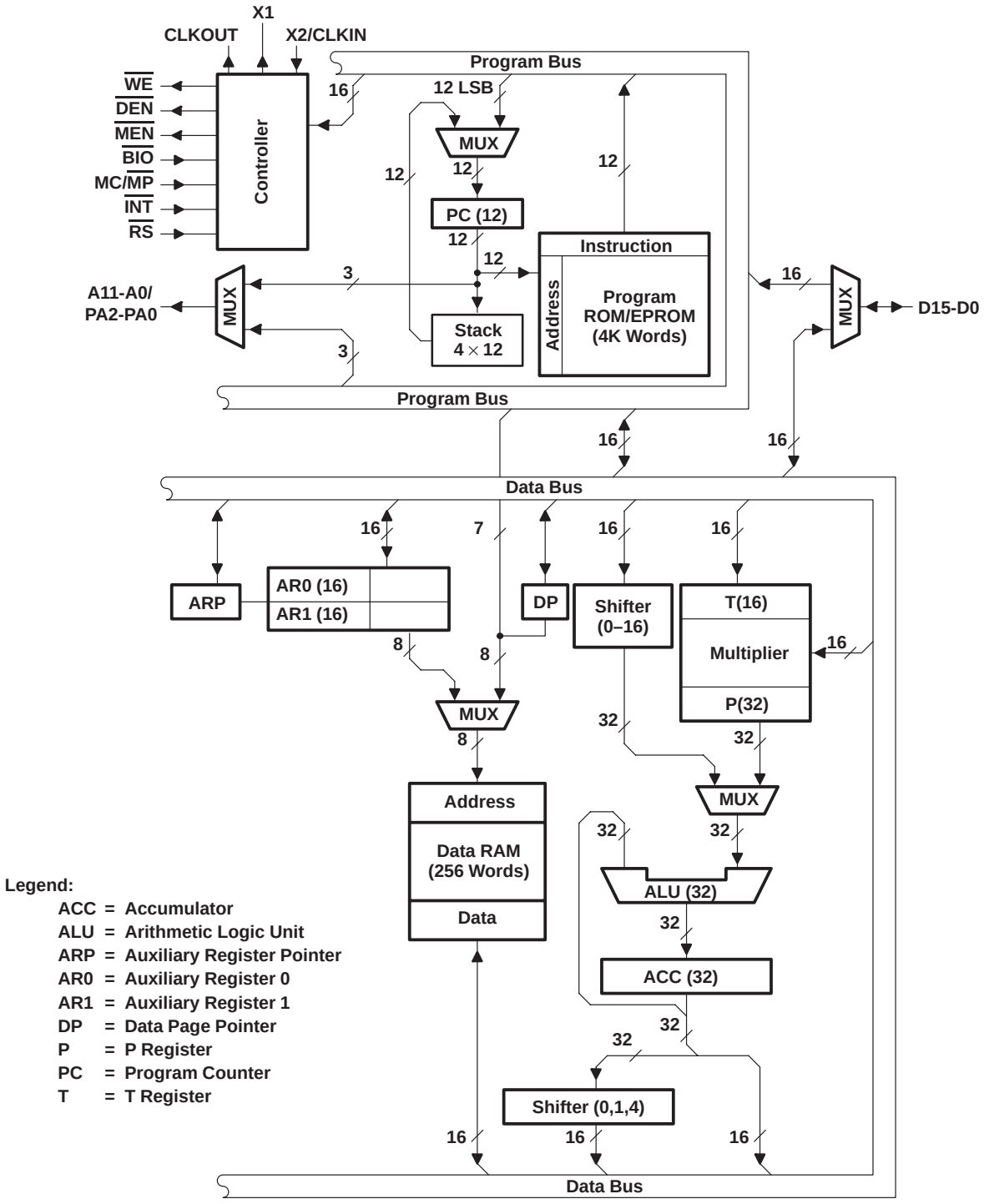
TMS320C15/E15/LC15/P15
N/JD Package
(Top View)



TMS320C15/E15/LC15/P15
FN/FZ Package
(Top View)



functional block diagram



Legend:

ACC	=	Accumulator
ALU	=	Arithmetic Logic Unit
ARP	=	Auxiliary Register Pointer
AR0	=	Auxiliary Register 0
AR1	=	Auxiliary Register 1
DP	=	Data Page Pointer
P	=	P Register
PC	=	Program Counter
T	=	T Register

TERMINAL FUNCTIONS (TMS320C15/E15/LC15/P15)†

NAME	I/O‡	DEFINITION
A11-A0/PA2-PA0	O	External address bus. I/O port address multiplexed over PA2-PA0.
$\overline{\text{BIO}}$	I	External polling input
CLKOUT	O	System clock output, 1/4 crystal/CLKIN frequency
D15-D0	I/O	16-bit parallel data bus
$\overline{\text{DEN}}$	O	Data enable for device input data on D15-D0
$\overline{\text{INT}}$	I	External interrupt input
MC/$\overline{\text{MP}}$	I	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
$\overline{\text{MEN}}$	O	Memory enable indicates that D15-D0 will accept external memory instruction.
NC	O	No connection
$\overline{\text{RS}}$	I	Reset for initializing the device
V_{CC}	I	+ 5 V supply
V_{SS}	I	Ground
$\overline{\text{WE}}$	O	Write enable for device output data on D15-D0
X1	O	Crystal output for internal oscillator
X2/CLKIN	I	Crystal input internal oscillator or external system clock input

† See EPROM programming section.
‡ Input/Output/High-impedance state.

electrical specifications

This section contains the electrical specifications for the ′C15/E15/P15 digital signal processors, including test parameter measurement information. Parameters with $_{PP}$ subscripts apply only to the ′E15/P15 in the EPROM programming mode (see Note 11).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 6) . . . . . –0.3 V to 7 V
Supply voltage range, V_{PP} . . . . . –0.6 V to 14 V
Input voltage range . . . . . –0.3 V to 14 V
Output voltage range . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . 0.5 mW
Operating free-air temperature: L suffix . . . . . 0°C to 70°C
A suffix . . . . . – 40°C to 85°C
Storage temperature . . . . . –55 °C to 150 °C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	EPROM devices	4.75	5	5.25	V
		All other devices	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 11)		12.25	12.5	12.75	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN	3			V
		All remaining inputs	2			V
V_{IL}	Low-level input voltage	MC/$\overline{MP}$			0.6	V
		All remaining inputs			0.8	V
I_{OH}	High-level output current, all outputs				– 300	μA
I_{OL}	Low-level output current (All outputs except for TMS320LC15)				2	mA
T_A	Operating free-air temperature	L suffix	0		70	°C
		A suffix	– 40		85	°C

NOTE 11: V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 μA (see Note 8)		V_{CC} – 0.4			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{OZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	μA
				V_O = 0.4 V			–20	
I_I	Input current		V_I = V_{SS} to V_{CC}	All inputs except CLKIN			±20	μA
				CLKIN			±50	
I_{CC}‡	Supply current	TMS320C15	f = 20.5 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C			45	55	mA
		TMS320C15-25	f = 25.6 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C			50	65	
		TMS320E15	f = 20.5 MHz, V_{CC} = 5.25 V, T_A = – 40°C to 85°C			55	75	
		TMS320E15-25	f = 25.6 MHz, V_{CC} = 5.25 V, T_A = 0°C to 70°C			65	85	
C_i	Input capacitance	Data bus	f = 1 MHz, all other pins 0 V			25‡		pF
		All other				15‡		
C_o	Output capacitance	Data bus				25‡		pF
		All others				10‡		

† All typical values are at V_{CC} = 5 V, T_A = 70°C and are used for thermal resistance calculations.
‡ I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependence on temperature, frequency, and loading, see Figure 3.
NOTE 7: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C15/E15/P15 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and should be specified at a load capacitance of 20 pF.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_X	TMS320C15	T_A = 0°C to 70°C	6.7		20.5	MHz
	TMS320E15/P15	T_A = – 40°C to 85°C	6.7		20.5	
	TMS320C15-25/E15-25	T_A = 0°C to 70°C	6.7		25.6	
C1, C2		T_A = 0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(C)}$	CLKOUT cycle time‡	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	195.12	200		156.25	160		ns
$t_{r(C)}$	CLKOUT rise time			10†			10†		ns
$t_{f(C)}$	CLKOUT fall time			8†			8†		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92†			72†		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90†			70†		ns
$t_{d(MCC)}$	Delay time, CLKIN↑ to CLKOUT↓		25†		60†	25†		50†	ns

† Values derived from characterization data and not tested.
‡ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).

timing requirements over recommended operating conditions

		TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	39.06	40	150	ns
$t_{r(MC)}$	Rise time, master clock input		5†	10†		5†	10†	ns
$t_{f(MC)}$	Fall time, master clock input		5†	10†		5†	10†	ns
$t_{w(MCP)}$†	Pulse duration, master clock	$0.4t_{c(MC)}$		$0.6t_{c(MC)}$†	$0.45t_{c(MC)}$		$0.55t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration, master clock low		20†			15†		ns
$t_{w(MCH)}$	Pulse duration, master clock high		20†			15†		ns

† Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_{d1}	Delay time, CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	10†		50	10‡		40	ns
t_{d2}	Delay time, CLKOUT↓ to $\overline{MEN}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)}+15$	$1/4t_{c(C)} - 5$†		$1/4t_{c(C)}+12$	ns
t_{d3}	Delay time, CLKOUT↓ to $\overline{MEN}$↑		–10†		15	–10†		12	ns
t_{d4}	Delay time, CLKOUT↓ to $\overline{DEN}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)}+15$	$1/4t_{c(C)} - 5$†		$1/4t_{c(C)}+12$	ns
t_{d5}	Delay time, CLKOUT↓ to $\overline{DEN}$↑		–10†		15	–10†		12	ns
t_{d6}	Delay time, CLKOUT↓ to $\overline{WE}$↓		$1/2t_{c(C)} - 5$†		$1/2t_{c(C)}+15$	$1/2t_{c(C)} - 5$†		$1/2t_{c(C)}+12$	ns
t_{d7}	Delay time, CLKOUT↓ to $\overline{WE}$↑		–10†		15	–10†		12	ns
t_{d8}	Delay time, CLKOUT↓ to data bus OUT valid				$1/4t_{c(C)}+65$			$1/4t_{c(C)}+52$	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$1/4t_{c(C)} - 5$†			$1/4t_{c(C)} - 5$†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven (TMS320C15/C15-25 only)				$1/4t_{c(C)} + 40$†			$1/4t_{c(C)} + 40$†	ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven (TMS320E15/E15-25 only)				$1/4t_{c(C)} + 70$†			$1/4t_{c(C)} + 70$†	ns
t_v	Data bus OUT valid after CLKOUT↓		$1/4t_{c(C)} - 10$			$1/4t_{c(C)} - 10$			ns
$t_{h(A-WMD)}$	Address hold time after $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 15)		0†		2†	0†		2†	ns
$t_{su(A-MD)}$	Address bus setup time prior to $\overline{DEN}$↓		$1/4t_{c(C)} - 45$			$1/4t_{c(C)} - 35$			ns

† Values derived from characterization data and not tested.
NOTE 14: Address bus will be valid upon $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑.

timing requirements over recommended operating conditions

		TEST CONDITIONS	TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(D)}$	Setup time, data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	50			40			ns
$t_{h(D)}$	Hold time, data bus held valid after CLKOUT↓ (see Note 9)		0			0			ns

NOTE 9: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time, $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF (see Figure 2)			$1/2t_{c(C)} + 50^\dagger$	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$1/4t_{c(C)} + 50^\dagger$	ns

† Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 10)	50			40			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			$5t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(INT)}$	Fall time, $\overline{INT}$			15			15	ns
$t_{w(INT)}$	Pulse duration, $\overline{INT}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time, $\overline{INT}\downarrow$ before CLKOUT$\downarrow$	50			40			ns

IO ($\overline{BIO}$) TIMING

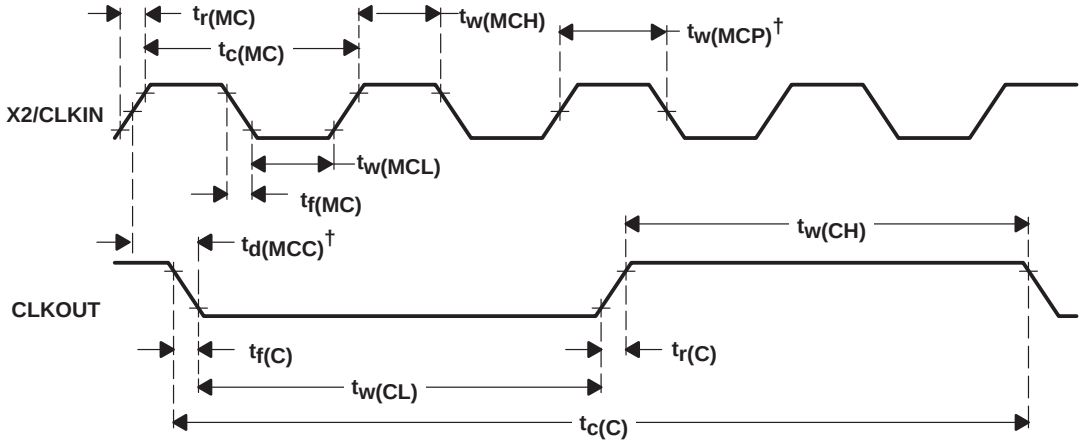
timing requirements over recommended operating conditions

		TMS320C15/E15/P15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(IO)}$	Fall time, $\overline{BIO}$			15			15	ns
$t_{w(IO)}$	Pulse duration, $\overline{BIO}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time, $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	50			40			ns

TIMING DIAGRAMS

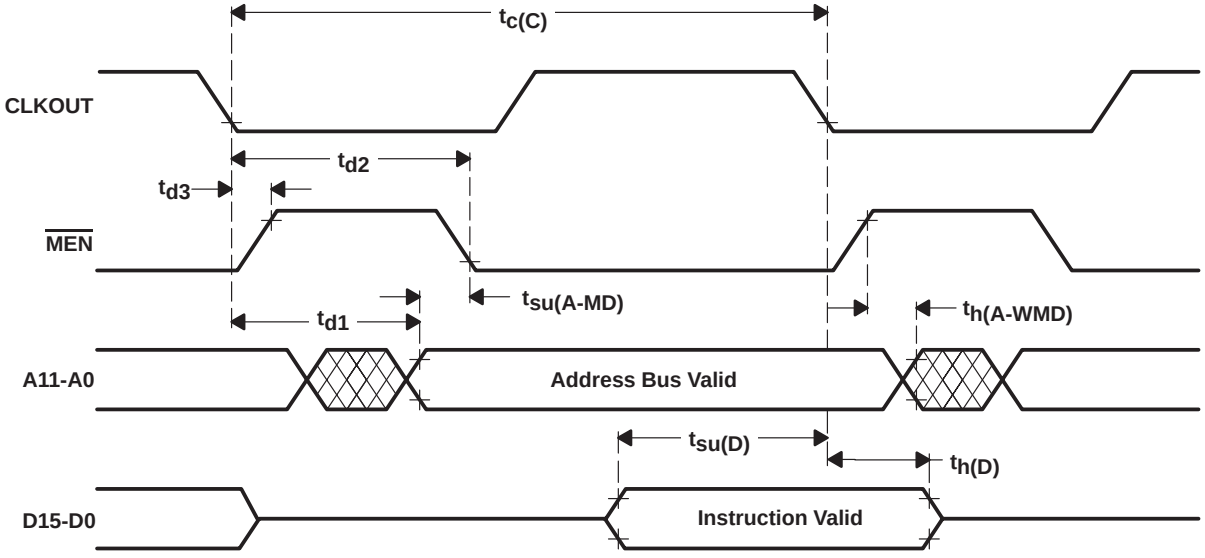
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

clock timing

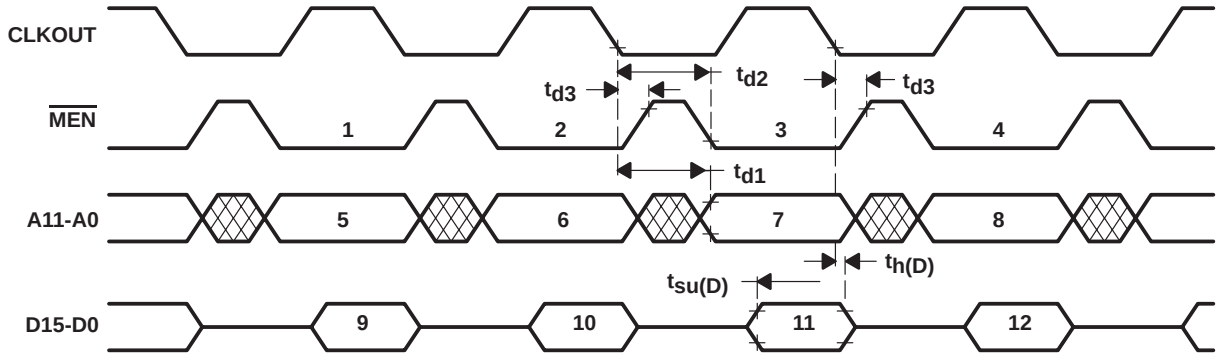


† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

memory read timing



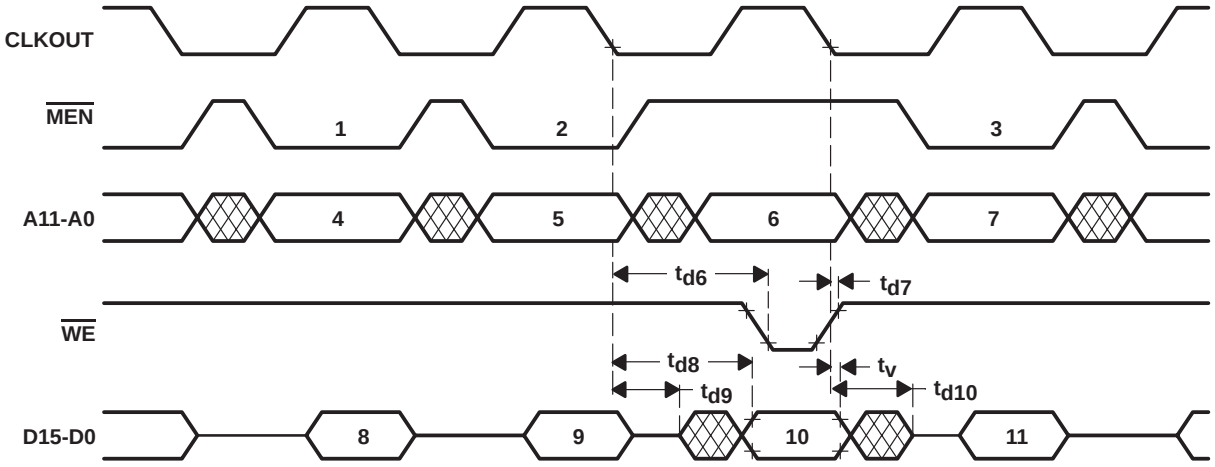
TBLR instruction timing



Legend:

1. TBLR Instruction Prefetch
2. Dummy Prefetch
3. Data Fetch
4. Next Instruction Prefetch
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Address Bus Valid
9. Instruction Valid
10. Instruction Valid
11. Data Input Valid
12. Instruction Valid

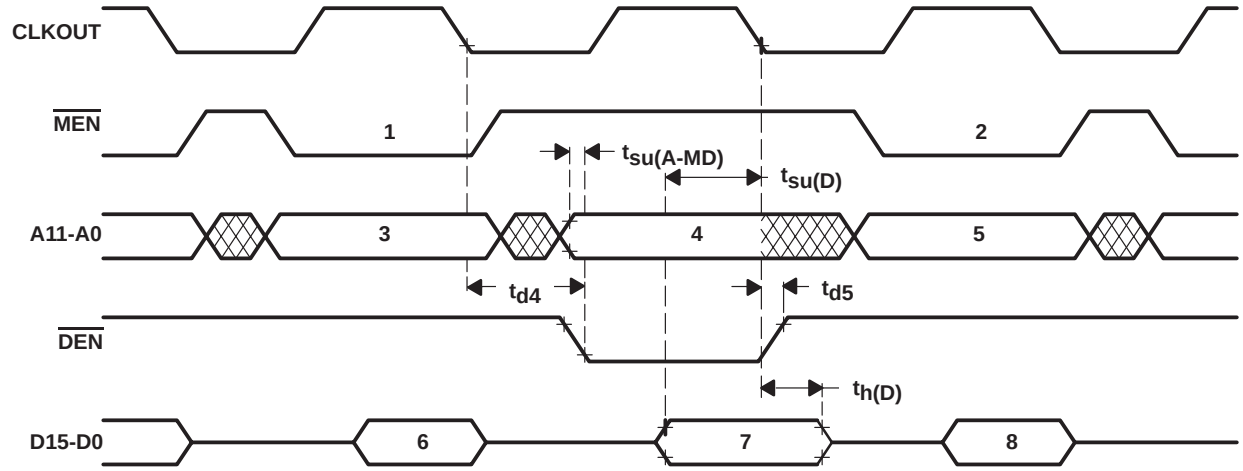
TBLW instruction timing



Legend:

1. TBLW Instruction Prefetch
2. Dummy Prefetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Instruction Valid
9. Instruction Valid
10. Data Output Valid
11. Instruction Valid

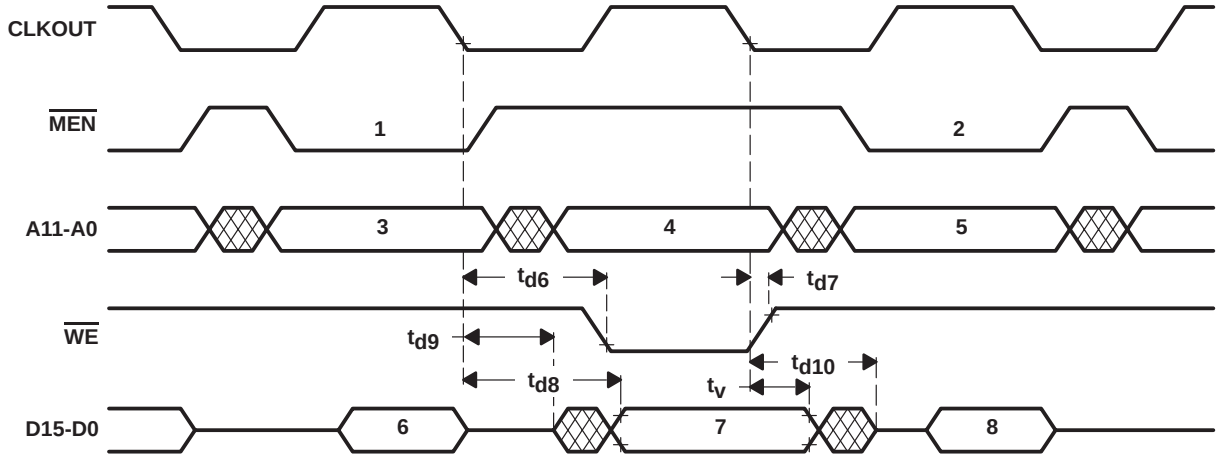
IN instruction timing



Legend:

1. IN Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Input Valid
8. Instruction Valid

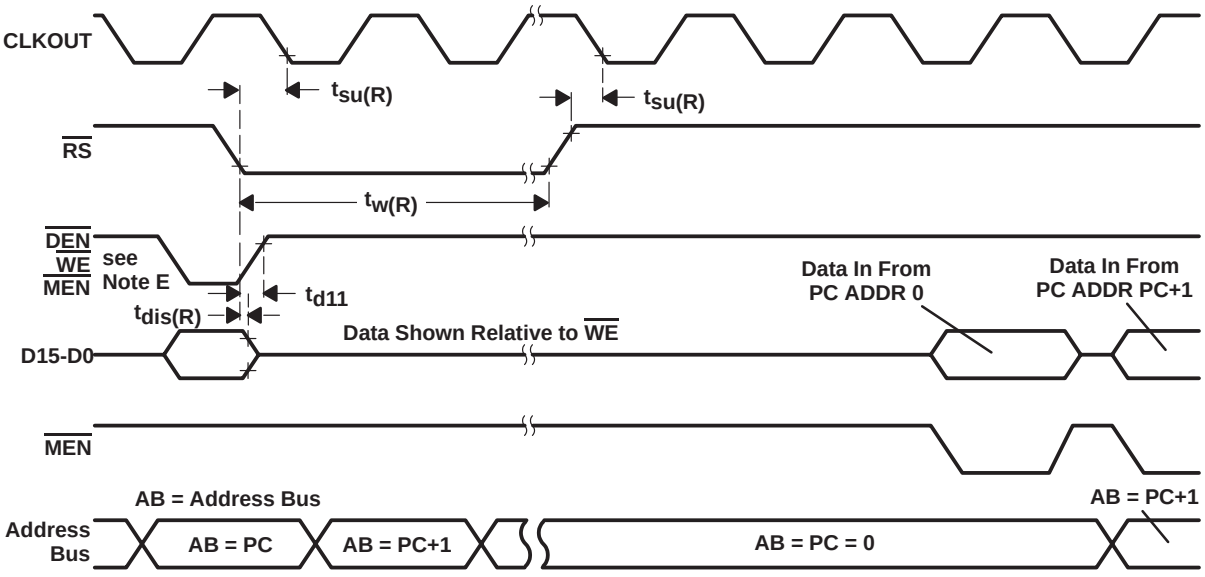
OUT instruction timing



Legend:

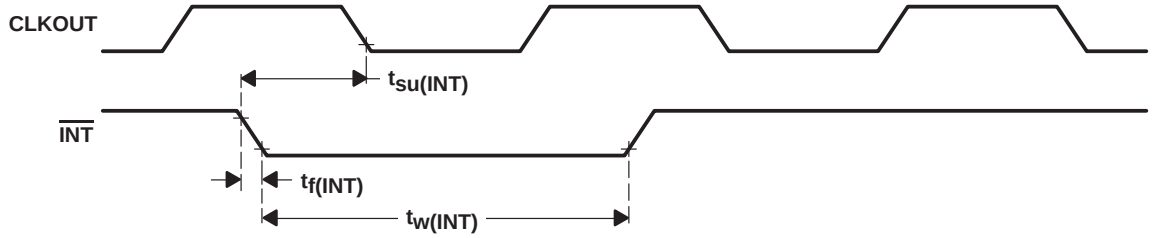
1. IN Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Output Valid
8. Instruction Input Valid

reset timing

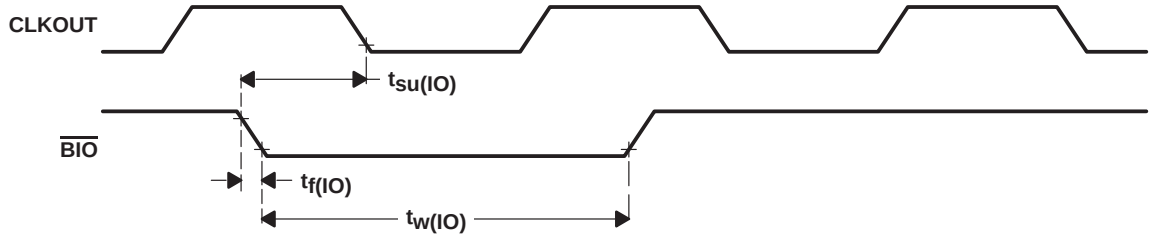


NOTES: A. RS forces DEN, WE, and MEN high and places data bus D0 through D15 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from RS↓.
B. RS must be maintained for a minimum of five clock cycles.
C. Resumption of normal program will commence after one complete CLK cycle from RS↑.
D. Due to the synchronization action on RS, time to execute the function can vary dependent upon when RS↑ or RS↓ occur in the CLK cycle.
E. Diagram shown is for definition purpose only. DEN, WE, and MEN are mutually exclusive.
F. During a write cycle, RS may produce an invalid write address.

interrupt timing



BIO timing



absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{PP} (see Note 6) . . . . . –0.6 V to 14 V

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{PP}	Supply voltage (see Note 11)	12.25	12.5	12.75	V

NOTE 11: V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{PP1}	V_{PP} supply current	$V_{PP} = V_{CC}$ 5.5 V			100	V
I_{PP2}	V_{PP} supply current (during program pulse)	V_{PP} = 12.75 V		30	50	V

‡ All typical values except for I_{CC} are at V_{CC} = 5 V, T_A = 25°C.

recommended timing requirements for programming, T_A = 25°C, V_{CC} = 6, V_{PP} = 12.5 V, (see Note 13)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	3.8		63	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$ (see Note 15)	0		130§	ns
$t_{en(G)}$	Output enable time from $\overline{G}$	0		150§	ns
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

§ Values derived from characterization data and not tested.

NOTES: 13. For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V and V_{PP} = 12.5 V ± 0.5 V during programming.

15. Common test conditions apply for $t_{dis(G)}$ except during programming.

PROGRAMMING THE TMS320E15/P15 EPROM CELL

′E15/P15 devices include a 4K × 16-bit industry-standard EPROM cell for prototyping, early field testing, and low-volume production. In conjunction with this EPROM, the ′E15/P15 with a 4K-word masked ROM, then, provide more migration paths for cost-effective production.

EPROM adapter sockets are available that provide pin-to-pin conversions for programming any ′E15/P15 devices. One adapter socket (part number RTC/PGM320C-06), shown in Figure 8, converts a 40-pin DIP device into an equivalent 28-pin device. Another socket (part number RTC/PGM320A-06), not shown, permits 44- to 28-pin conversion.

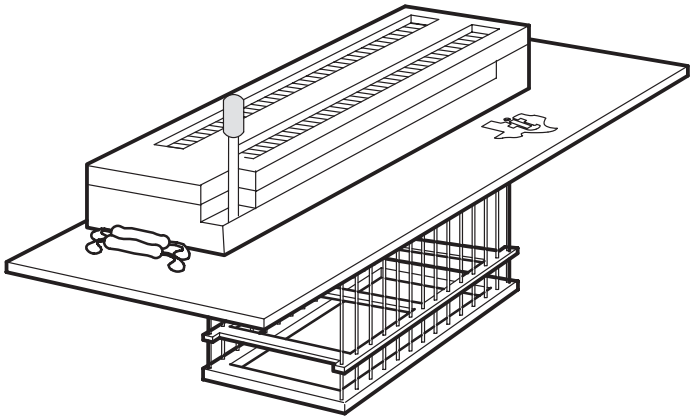
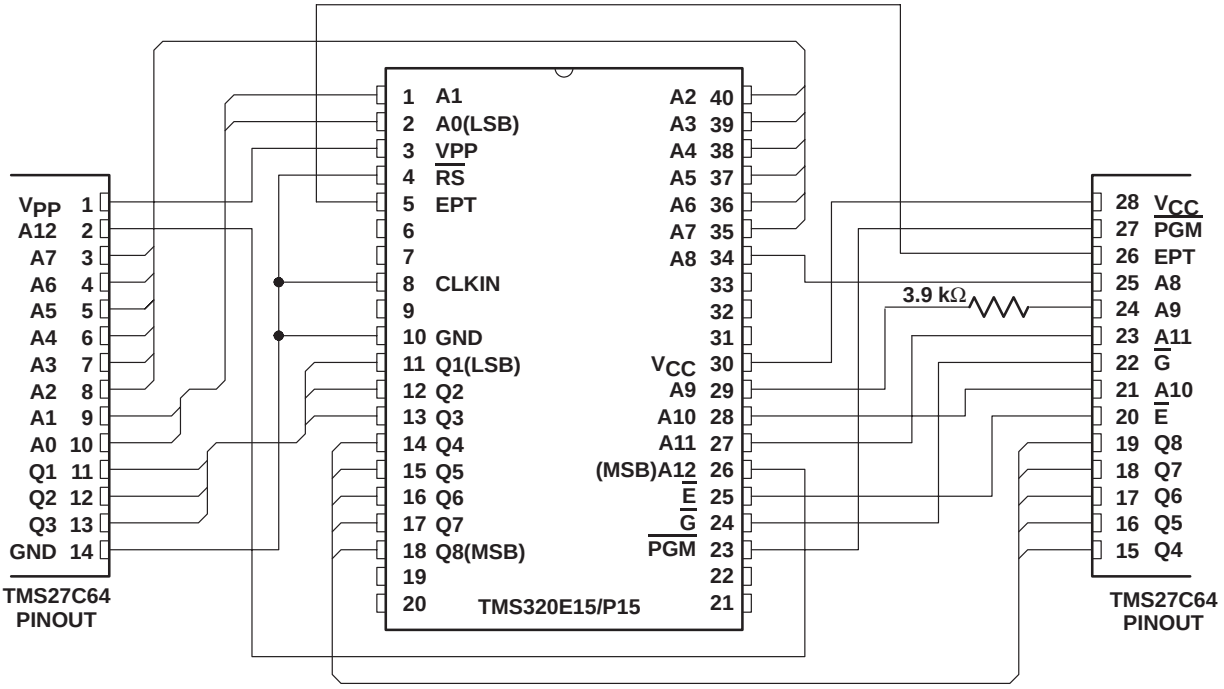


Figure 8. EPROM Adapter Socket (40-pin to 28-pin DIP Conversion)

Key features of the EPROM cell include the normal programming operation as well as verification. The EPROM cell also includes a code protection feature that allows code to be protected against copyright violations.

The ′E15/P15 EPROM cell is programmed using the same family and device pinout codes as the TMS27C64 8K × 8-bit EPROM. The TMS27C64 EPROM series are unltraviolet-light erasable, electrically programmable, read-only memories, fabricated using HVCMOS technology. They are pin-compatible with existing 28-pin ROMs and EPROMs. These EPROMs operate from a single 5-V supply in the read mode; however, a 12.5-V supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

Figure 9 shows the wiring conversion to program the ′E15/P15 using the 28-pin pinout of the TMS27C64. Table 5 on pin nomenclature provides a description of the TMS27C64 pins. The code to be programmed into the device should be in serial mode. The ′E15/P15 devices use 13 address lines to address 4K-word memory in byte format.



CAUTION

Although acceptable by some EPROM programmers, the signature mode cannot be used on any ′E1x device. The signature mode will input a high-level voltage (12.5 V_{dc}) onto pin A9. Since this pin is not designed for high voltage, the cell will be damaged. To prevent an accidental application of voltage, Texas Instruments has inserted a 3.9 kΩ resistor between pin A9 of the TI programmer socket and the programmer itself.

Pin Nomenclature (TMS320E15/P15)

NAME	I/O	DEFINITION
A0-A12	I	On-chip EPROM programming address lines
CLKIN	I	Clock oscillator input
$\overline{E}$	I	EPROM chip select
EPT	I	EPROM test mode select
$\overline{G}$	I	EPROM read/verify select
GND	I	Ground
$\overline{PGM}$	I	EPROM write/program select
Q1-Q8	I/O	Data lines for byte-wide programming of on-chip 8K bytes of EPROM
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	5-V power supply
V_{PP}	I	12.5-V power supply

Figure 9. TMS320E15/P15 EPROM Programming Conversion to TMS27C64 EPROM Pinout

Table 5 shows the programming levels required for programming, verifying, reading, and protecting the EPROM cell.

Table 5. TMS320E15/P15 Programming Mode Levels

SIGNAL NAME	TMS320E15 PIN	TMS27C64 PIN	PROGRAM	VERIFY	READ	PROTECT VERIFY	EPROM PROTECT
$\overline{E}$	25	20	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$	24	22	V_{IH}	$\overline{PULSE}$	$\overline{PULSE}$	V_{IL}	V_{IH}
$\overline{PGM}$	23	27	$\overline{PULSE}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}
V_{PP}	3	1	V_{PP}	V_{PP}	V_{CC}	V_{CC} + 1	V_{PP}
V_{CC}	30	28	V_{CC}	V_{CC}	V_{CC}	V_{CC} + 1	V_{CC} + 1
V_{SS}	10	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
CLKIN	8	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
$\overline{RS}$	4	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
EPT	5	26	V_{SS}	V_{SS}	V_{SS}	V_{PP}	V_{PP}
Q1-Q8	11-18	11-13, 15-19	D_{IN}	Q_{OUT}	Q_{OUT}	Q8=RBIT	Q8=$\overline{PULSE}$
A0-A3	2, 1, 40, 39	10-7	ADDR	ADDR	ADDR	X	X
A4	38	6	ADDR	ADDR	ADDR	X	V_{IH}
A5	37	5	ADDR	ADDR	ADDR	X	X
A6	36	4	ADDR	ADDR	ADDR	V_{IL}	X
A7-A9	35, 34, 29	3, 25, 24	ADDR	ADDR	ADDR	X	X
A10-A12	28-26	21, 23, 2	ADDR	ADDR	ADDR	X	X

Legend:

V_{IH} = TTL high level; V_{IL} = TTL low level; ADDR = byte address bit
V_{PP} = 12.5 V ± 0.25 V; V_{CC} = 5 V ± 0.25 V; X = don't care
$\overline{PULSE}$ = low-going TTL level pulse; D_{IN} = byte to be programmed at ADDR
Q_{OUT} = byte stored at ADDR; RBIT = ROM protect bit.

programming

Since every memory bit in the cell is a logic 1, the programming operation reprograms certain bits to 0. Once programmed, these bits can only be erased using ultraviolet light. The correct byte is placed on the data bus with V_{PP} set to the 12.5 V level. The $\overline{PGM}$ pin is then pulsed low to program in the zeros.

erasure

Before programming, the device must be erased by exposing it to ultraviolet light. The recommended minimum exposure dose (UV-intensity × exposure-time) is 15 W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After exposure, all bits are in the high state.

verify/read

To verify correct programming, the EPROM cell can be read using either the verify or read line definitions shown in Table 5, assuming the inhibit bit has not been programmed.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

read

The EPROM contents may be read independent of the programming cycle, provided the RBIT (ROM protect bit) has not been programmed. The read is accomplished by setting $\overline{E}$ to zero and pulsing $\overline{G}$ low. The contents of the EPROM location selected by the value on the address inputs appear on Q8-Q1.

output disable

During the EPROM programming process, the EPROM data outputs may be disabled, if desired, by establishing the output disable state. This state is selected by setting $\overline{G}$ and $\overline{E}$ pins high. While output disable is selected, Q8-Q1are placed in the high-impedance state.

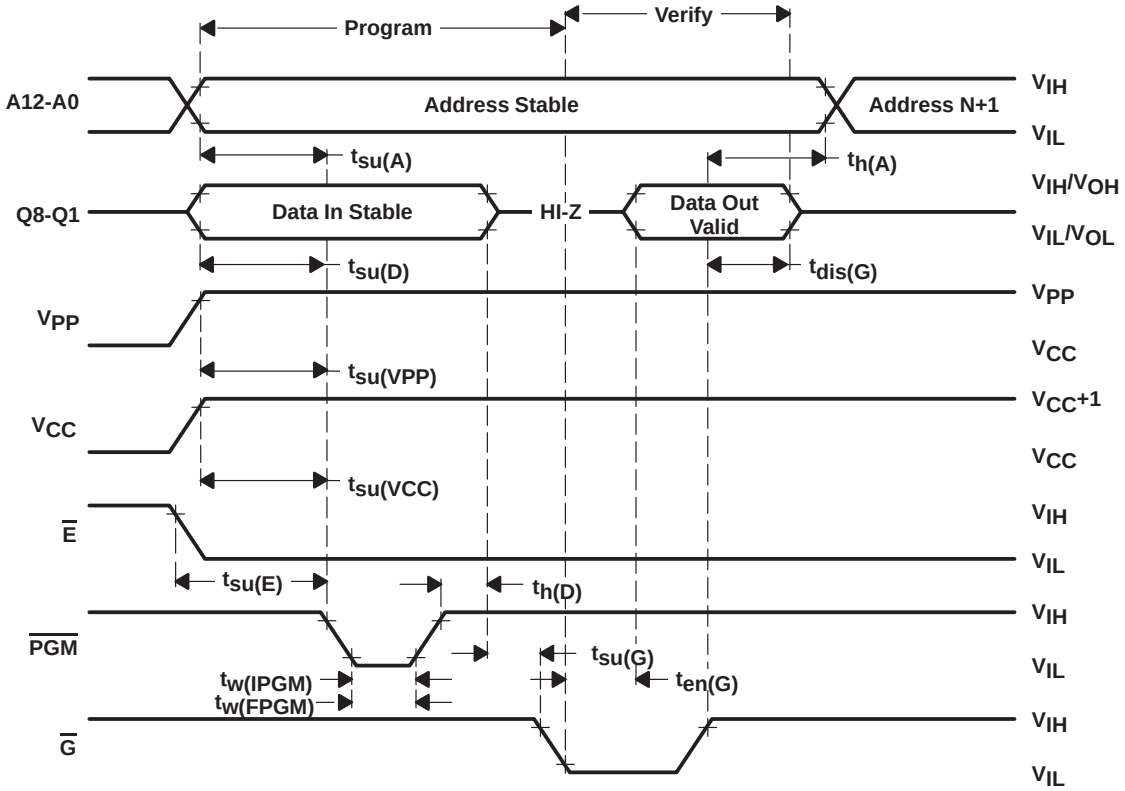
EPROM protection

To protect the proprietary algorithms existing in the code programmed on-chip, the ability to read or verify code from external accesses can be completely disabled. Programming the RBIT disables external access of the EPROM cell and disables the microprocessor mode, making it impossible to access the code resident in the EPROM cell. The only way to remove this protection is to erase the entire EPROM cell, thus removing the proprietary information. The signal requirements for programming this bit are shown in Table 5. The cell can be determined as protected by verifying the programming of the RBIT shown in the table.

standard programming procedure

Before programming, the device must first be completely erased. Then the device can be programmed with the correct code. It is advisable to program unused sections with zeroes as a further security measure. After the programming is complete, the code programmed into the cell should be verified. If the cell passes verification, the next step is to program the ROM protect bit (RBIT). Once the RBIT programming is verified, an opaque label should be placed over the window to protect the EPROM cell from inadvertent erasure by ambient light. At this point, the programming is complete, and the device is ready to be placed into its destination circuit.

program cycle timing



absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 6) . . . . . –0.3 V to 4.6 V
Input voltage range . . . . . –0.3 V to V_{CC} + 0.5
Output voltage range . . . . . –0.3 V to V_{CC} + 0.5
Continuous power dissipation . . . . . 75 mW
Air temperature range above operating devices: L version . . . . . 0°C to 70°C
A version . . . . . –40°C to 85°C
Storage temperature range . . . . . –55°C to +150°C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2.0			V
		CLKIN	2.5			V
V_{IL}	Low-level input voltage	All inputs			0.55	V
I_{OH}	High-level output current (all outputs)				–300	µA
I_{OL}	Low-level output current (all outputs)				1.5	mA
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C

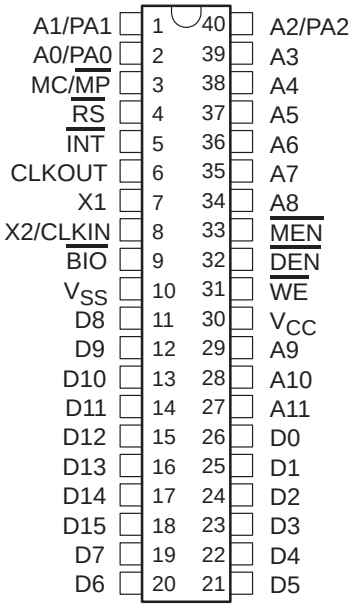
electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.0			V
			I_{OH} = 20 µA (see Note 7)		V_{CC} – 0.4‡			V
V_{OL}	Low-level output voltage		I_{OL} = MAX				0.5	V
I_{OZ}	Off-state ouput current		V_{CC} = MAX, $V_O = V_{CC}$				20	µA
			$V_O = V_{SS}$				–20	
I_I	Input current		$V_I = V_{SS}$ to V_{CC}	All inputs except CLKIN			±20	µA
			$V_I = V_{SS}$ to V_{CC}	CLKIN			±50	
C_i	Input capacitance	Data bus	f = 1 MHz, All other pins 0 V			25‡		pF
		All others				15‡		
C_o	Output capacitance	Data bus				25‡		pF
		All others				10‡		

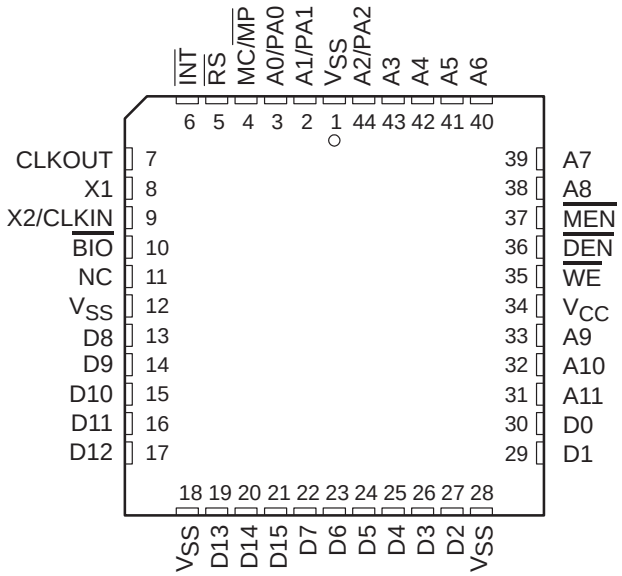
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Values derived from characterization data and not tested.

NOTE 7: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

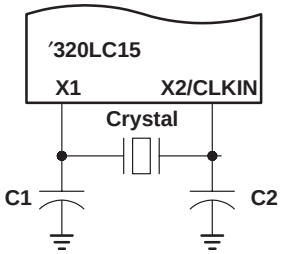
N Package
(Top View)



FN Package
(Top View)



INTERNAL CLOCK OPTION



PARAMETER MEASUREMENT INFORMATION

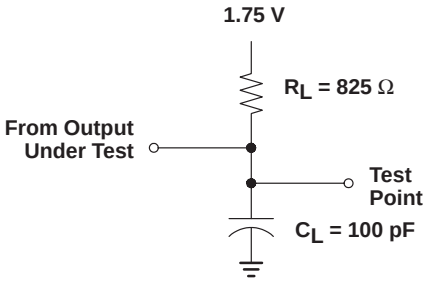


Figure 10. Test Load Circuit

CLOCK CHARACTERISTICS AND TIMING

The ′LC15 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency f_X	T_A = – 40°C to 85°C	4.0		16	MHz
C1, C2			10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	250		1000	ns
$t_{r(C)}$	CLKOUT rise time			10‡		ns
$t_{f(C)}$	CLKOUT fall time			8‡		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			117‡		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			115‡		ns
$t_{d(MCC)}$	Delay time, CLKIN↑ to CLKOUT↓		20		70	ns

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	62.5		150	ns
$t_{r(MC)}$	Rise time, master clock input		5‡	10†	ns
$t_{f(MC)}$	Fall time, master clock input		5‡	10†	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.4t_{c(MC)}$‡		$0.6t_{c(MC)}$‡	ns
$t_{w(MCL)}$	Pulse duration, master clock low at $t_{c(MC)}$ min		26		ns
$t_{w(MCH)}$	Pulse duration, master clock high at $t_{c(MC)}$ min		26		ns

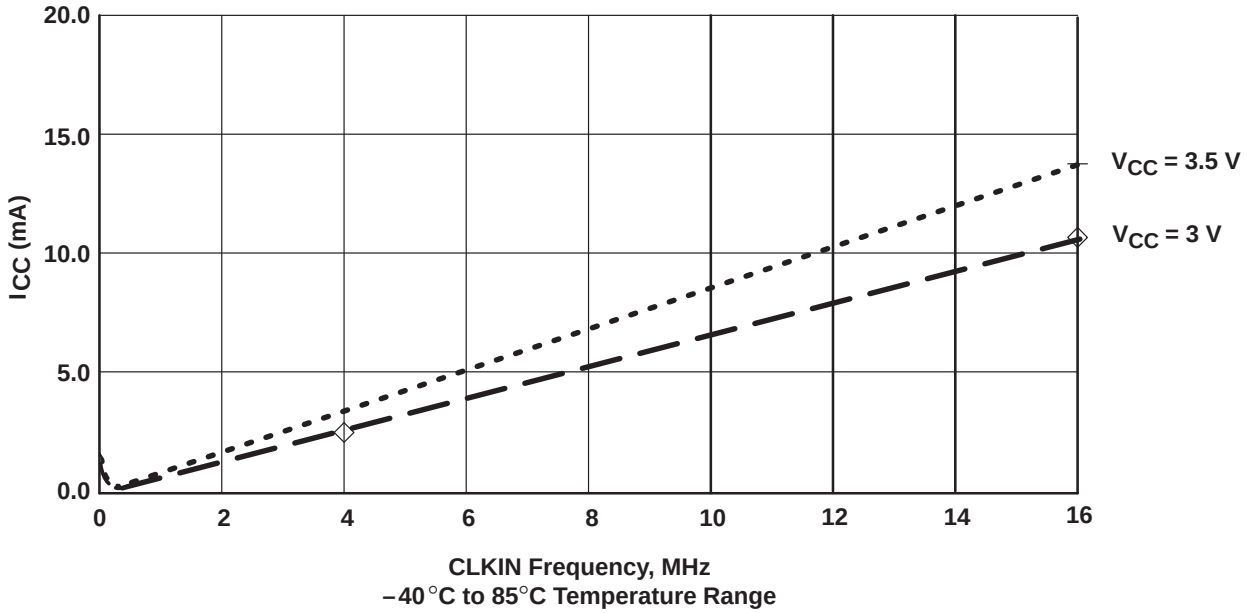
† $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used)
‡ Values derived from characterization data and not tested.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡	f = 16.0 MHz, V_{CC} = 3.6 V, T_A = 0°C to 70°C		15	20	mA

† All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡ I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependence on frequency, see figure below.

typical power vs. frequency graph (outputs unloaded)§



§ Device operation is not guaranteed below 4 MHz CLKIN.
Graph is for device in RESET; i.e., only clock-out is driven.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825Ω, C_L = 100 pF, (see Figure 2)	10†	75	ns
t_{d2}	Delay time CLKOUT↓ to $\overline{MEN}$↓		1/4 $t_{c(C)}$–5†	1/4 $t_{c(C)}$+25	ns
t_{d3}	Delay time CLKOUT↓ to $\overline{MEN}$↑		–10†	30	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		1/4 $t_{c(C)}$–5†	1/4 $t_{c(C)}$+25	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		–10†	30	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		1/2 $t_{c(C)}$–5†	1/2 $t_{c(C)}$+25	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		–10†	30	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid			1/4 $t_{c(C)}$+75	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		1/4 $t_{c(C)}$–5†		ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven			1/4 $t_{c(C)}$+60	ns
t_v	Data bus OUT valid after CLKOUT↓		1/4 $t_{c(C)}$–10		ns
$t_{h(A\text{-}WMD)}$	Address hold time after WE↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 14)		0†		ns
$t_{su(A\text{-}MD)}$	Address bus setup time to $\overline{DEN}$↓		– 4†		ns

† Values derived from characterization data and not tested.
NOTE 14: Address bus will be valid upon $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825Ω, C_L = 100 pF, (see Figure 2)	56			ns
$t_{h(D)}$	Hold time, data bus held valid after CLKOUT↓ (see Note 9)		0			ns

NOTE 9: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{d11}	Delay time, $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}$	R_L = 825Ω, C_L = 100 pF, (see Figure 2)			$1/2t_{c(C)}+75$	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$1/4t_{c(C)}+75$	ns

† These parameters do not apply to this device.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 10)	85			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

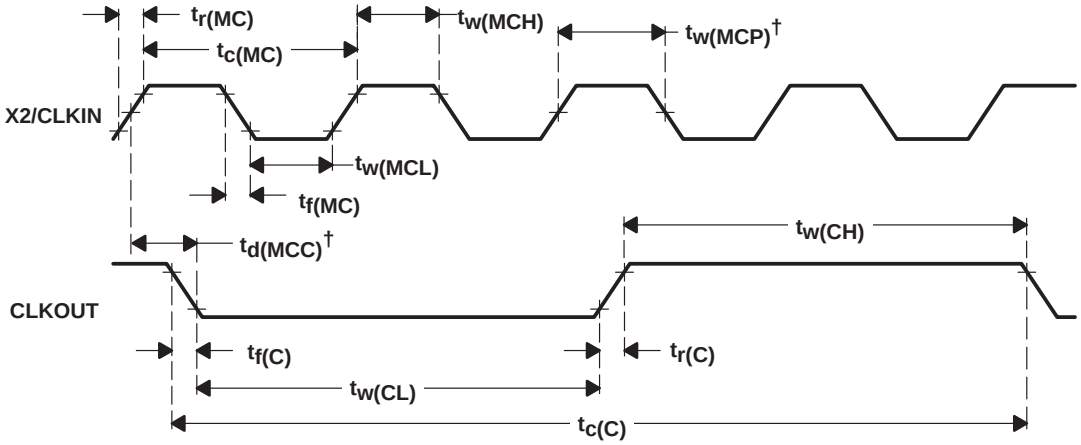
		MIN	NOM	MAX	UNIT
$t_{F(INT)}$	Fall time, $\overline{INT}$			15	ns
$t_{w(INT)}$	Pulse duration, $\overline{INT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time, $\overline{INT}\downarrow$ before CLKOUT$\downarrow$	85			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

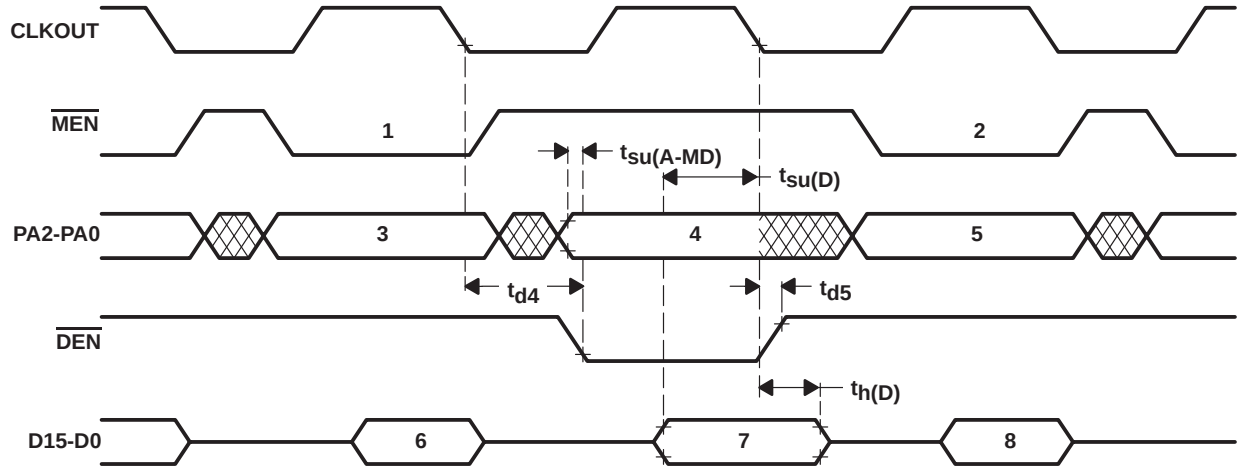
		MIN	NOM	MAX	UNIT
$t_{f(IO)}$	Fall time $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	85			ns

clock timing



† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

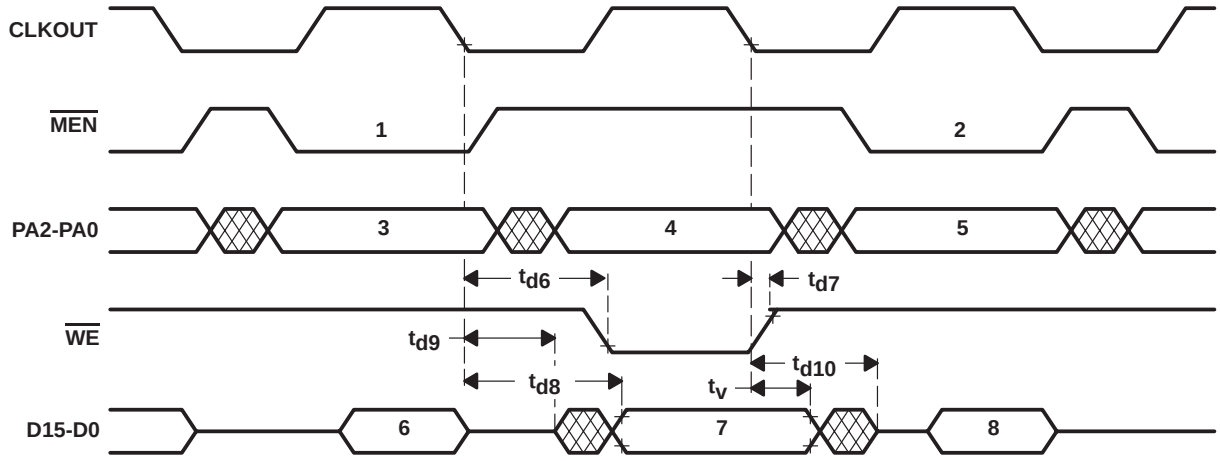
IN instruction timing



Legend:

1. IN Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Input Valid
8. Instruction Valid

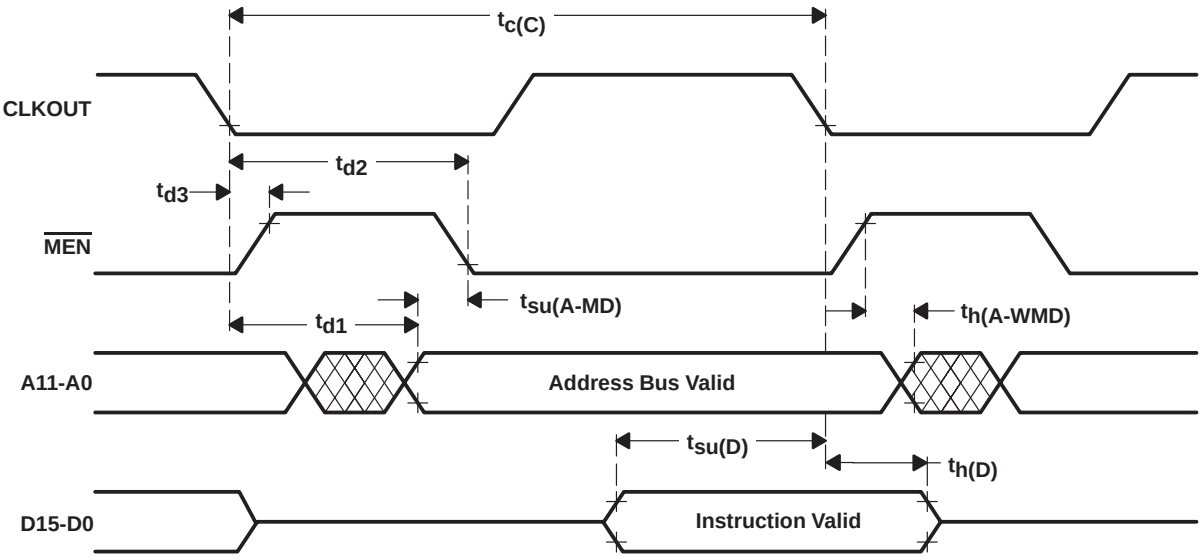
OUT instruction timing



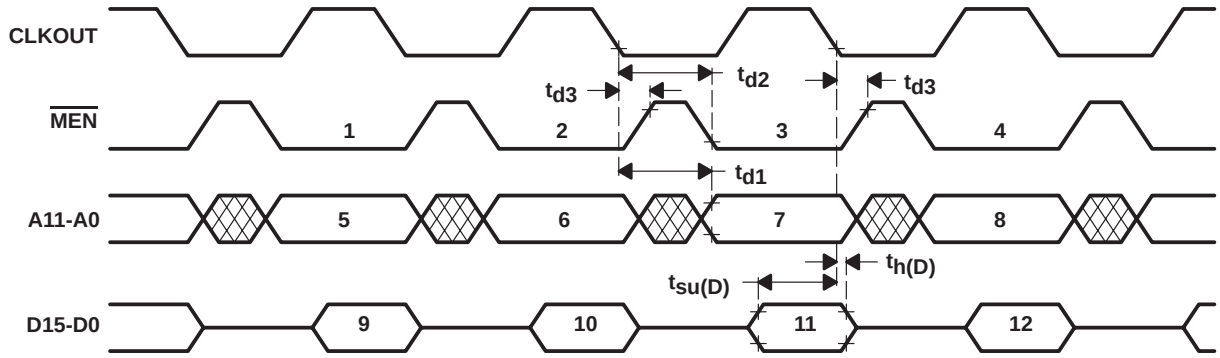
Legend:

1. OUT Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Output Valid
8. Instruction Valid

external memory read timing



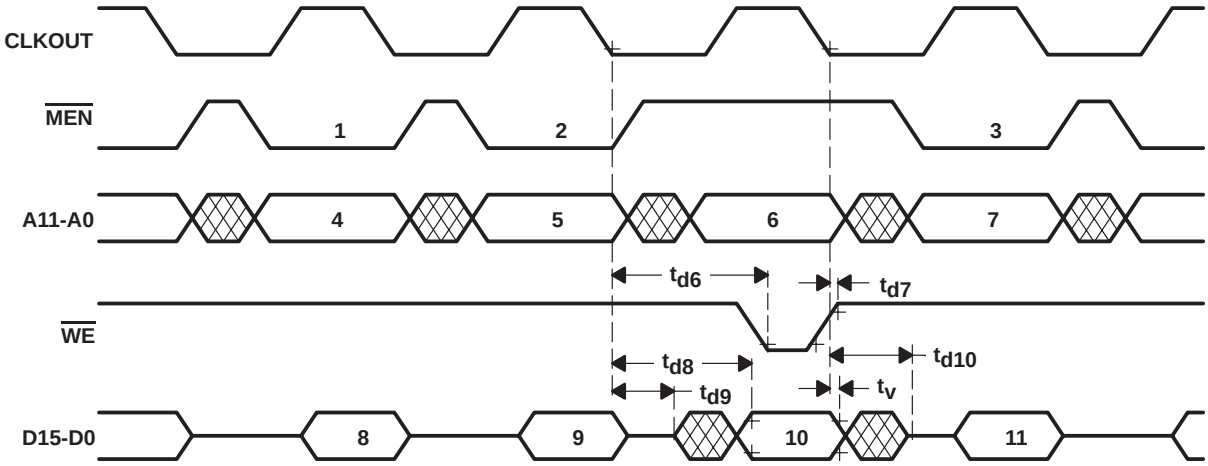
TBLR instruction timing



Legend:

1. TBLR Instruction Prefetch
2. Dummy Prefetch
3. Data Fetch
4. Next Instruction Prefetch
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Address Bus Valid
9. Instruction Valid
10. Instruction Valid
11. Data Input Valid
12. Instruction Valid

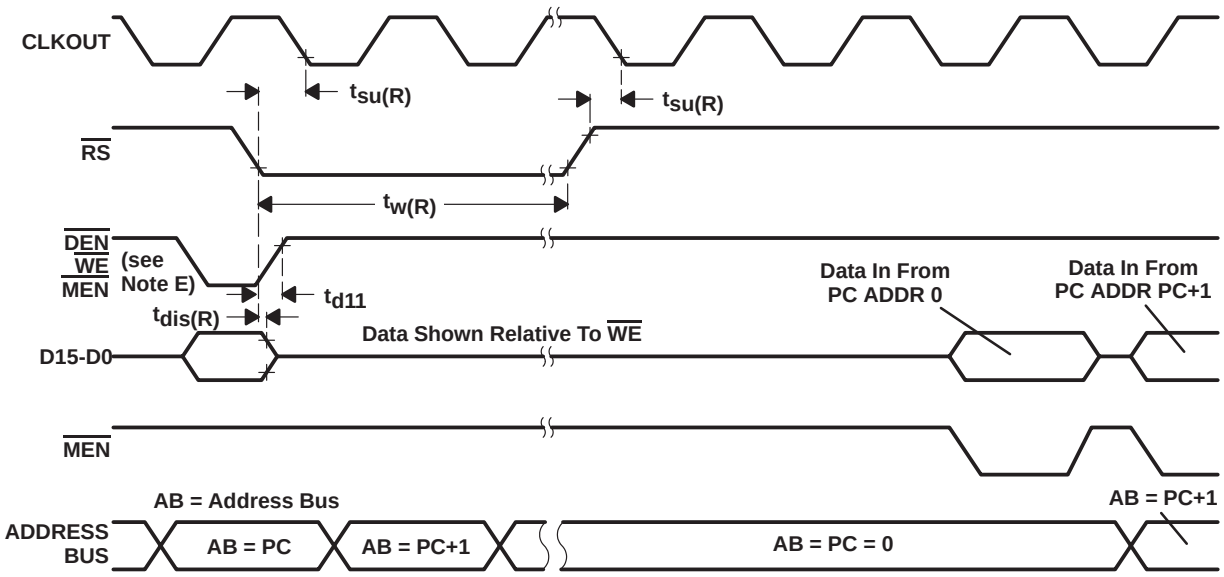
TBLW instruction timing



Legend:

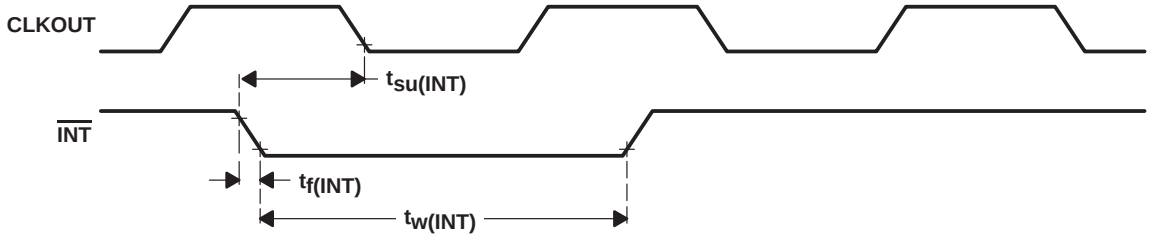
1. TBLW Instruction Prefetch
2. Dummy Prefetch
3. Next Instruction Prefetch
4. Address Bus Valid
5. Address Bus Valid
6. Address Bus Valid
7. Address Bus Valid
8. Instruction Valid
9. Instruction Valid
10. Data Output Valid
11. Instruction Valid

reset timing

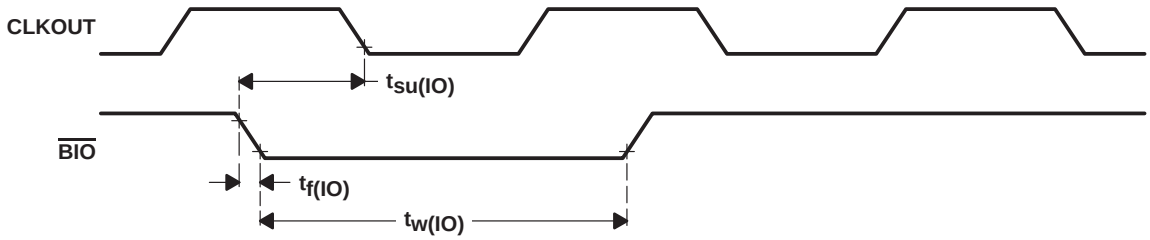


NOTES: A. RS forces DEN, WE, and MEN high and places data bus D0 through D15 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from RS↓.
B. RS must be maintained for a minimum of five clock cycles.
C. Resumption of normal program will commence after one complete CLK cycle from RS↑.
D. Due to the synchronization action on RS, time to execute the function can vary dependent upon when RS↑ or RS↓ occur in the CLK cycle.
E. Diagram shown is for definition purpose only. DEN, WE, and MEN are mutually exclusive.
F. During a write cycle, RS may produce an invalid write address.

interrupt timing

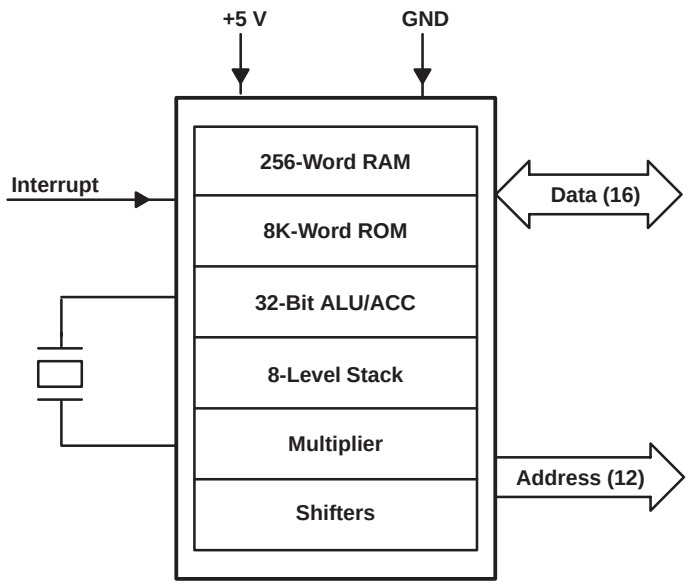


BIO timing

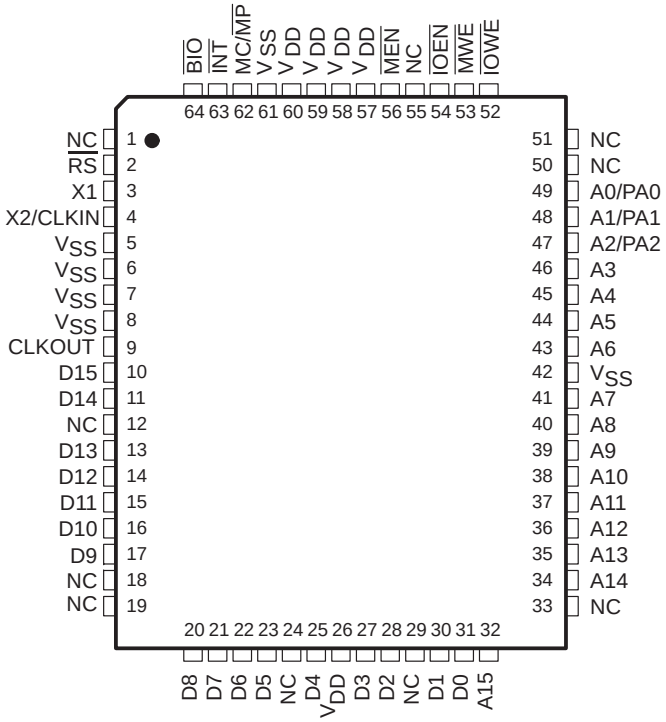


Key Features: TMS320C16

- 114-ns Instruction Cycle Time
- 256 Words of On-Chip Data RAM
- 8K Words of On-Chip Program ROM
- 64K Words Total External Memory at Full Speed
- 8 Level Stack
- 32-Bit ALU/Accumulator
- 16 × 16-Bit Multiplier With 32-Bit Product
- 16-Bit Barrel Shifter
- Eight Input and Eight Output Channels
- Simple Memory and I/O Interface:
  - Memory Write Enable Signal $\overline{\text{MWE}}$
  - I/O Write Enable Signal $\overline{\text{IOWE}}$
- Single 5-V Supply
- 64-Pin Quad Flatpack (PG Suffix)
- Operating Free-Air Temperature Range . . . 0°C to 70°C



PG Package
(Top View)



TERMINAL FUNCTIONS

PIN		I/O/Z†	DESCRIPTION
NAME	NO.		ADDRESS/DATA BUSES
A15 MSB	32	I/O/Z	Program memory address bus A15 (MSB) through A0 (LSB) and port addresses PA2 (MSB) through PA0 (LSB). Addresses A15 through A0 are always active and never go to high impedance. During execution of the IN and OUT instructions, pins A2 through A0 carry the port addresses. (Address pins A15 through A3 are always driven low on IN and OUT instruction.
A14	34		
A13	35		
A12	36		
A11	37		
A10	38		
A9	39		
A8	40		
A7	41		
A6	43		
A5	44		
A4	45		
A3	46		
A2/PA2	47		
A1/PA1	48		
A0/PA0	49		
D15 MSB	10	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The data bus is always in the high-impedance state except when $\overline{\text{IOWE}}$ or $\overline{\text{MWE}}$ are active (low).
D14	11		
D13	13		
D12	14		
D11	15		
D10	16		
D9	17		
D8	20		
D7	21		
D6	22		
D5	23		
D4	25		
D3	27		
D2	28		
D1	30		
D0 LSB	31		

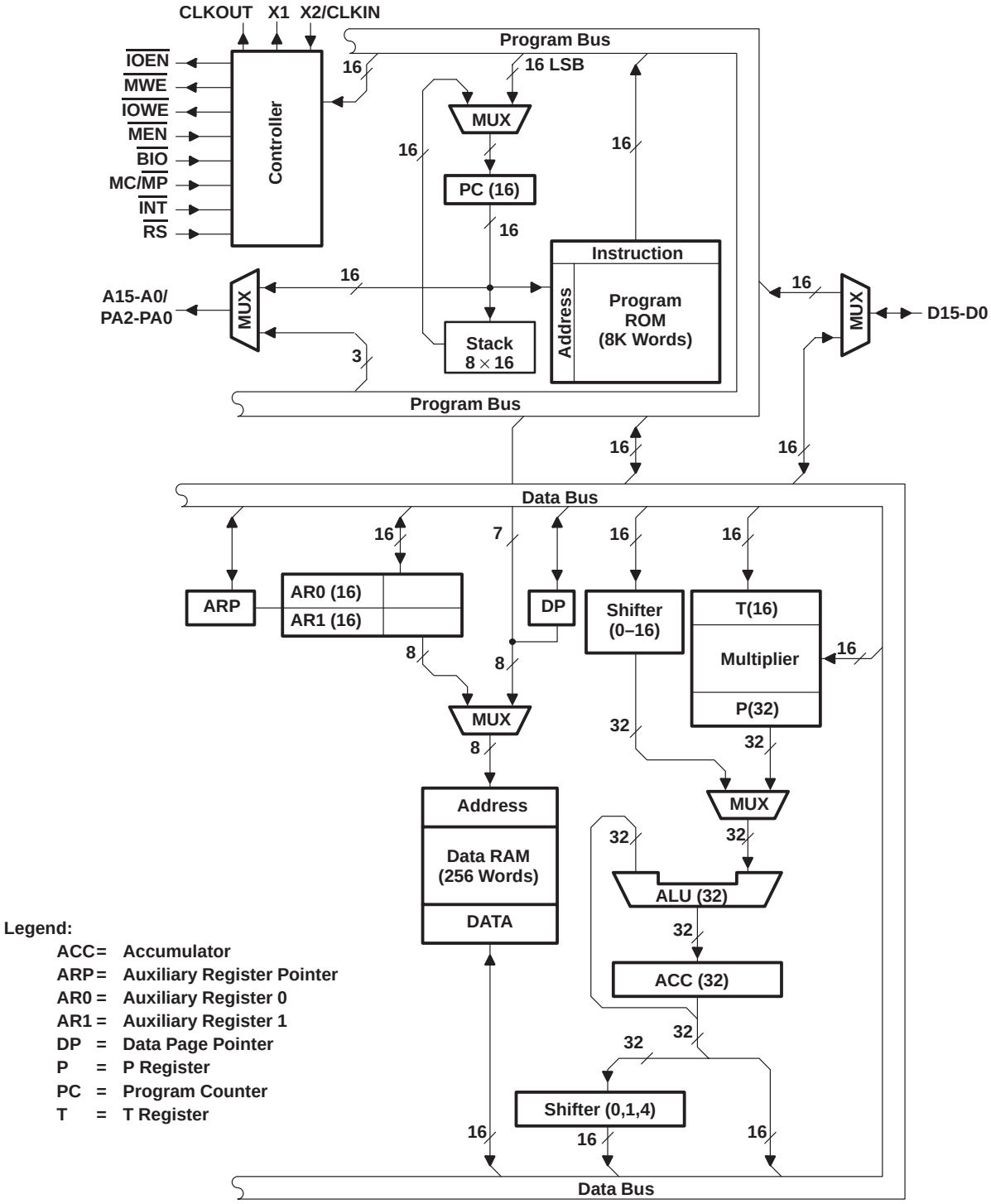
† Input/Output/High-impedance state.

TERMINAL FUNCTIONS (concluded)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			INTERRUPT AND MISCELLANEOUS SIGNALS
$\overline{BIO}$	64	I	External polling input. Polled by BIOZ instruction. If low, the device branches to the address specified by the instruction.
$\overline{IOEN}$	54	O	Data enable for device input data. When active (low), $\overline{IOEN}$ indicates that the device will accept data from the data bus. $\overline{IOEN}$ is active only during the IN instruction. When $\overline{IOEN}$ is active, $\overline{MEN}$, $\overline{IOWE}$, and $\overline{MWE}$ will always be inactive (high).
$\overline{IOWE}$	52	O	Write enable for device output data. When active (low), $\overline{IOWE}$ indicates that data will be output from the device on the data bus. $\overline{IOWE}$ is active only during the OUT instruction. When $\overline{IOWE}$ is active, $\overline{MEN}$, $\overline{IOEN}$, and $\overline{MWE}$ will always be inactive (high).
$\overline{INT}$	63	I	External interrupt input. The interrupt signal is generated by applying a negative-going edge to the $\overline{INT}$ pin. The edge is used to latch the interrupt flag register (INTF) until an interrupt is granted by the device. An active low level will also be sensed.
MC/$\overline{MP}$	62	I	Memory mode select pin. High selects the microcomputer mode, in which 8K words of on-chip program memory are available. A low on MC/$\overline{MP}$ pin enables the microprocessor mode. In this mode, the entire memory space is external; i.e., addresses 0 through 65535.
$\overline{MEN}$	56	O	Memory enable. $\overline{MEN}$ is an active (low) control signal generated by the device to enable instruction fetches from program memory. $\overline{MEN}$ will be active on instructions fetched from both internal and external memory. When $\overline{MEN}$ is active, $\overline{MWE}$, $\overline{IOWE}$, and $\overline{IOEN}$ will be inactive (high).
$\overline{MWE}$	53	O	Write enable for device output data. When active (low), $\overline{MWE}$ indicates that data will be output from the device on the data bus. $\overline{MWE}$ is active only during the TBLW instruction. When $\overline{MWE}$ is active, $\overline{MEN}$, $\overline{IOEN}$, and $\overline{IOWE}$ will always be inactive (high).
NC	1, 12, 18, 19, 24, 29, 33, 50, 51, 55	—	No connection.
$\overline{RS}$	2	I	Schmitt-triggered input for initializing the device. When held active for a minimum of five clock cycles. $\overline{IOEN}$, $\overline{IOWE}$, $\overline{MWE}$, and $\overline{MEN}$ are forced high; and, the data bus (D15 through D0) is not driven. The program counter (PC) and the address bus (A15 through A0) are then synchronously cleared after the next complete clock cycle from the falling edge of $\overline{RS}$. Reset also disables the interrupt, clears the interrupt flag register, and leaves the overflow mode register unchanged. The device can be held in the reset state indefinitely.
			SUPPLY/OSCILLATOR SIGNALS
PIN NAME	**PIN NO.**	**I/O/Z†**	**DESCRIPTION**
CLKOUT	9	O	System clock output (one-fourth crystal/CLKIN frequency).
V_{DD}	26, 57, 58, 59, 60	I	5-V suppy pins.
V_{SS}	5, 6, 7, 8, 42, 61	I	Ground pins.
X1	3	O	Crystal output pin for internal oscillator. If the internal oscillator is not used, this pin should be left unconnected.
X2/CLKIN	4	I	Input pin to the internal oscillator (X2) from the crystal. Alternatively, an input pin for an external oscillator (CLKIN).

† Input/Output/High-impedance state.

functional block diagram



Legend:

ACC	=	Accumulator
ARP	=	Auxiliary Register Pointer
AR0	=	Auxiliary Register 0
AR1	=	Auxiliary Register 1
DP	=	Data Page Pointer
P	=	P Register
PC	=	Program Counter
T	=	T Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 6) . . . . . –0.3 V to 7 V
Input voltage range . . . . . –0.3 V to 7 V
Output voltage range . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . 0.5 W
Operating free-air temperature: . . . . . 0°C to 70°C
Storage temperature . . . . . –55 °C to 150 °C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2			V
		CLKIN	3			V
V_{IL}	Low-level input voltage	All inputs except MC/$\overline{MP}$			0.8	V
		MC/$\overline{MP}$			0.6	V
I_{OH}	High-level output current, all outputs				–300	µA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 µA		V_{CC} – 0.4			
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{OZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	µA
				V_O = 0.4 V			–20	
I_I	Input current		V_{CC} = V_{SS} to V_{CC}	All inputs except CLKIN			±20	µA
				CLKIN			±50	
I_{CC}	Supply current		f = 35 MHz, V_{CC} = 5.25 V			60	75	mA
C_i	Input capacitance	Data bus	f = 1 MHz, all other pins 0 V			25		pF
		All others				15		
C_o	Output capacitance	Data bus				25		pF
		All others				10		

internal clock option

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_X	T_A = 0°C to 70°C	6.7		35.1	MHz
C1, C2	T_A = 0°C to 70°C		10		pF

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	28.49	28.57	150	ns
$t_{r(MC)}$	Rise time, master clock input		5	10	ns
$t_{f(MC)}$	Fall time, master clock input		5	10	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.45t_{c(C)}$		$0.55t_{c(C)}$	ns
$t_{w(MCL)}$	Pulse duration, master clock low		10		ns
$t_{w(MCH)}$	Pulse duration, master clock high		10		ns

switching characteristics over recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time	113.96	114.3	600	ns
$t_{r(C)}$	CLKOUT rise time		10		ns
$t_{f(C)}$	CLKOUT fall time		8		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low		49		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high		47		ns
$t_{d(MCC)}$	Delay time, CLKIN↑ to CLKOUT↓	5		50	ns

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
t_{d1}	Delay time, $\overline{MEN}\uparrow$, $\overline{MWE}\uparrow$, $\overline{IOEN}\uparrow$, $\overline{IOWE}\uparrow$, to next address bus valid	0		35	ns
t_{d2}	Delay time, CLKOUT$\downarrow$ to $\overline{MEN}\downarrow$	$^1/_4t_{c(C)} - 5$		$^1/_4t_{c(C)} + 12$	ns
t_{d3}	Delay time, CLKOUT$\downarrow$ to $\overline{MEN}\uparrow$	– 3		6	ns
t_{d4}	Delay time, CLKOUT$\downarrow$ to $\overline{IOEN}\downarrow$	$^1/_4t_{c(C)} - 5$		$^1/_4t_{c(C)} + 12$	ns
t_{d5}	Delay time, CLKOUT$\downarrow$ to $\overline{IOEN}\uparrow$	– 3		6	ns
t_{d6}	Delay time, CLKOUT$\downarrow$ to $\overline{MWE}\downarrow$, $\overline{IOWE}\downarrow$	$^1/_2t_{c(C)} - 5$		$^1/_2t_{c(C)} + 12$	ns
t_{d7}	Delay time, CLKOUT$\downarrow$ to $\overline{MWE}\uparrow$, $\overline{IOWE}\uparrow$	– 3		6	ns
t_{d8}	Delay time, $\overline{MWE}\downarrow$, $\overline{IOwE}\downarrow$, data bus out valid			0	ns
$t_{d9(CLK)}$	Delay time, CLKOUT$\downarrow$ to data bus starts to be driven	$^1/_4t_{c(C)} - 5$			ns
$t_{d9(MEN)}$	Delay time, $\overline{MEN}\uparrow$, to data bus starts to be driven	$^1/_4t_{c(C)}$			ns
$t_{d10(CLK)}$	Delay time, CLKOUT$\downarrow$ to data bus stops being driven			15	ns
$t_{d10(WE)}$	Delay time, $\overline{MWE}\uparrow$, $\overline{IOWE}\uparrow$, data bus stops being driven			20	ns
t_v	Data bus OUT valid after $\overline{MWE}\uparrow$, $\overline{IOWE}\uparrow$	5	10		ns
$t_{h(A\text{-}WMD)}$	Address bus hold time after $\overline{MWE}\uparrow$, $\overline{MEN}\uparrow$, $\overline{IOWE}\uparrow$, or $\overline{IOEN}\uparrow$	0	2		ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{MEN}\downarrow$, $\overline{IOEN}\downarrow$	5			ns

timing requirements over recommended operating conditions

		MIN	MAX	UNIT
$t_{su(D)}$	Setup time, data bus valid prior to $\overline{MEN}\uparrow$, $\overline{IOEN}\uparrow$	35		ns
$t_{h(D)}$	Hold time, data bus held valid after $\overline{MEN}\uparrow$, $\overline{IOEN}\uparrow$	0		ns

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		MIN	MAX	UNIT
t_{d11}	Delay time, $\overline{IOEN}\uparrow$, $\overline{IOWE}\uparrow$, $\overline{MWE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}$		$^1/_2t_{c(C)} + 50$	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$		$^1/_4t_{c(C)} + 50$	ns

timing requirements over recommended operating conditions

		MIN	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT	30		ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$		ns

INTERRUPT ($\overline{\text{INT}}$) TIMING

timing requirements over recommended operating conditions

		MIN	MAX	UNIT
$t_{f(INT)}$	Fall time, $\overline{\text{INT}}$		15	ns
$t_{w(INT)}$	Pulse duration, $\overline{\text{INT}}$	$t_{c(C)}$		ns
$t_{su(INT)}$	Setup time, $\overline{\text{INT}}\downarrow$ before CLKOUT$\downarrow$	30		ns

IO ($\overline{\text{BIO}}$) TIMING

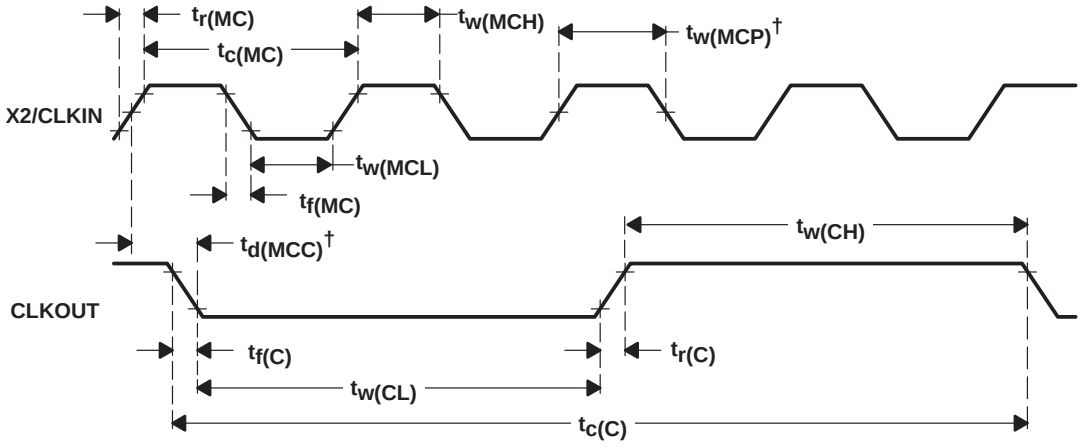
timing requirements over recommended operating conditions

		MIN	MAX	UNIT
$t_{f(IO)}$	Fall time, $\overline{\text{BIO}}$		15	ns
$t_{w(IO)}$	Pulse duration, $\overline{\text{BIO}}$	$t_{c(C)}$		ns
$t_{su(IO)}$	Setup time, $\overline{\text{BIO}}\downarrow$ before CLKOUT$\downarrow$	30		ns

TIMING DIAGRAMS

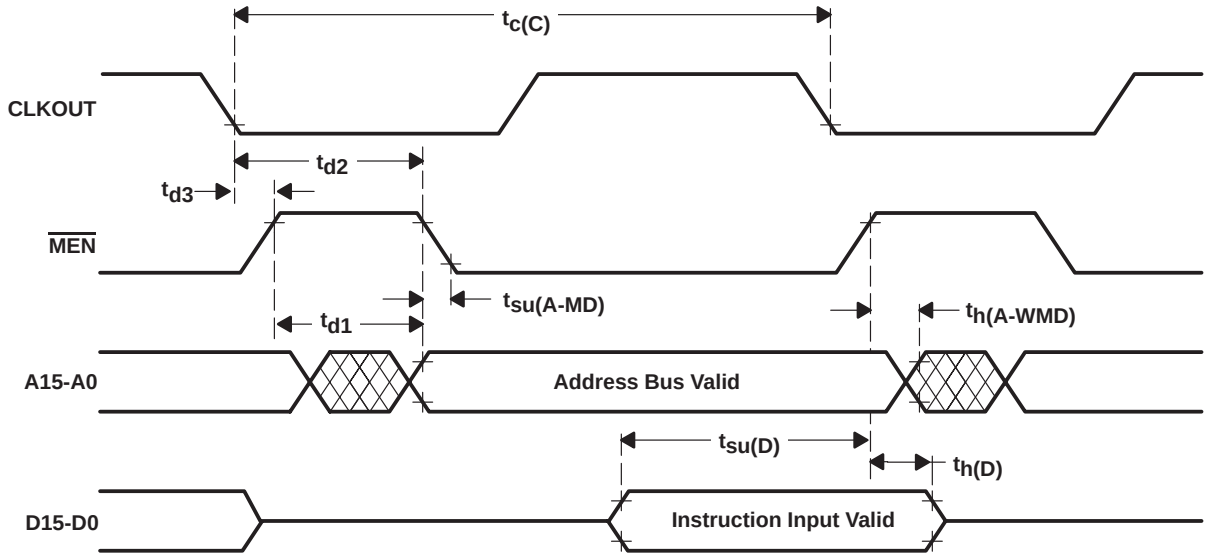
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

clock timing

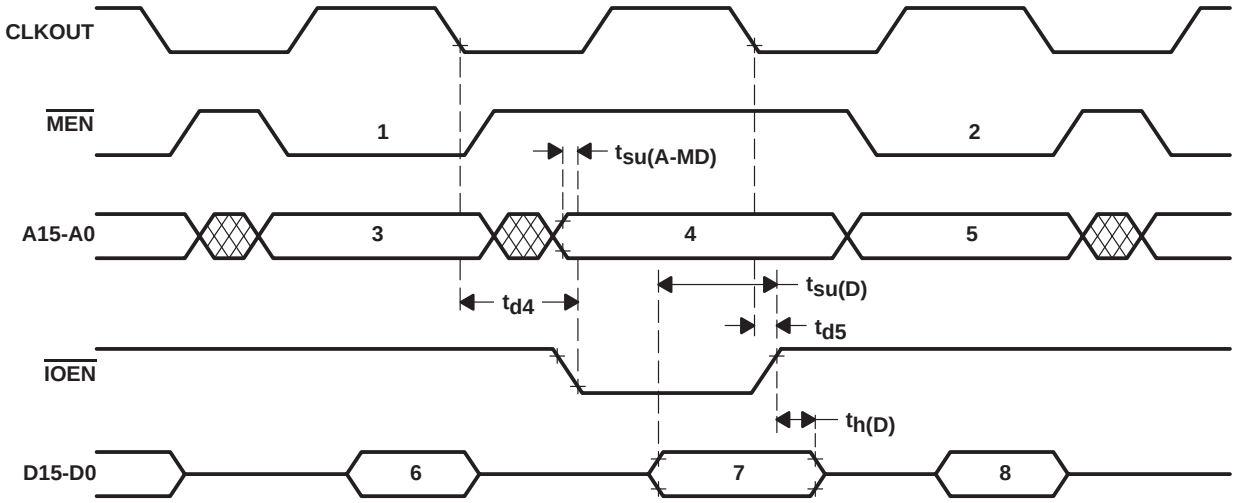


† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

memory read timing



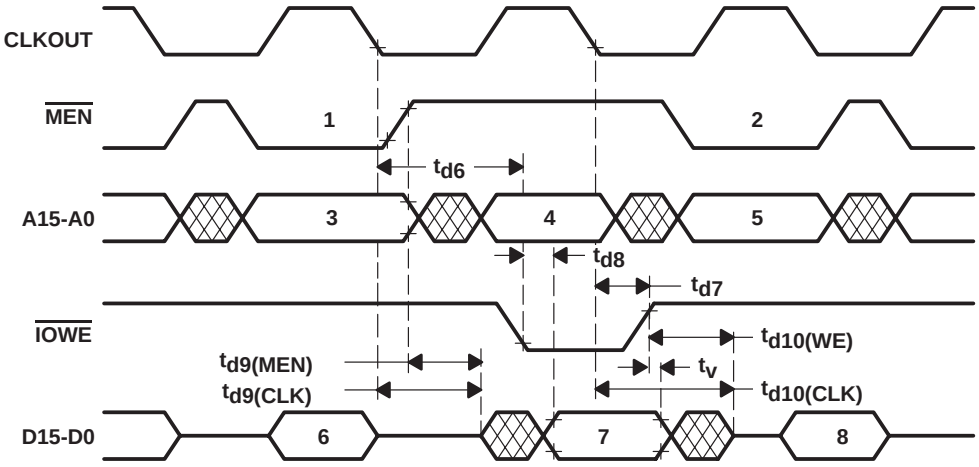
IN instruction timing



Legend:

1. IN instruction prefetch
2. Next instruction prefetch
3. Address bus valid
4. Peripheral address valid
5. Address bus valid
6. Instruction input valid
7. Data input valid
8. Instruction input valid

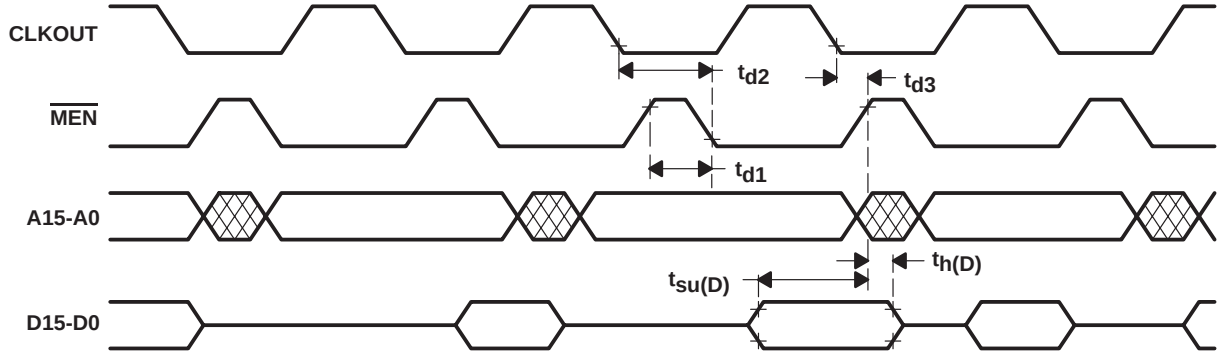
OUT instruction timing



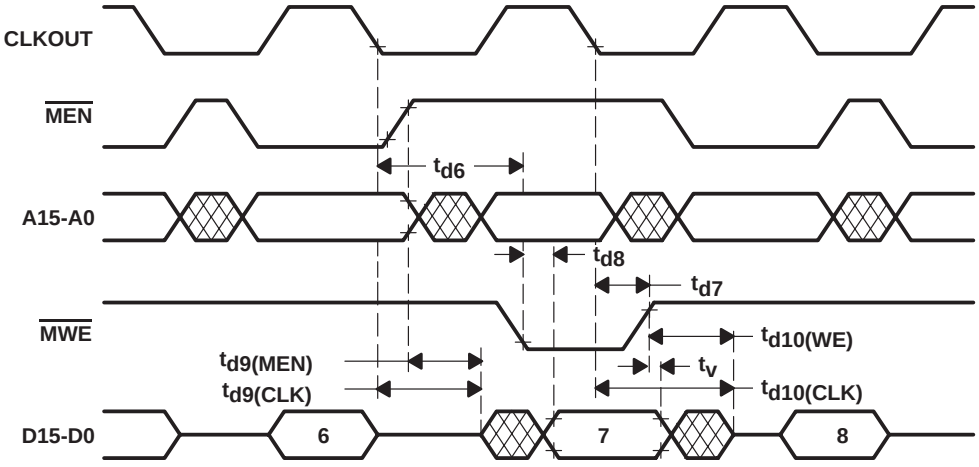
Legend:

1. OUT instruction prefetch
2. Next instruction prefetch
3. Address bus valid
4. Peripheral address valid
5. Address bus valid
6. Instruction valid
7. Data output valid
8. Instruction valid

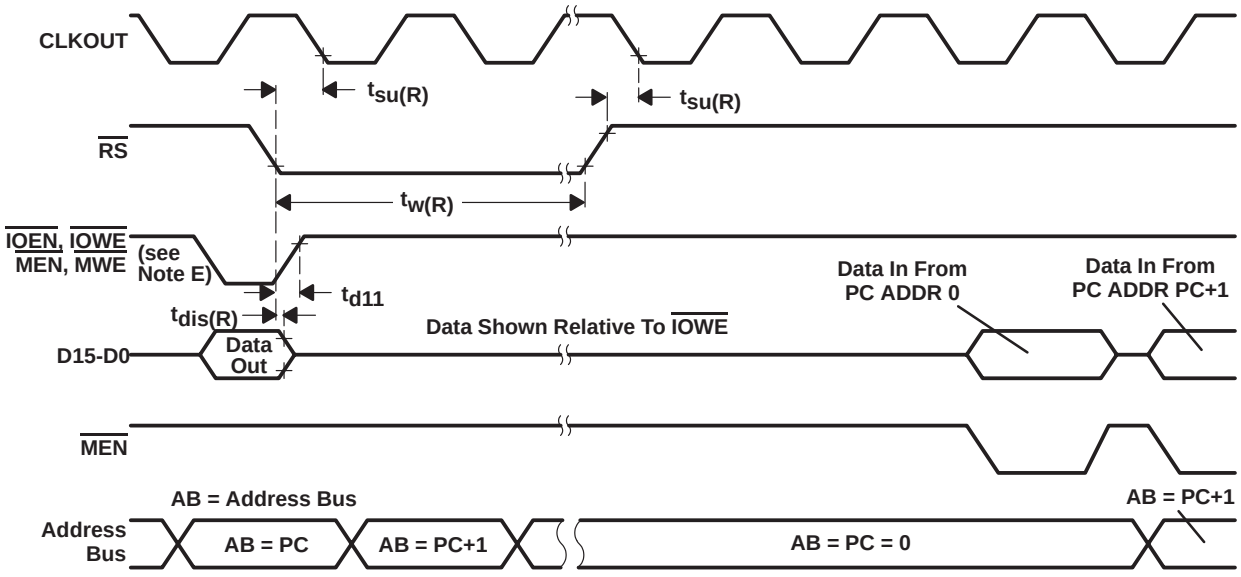
TBLR instruction timing



TBLW instruction timing



reset timing



NOTES: A. $\overline{RS}$ forces $\overline{IOEN}$, $\overline{IOWE}$, $\overline{MWE}$, and $\overline{MEN}$ high and places data bus D0 through D15 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}\downarrow$.

B. $\overline{RS}$ must be maintained for a minimum of five clock cycles.

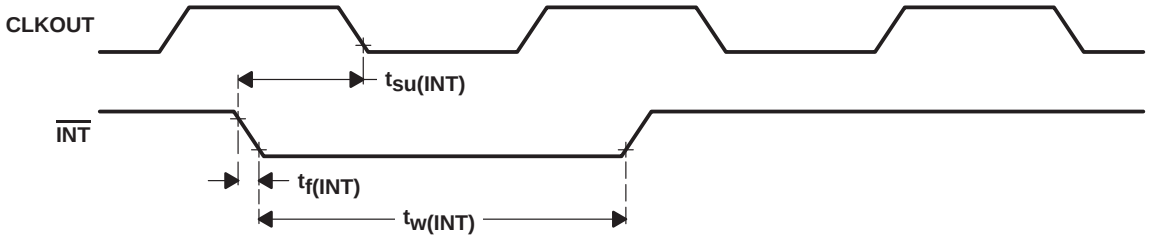
C. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}\uparrow$.

D. Due to the synchronization action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}\uparrow$ or $\overline{RS}\downarrow$ occur in the CLK cycle.

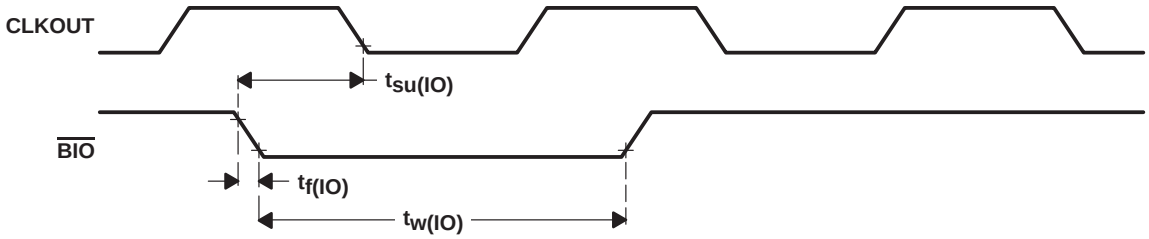
E. Diagram shown is for definition purpose only. $\overline{IOEN}$, $\overline{IOWE}$, $\overline{MWE}$, and $\overline{MEN}$ are mutually exclusive.

F. During a write cycle, $\overline{RS}$ may produce an invalid write address.

interrupt timing



$\overline{BIO}$ timing



design considerations for interfacing to SRAM, EPROM and peripherals

The ′C16 differs somewhat from the other members of the ′C1x family of digital signal processors (DSPs). Additional control signals are available for easier interface to external memory or peripherals, and the memory write cycle timings have been changed.

The discussion here will center around changes in t_v and its impact upon SRAM, EPROM and peripherals/latches interfaces.

Access time requirements for interface may be defined relative to :

1. Valid address (t_a);
2. $\overline{MEN}$/$\overline{IOEN}$, [($t_{a(MEN)}$];

Figure 11 and the following examples summarize these timings at 35 MHz CLKIN.

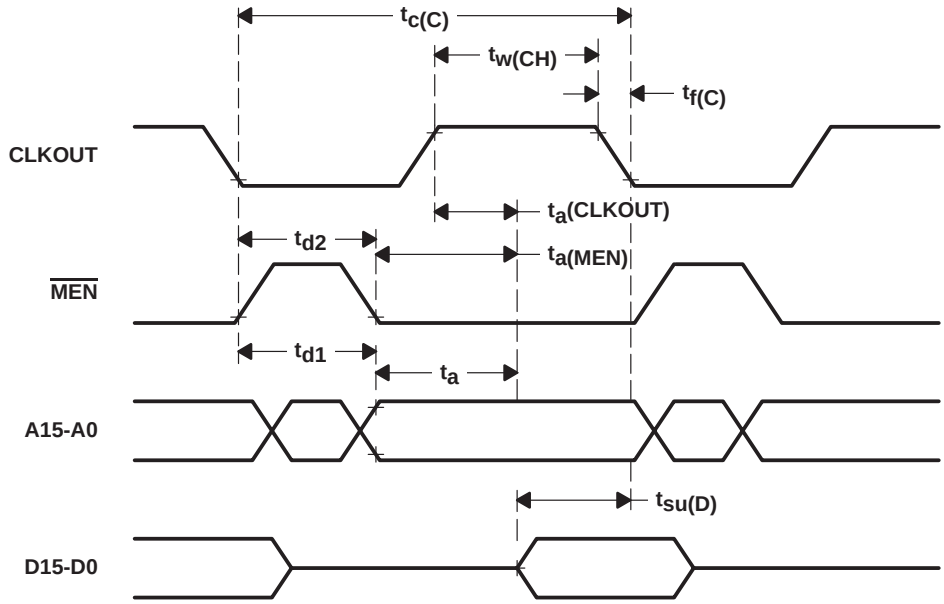


Figure 11.

where:

t_a : (access time from address valid) = $t_{c(C)} - t_{d1} - t_{su(D)}$ = 44.3 ns
$t_{a(MEN)}$: (access time from $\overline{MEN}$ valid) = $t_{c(C)} - t_{d2} - t_{su(D)} + t_{d3}$ = 35.73 ns

and where (for 35 MHz CLKIN):

$t_{c(C)}$ = 114.3 ns
t_{d1} = 35 ns
t_{d2} = [1/4 × (114.3) + 12] ns
$t_{su(D)}$ = 35 ns
$t_{w(CH)}$ = 47 ns nominal
$t_{f(C)}$ = 8 ns nominal

In addition to the above timings, t_v must be taken into account. t_v is the time that the data bus is guaranteed to be held after the rising edge of $\overline{MWE}$ or $\overline{IOWE}$. In other ′C1x devices, the value of t_v was referenced to CLKOUT↓ and not $\overline{WE}$↑ (see Figure 12). For the ′C16, t_v is a minimum of 5 ns. This implies that $\overline{MWE}$ and $\overline{IOWE}$ must be tied directly to the external device. If required, decode logic must be added to an input other than the read/write input — for example, the chip select on SRAMs. If the external device does not have two inputs, then transparent latches must be added to extend the time data is held on the data bus. These latches must be off the bus prior to the next instruction (see Figure 12).

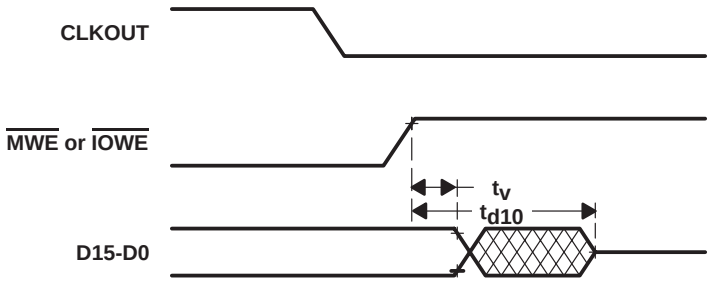


Figure 12.

where:

t_v = 5 ns (min)
t_{d10} = 15 ns (max)

There is a potential for bus conflict on the prefetch and execution of a TBLW or an OUT instruction. Figure 13 details the timings to be considered. In addition to the timings for the ′C16, timing definitions for interface are also included.

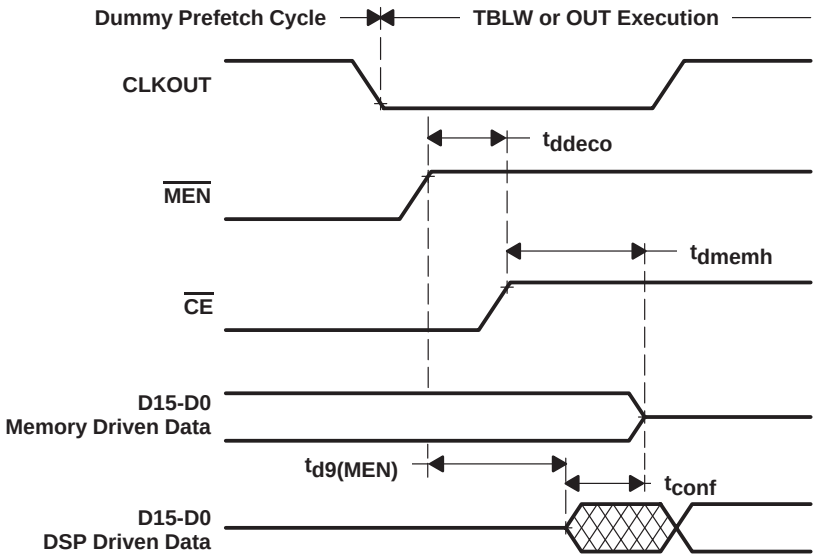


Figure 13.

where:

t_{conf} (data bus conflict time) = $t_{ddeco} + t_{dmemh} - t_{d9(MEN)}$

with:

t_{ddeco} : decode delay time to make the CE or OE signal
t_{dmemh} : memory data hold time from CE or OE
t_{d9} : delay time, $\overline{MEN}$ to data bus starts being driven
t_{d9} : (at 35 MHz CLKIN) = $[1/4t_{c(C)}]$ = [1/4(114.3)] = 28.58 ns

If t_{conf} is less than or equal to zero, data bus conflict does not occur.
If t_{conf} is greater than zero, data conflict occurs.

Note that the following discussion is for CLKIN of 35 MHz.

static memory with output enable and write enable/chip select

The following SRAMs are able to interface directly to the ′C16, needing only to directly connect the ′C16 memory control signals $\overline{MEN}$ and $\overline{MWE}$ to the memory. Device select decode is accomplished with address decode and then input to the device chip select.

PRODUCT	t_{ddeco}	t_{dmemh}	t_{dconf}	UNITS
TC55645-35	0	15	–13.58	ns
TC55328-35	0	15	–13.58	ns
TMS6789-35	0	8	–20.58	ns
TC5588-35	0	10	–18.58	ns
TMS6716-35	0	10	–18.58	ns

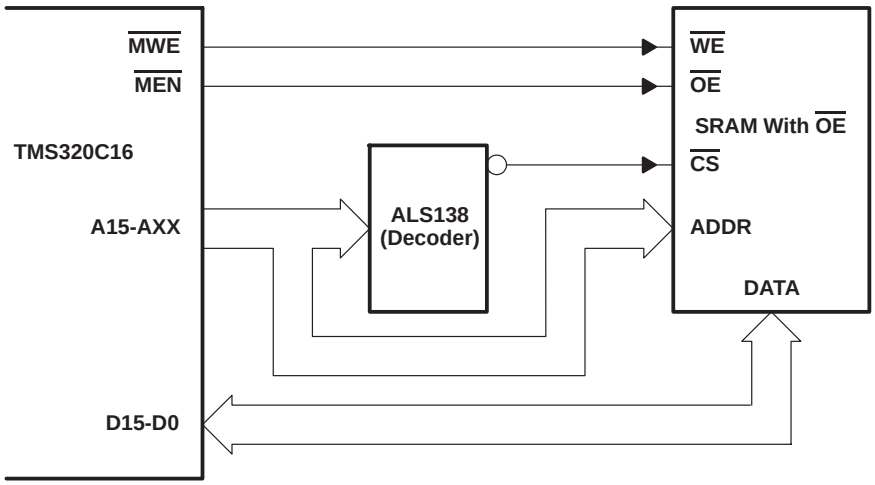


Figure 14.

static memory with chip enable and write enable

Without a separate output enable, a faster SRAM is required. Logic is added to decode address and memory control to perform a read/write cycle. The $\overline{\text{MWE}}$ signal is directly connected to the WE input of the SRAM to meet the t_v specification (see Figure 15).

Product	t_{ddeco}	t_{dmemh}	t_{dconf}	Units
CY7C164-25	7.5	10	– 11.08	ns

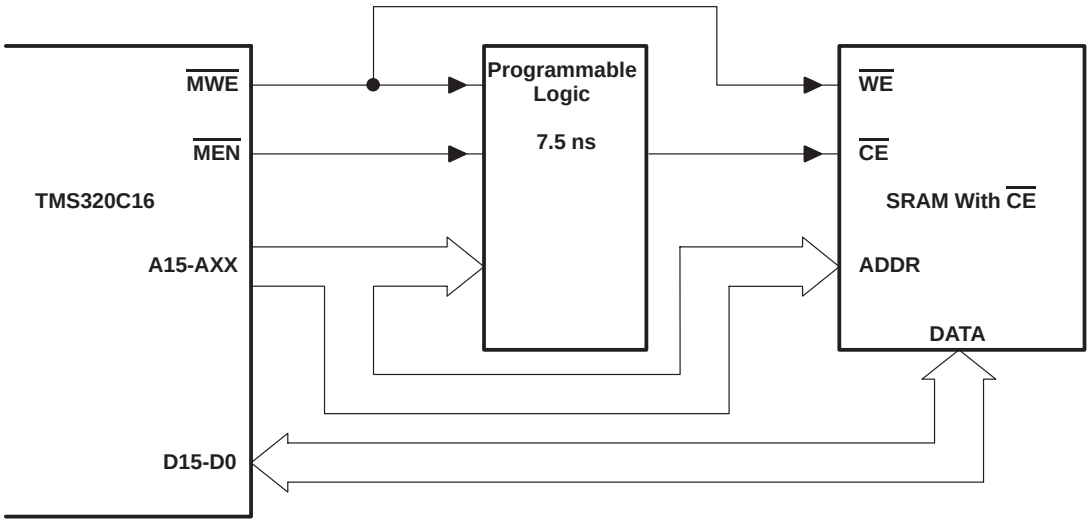


Figure 15.

EPROM interface

The following high-speed EPROMs can be used directly:

Product	t_{ddeco}	t_{dmemh}	t_{dconf}	Units
CY7C291-35	0	25	– 3.58	ns
TMS27C291-35	0	25	– 3.58	ns

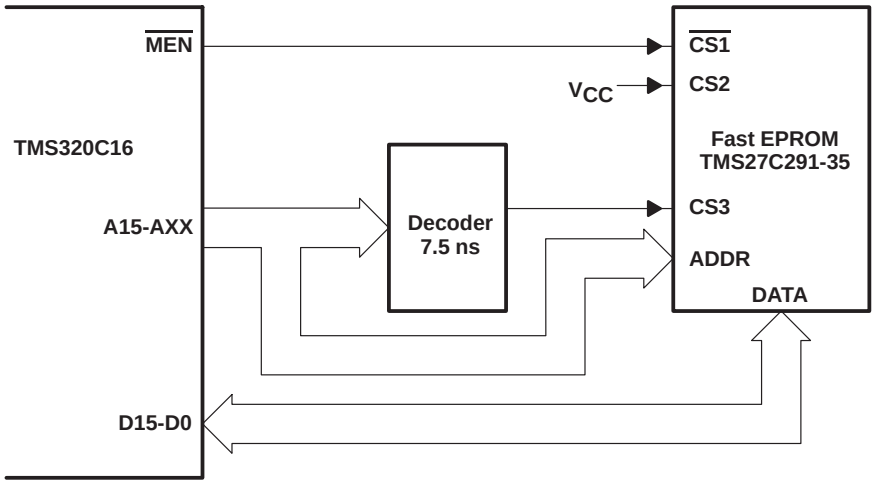


Figure 16.

interfacing latches to the TMS320C16

As with the previous devices, the memory control signal must be directly connected to the latch and the latch needs to have a separate chip select. There are several devices with this feature, including the SN74ALS996. The SN74ALS996 is an 8-bit D-type edge-triggered read-back latch with three-state outputs, connected to the ′C16 as illustrated in Figure 17.

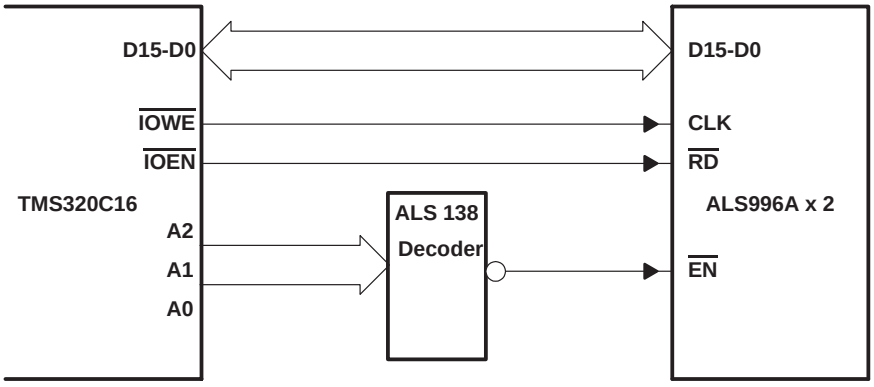
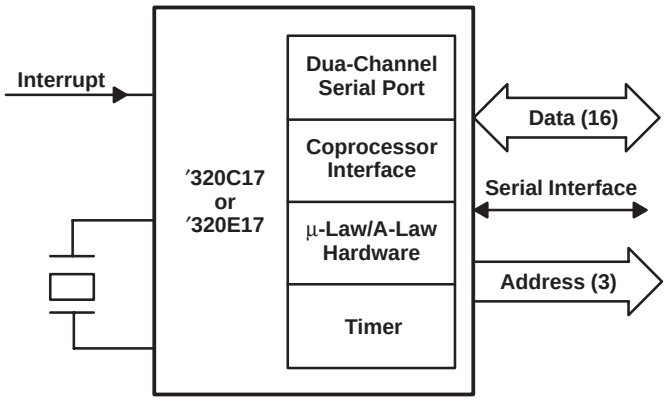


Figure 17.

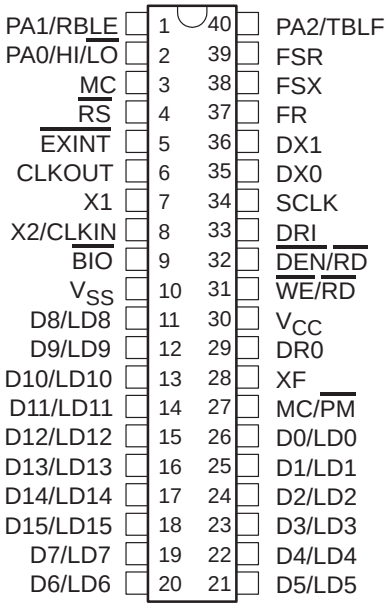
Key Features: TMS320C17/E17/LC17/P17

- 200-ns Instruction Cycle Timing (TMS320C17/E17/P17)
- 278-ns Instruction Cycle Timing (TMS320LC17)
- 256 Words of On-Chip Data RAM
- 4K Words of On-Chip Program ROM (TMS320C17/LC17)
- 4K Words of On-Chip Program EPROM (TMS320E17/P17)
- One-Time Programmable (OTP) Windowless EPROM Version Available (TMS320P17)
- EPROM Code Protection for Copyright Security
- Dual-Channel Serial Port for Full-Duplex Serial Communication
- Serial Port Timer for Standalone Serial Communication
- On-Chip Companding Hardware for μ-law/A-law PCM Conversions

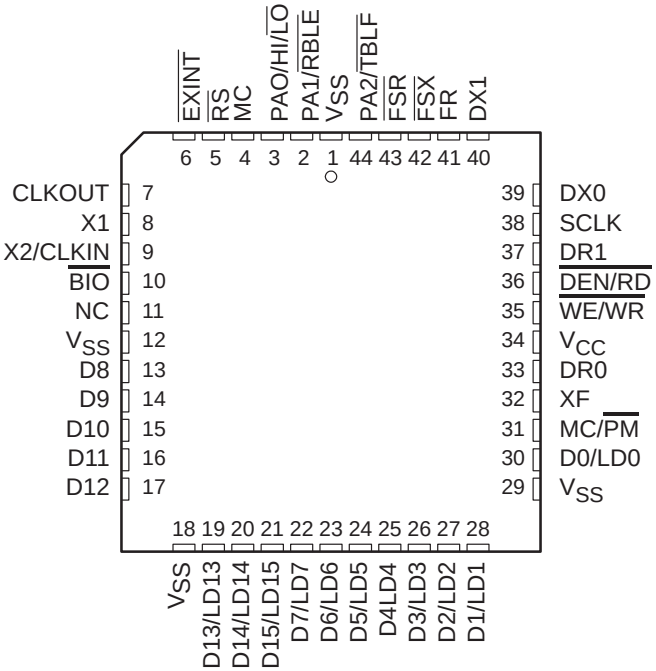


- Device Packaging:
  - 40-Pin DIP (All Devices)
  - 44-Lead PLCC (TMS320C17/LC17/P17
  - 44-Lead CER-QUAD (TMS320E17)
- 3.3 -V Low-Power Version Available (TMS320LC17)
- Operating Free-Air Temperature Range . . . 0°C to 70°C
- 16-Bit Coprocessor Interface for Common 4/8/16/32-Bit Microcomputers/Microprocessors

TMS320C17/E17/LC17/P17
N/JD Package
(Top View)



TMS320C17, TMS320E17
FN/FZ Packages
(Top View)



architecture

The ′C17/E17/LC17/P17 consists of five major functional units: the ′C15 microcomputer, a system control register, a full-duplex dual-channel serial port, companding hardware, and a coprocessor port.

Three of the I/O ports are used by the serial port, companding hardware, and the coprocessor port. Their operation is determined by the 32 bits of the system control register (see Table 6 for the control register bit definitions). Port 0 accesses control register 0 and consists of the lower 16 register bits (CR15-CR0), and is used to control the interrupts, serial port connections, and companding hardware operation. Port 1 accesses control register 1, consisting of the upper 16 control bits (CR31-CR16), as well as both serial port channels, the companding hardware, and the coprocessor port channels. Communication with the control register is via IN and OUT instructions to ports 0 and 1.

Interrupts fully support the serial port interface. Four maskable interrupts ($\overline{\text{EXINT}}$, FR, $\overline{\text{FSX}}$, and $\overline{\text{FSR}}$) are mapped into I/O port 0 via control register 0. When disabled, these interrupts may be used as single-bit logic inputs polled by software.

serial port

The dual-channel serial port is capable of full-duplex serial communication and offers direct interface to two combo-codecs. Two receive and two transmit registers are mapped into I/O port 1, and operate with 8-bit data samples. Internal and external framing signals for serial port transfers (MSB first) are selected via the system control register. The serial port clock, SCLK, provides the bit timing for transfers with the serial port, and may be either an input or output. As an input, an external clock provides the timing for data transfers and framing pulse synchronization. As an output, SCLK provides the timing for standalone serial communication and is derived from the ′C17/E17/P17 system clock, X2/CLKIN, and system control register bits CR27-CR24 (see Table 7 for the available divide ratios). The internal framing (FR) pulse frequency is derived from the serial port clock (SCLK) and system control register bits CR23-CR16. This framing pulse signal provides framing pulses for combo-codecs, for a sample clock for voice-band systems, or for a timer used in control applications.

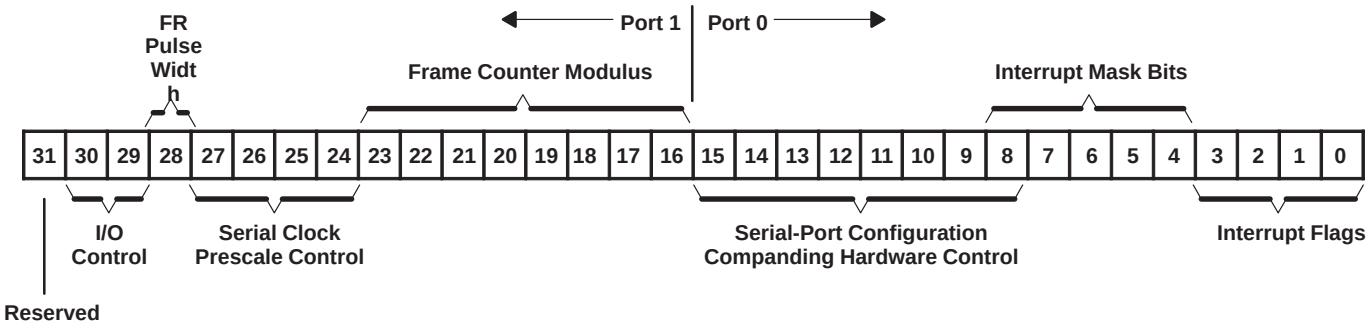
μ-law/A-law companding hardware

The ′C17/E17/LC17/P17 features hardware companding logic and can operate in either μ-law or A-law format with either sign-magnitude or twos-complement numbers. Data may be companded in either a serial mode for operation on serial port data or a parallel mode for computation inside the device. The companding logic operation is selected through CR14. No bias is required when operating in twos-complement. A bias of 33 is required for sign-magnitude in μ-law companding. Upon reset, the device is programmed to operate in sign-magnitude mode. This mode can be changed by modifying control bit 29 (CR29) in control register 1. For further information on companding, see the *TCM29C13/TCM29C14/TCM29C16/TCM29C17 Combined Single-Chip PCM Codec and Filter Data Sheet*, and the application report, "*Companding Routines for the TMS32010/TMS32020,"* in the book *Digital Signal Processing Applications with the TMS320 Family* (SPRA012A), both documents published by Texas Instruments.

In the serial mode, sign-magnitude linear PCM (13 magnitude bits plus 1 sign bit for μ-law format or 12 magnitude bits plus 1 sign bit for A-law format) is compressed to 8-bit sign-magnitude logarithmic PCM by the encoder and sent to the transmit register for transmission on an active framing pulse. The decoder converts 8-bit sign-magnitude log PCM from the serial port receive registers to sign-magnitude linear PCM.

In the parallel mode, the serial port registers are disabled to allow parallel data from internal memory to be encoded or decoded for computation inside the device. In the parallel encode mode, the encoder is enabled and a 14-bit sign-magnitude value written to port 1. The encoded value is returned with an IN instruction from port 1. In the parallel decode mode, the decoder is enabled and an 8-bit sign-magnitude log PCM value is written to port 1. On the successive IN instruction from port 1, the decoded value is returned. At least one instruction should be inserted between an OUT and the successive IN when companding is performed with twos-complement values.

Table 6. Control Register Configuration



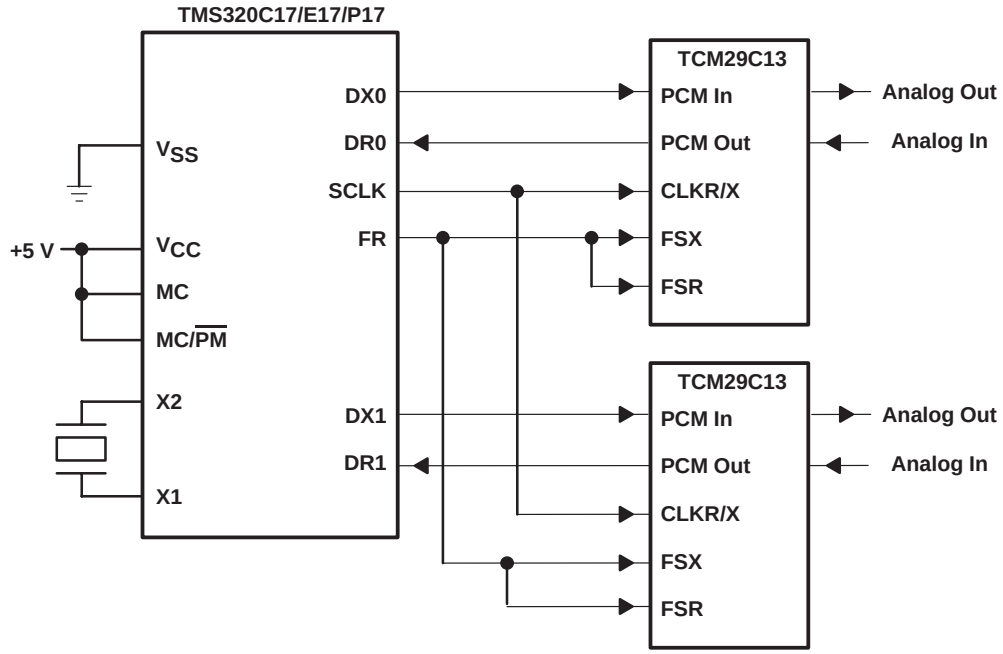
BIT	DESCRIPTION AND CONFIGURATION
0	$\overline{\text{EXINT}}$ Interrupt flag†
1	$\overline{\text{FSR}}$ interrupt flag†
2	$\overline{\text{FSX}}$ interrupt flag†
3	FR interrupt flag†
4	$\overline{\text{EXINT}}$ interrupt enable mask. When set to logic 1, an interrupt on $\overline{\text{EXINT}}$ activates device interrupt circuitry.
5	$\overline{\text{FSR}}$ interrupt enable mask. Same as $\overline{\text{EXINT}}$ control.
6	$\overline{\text{FSX}}$ interrupt enable mask. Same as $\overline{\text{EXINT}}$ control.
7	FR interrupt enable mask. Same as $\overline{\text{EXINT}}$ control.
8	Port 1 configuration control: 0 = port 1 connects to either serial-port registers or companding hardware. 1 = port 1 accesses CR31-CR16.
9	External framing enable: 0 = serial-port data transfers controlled by active FR. 1 = serial-port data transfers controlled by active $\overline{\text{FSX}}$/$\overline{\text{FSR}}$.
10	XF external logic output flag latch
11	Serial-port enable: 0 = Parallel companding mode; serial port disabled. 1 = serial companding mode; serial port registers enabled.
12	μ-law/A-law encoder enable: 0 = disabled. 1 = data written to port 1 is μ-law or A-law encoded.
13	μ-law/A-law decoder enable: 0 = disabled. 1 = data written to port 1 is μ-law or A-law decoded.
14	μ-law/A-law decoder encode/decoded select: 0 = companding hardware performs μ-law conversion. 1 = companding hardware performs A-law conversion.
15	Serial clock control: 0 = SCLK is an output, derived from the prescaler in timing logic. 1 = SCLK is an input that provides the clock for serial port and frame counter in timing logic.
23-16	Frame counter modulus. Controls FR frequency = SCLK/(CNT + 2) where CNT is binary value fo CR23-CR16‡
27-24	SCLK prescale cotnrol bits. (See Table 7 for divide ratios.)
28	FR pulse-width control: 0 = fixed-data rate; FR is 1 SCLK cycle wide. 1 = variable-data rate; FR is 8 SCLK cycles wide.
29	Two's-complement μ-law/A-law conversion enable: 0 = sign-magnitude companding 1 = twos-complement companding
30	8/16-bit length coprocessor mode select: 0 = 8-bit byte length 1 = 16-bit word length
31	Reserved for future expansion: Should be set to zero.

† Interrupt flag is cleared by writing a logic 1 to the bit with an OUT instruction to port 0.
‡ All ones in CR23-CR16 indicate a degenerative state and should be avoided. Bits are operational whether SCLK is an input or an output. CNT must be greater than 7.

Table 7. Serial Clock (SCLK) Divide Ratios (X2/CLKIN = 20.48 MHz)

CR27	CR26	CR25	CR24	DIVIDE RATIO	SCLK FREQUENCY	UNIT
0	0	0	0	32	0.640	MHz
0	0	0	1	28	0.731	MHz
0	0	1	0	24	0.853	MHz
0	1	0	0	20	1.024	MHz
1	0	0	0	16	1.280	MHz
1	0	0	1	14	1.463	MHz
1	0	1	0	12	1.706	MHz
1	1	0	0	10	2.048	MHz

The specification for μ-law and A-law log PCM coding is part of the CCITT G.711 recommendation. The following diagram shows a ′C17/E17/P17 interface to two codecs as used for μ-law or A-law companding format.



coprocessor port

The coprocessor port, accessed through I/O port 5 using IN and OUT instructions, provides a direct connection to most 4/8-bit microcomputers and 16/32-bit micorprocessors. The coprocessor interface allows the ′C17/E17/P17 to act as a peripheral (slave) microcomputer to a microprocessor, or a master to a peripheral microcomputer such as TMS7042. The coprocessor port is enabled by setting MC/$\overline{PM}$ and MC low. The microcomputer mode is enabled by setting these two pins high. (Note that MC/$\overline{PM}$ ≠ MC is undefined.)
In the microcomputer mode, the 16 data lines are used for the 6 parallel 16-bit I/O ports.

In the coprocessor mode, the 16-bit coprocessor port is reconfigured to operate as a 16-bit latched bus interface. Control bit 30 (CR30) in control register 1 is used to configure the coprocessor port to either an 8-bit or a 16-bit length. When CR30 is high, the coprocessor port is 16 bits wide thereby making all 16 bits of the data port available for 16-bit transfers to 16 and 32-bit microprocessors. When CR30 is low, the port is 8-bits wide and mapped to the low byte of the data port for interfacing to 8-bit microcomputers. When operating in the 8-bit mode, both halves of the 16-bit latch can be addressed using the HI/$\overline{LO}$ pin, thus allowing 16-bit transfers over 8 data lines. When not in the coprocessor mode, port 5 can be used as a generic I/O port.

coprocessor port (continued)

The external processor recognizes the coprocessor interface in which both processors run asynchronously as a memory-mapped I/O operation. The external processor lowers the $\overline{WR}$ line and places data on the bus. It next raises the $\overline{WR}$ line to clock the data into the on-chip latch. The rising edge of $\overline{WR}$ automatically creates an interrupt to the ′C17/E17/P17, and the falling edge of $\overline{WR}$ clears the $\overline{RBLE}$ (receive buffer latch empty) flag. When the ′C17/E17/P17 reads the coprocessor port, it causes the $\overline{RBLE}$ signal to transition to a logic low state that clears the data in the latch, and allows the interrupt condition to be cleared internally. Likewise, the external processor reads form the latch by driving the $\overline{RD}$ line active low, thus enabling the output latch to drive the latched data. When the data has been read, the external device will again bring the $\overline{RD}$ line high. This activates the $\overline{BIO}$ line to signal that the transfer is complete and the latch is available for the next transfer. The falling edge of $\overline{RD}$ resets the $\overline{TBLF}$ (transmit buffer latch full) flag. Note that the $\overline{EXINT}$ and $\overline{BIO}$ lines are reserved for coprocessor interface and cannot be driven externally when in the coprocessor mode.

An example of the use of a coprocessor interface is shown in Figure 18, in which the ′C17/E17/P17 are DSPs interfaced to the TMS70C42, an 8-bit microcontroller.

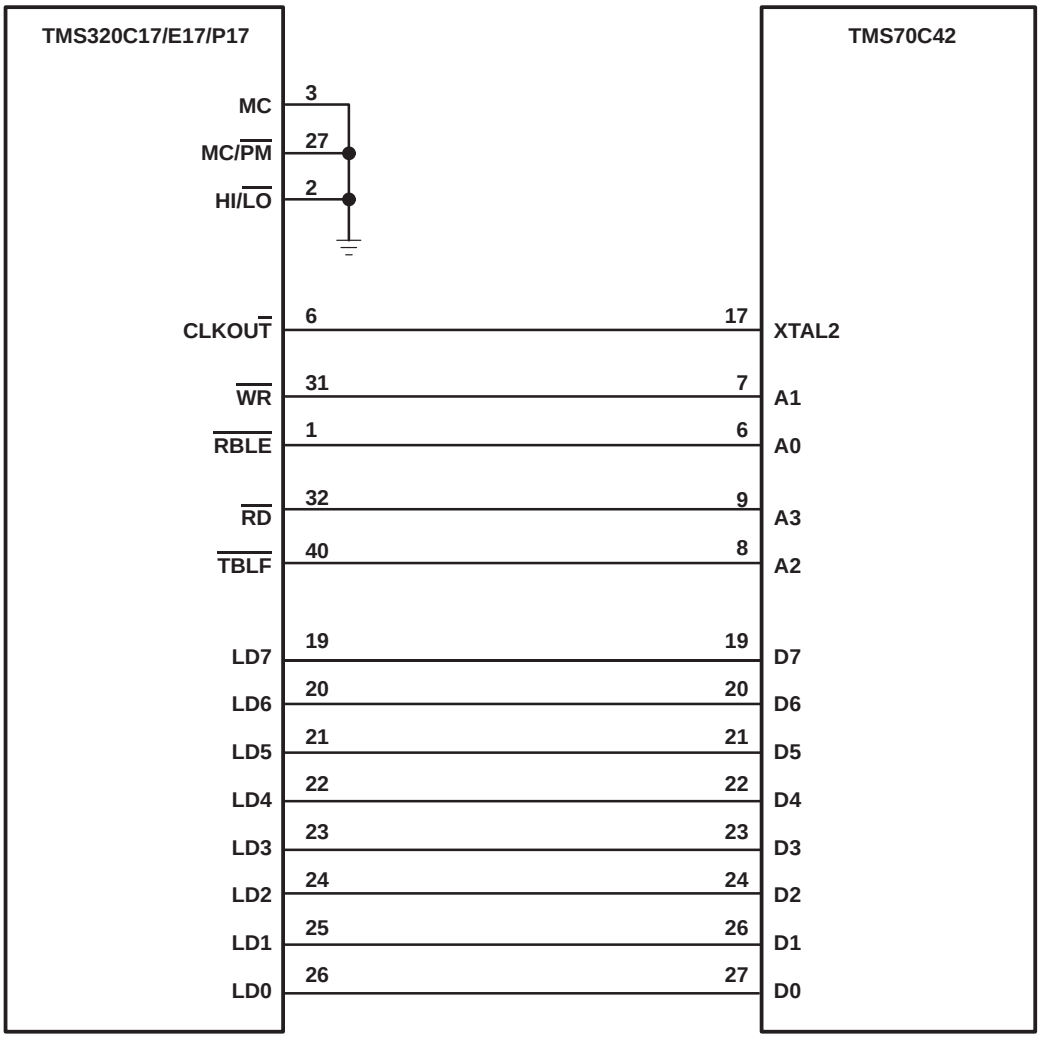


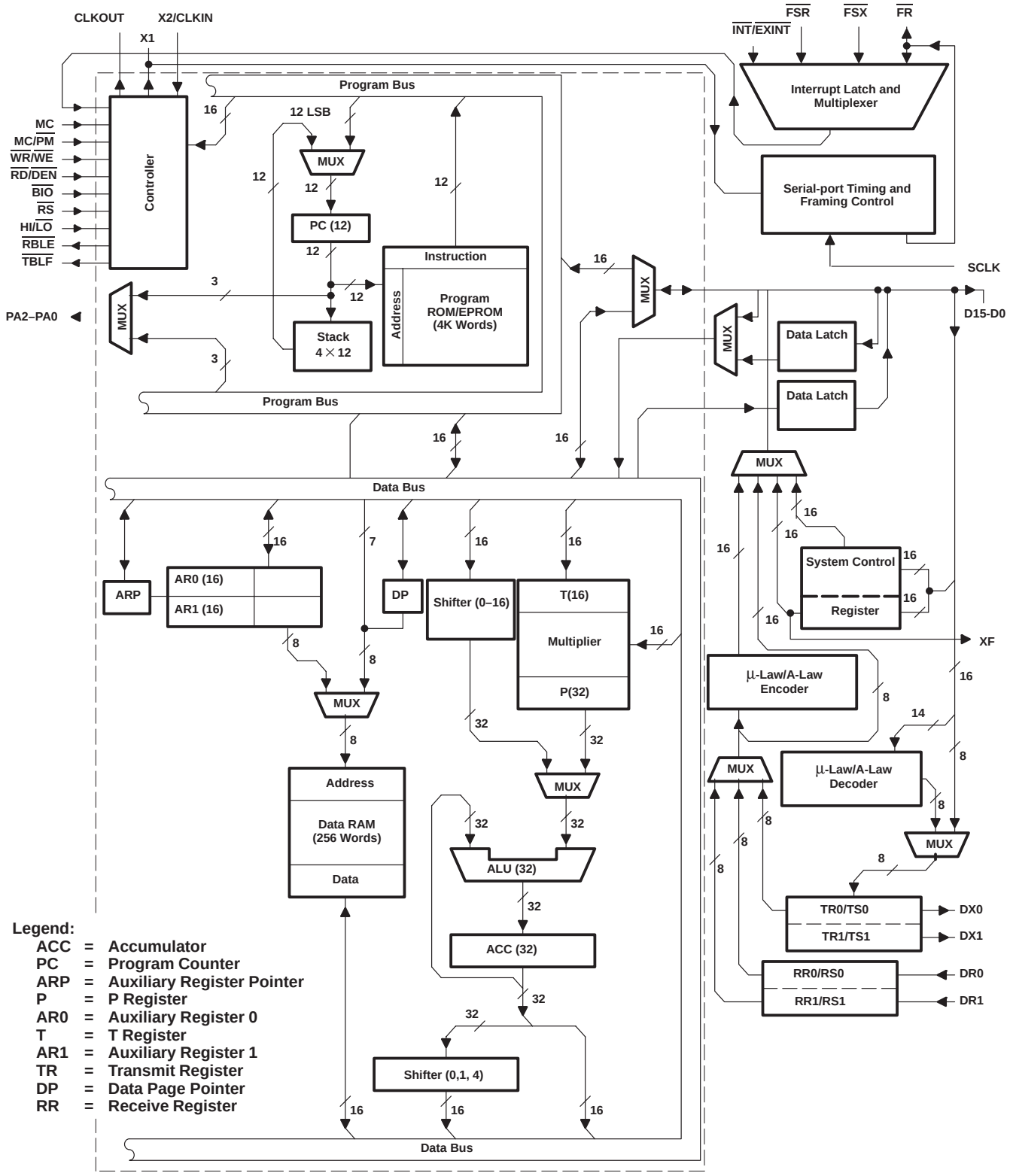
Figure 18. Coprocessor Interface

TERMINAL FUNCTIONS†

NAME	I/O‡	DEFINITION
$\overline{\text{BIO}}$	I	External polling input
CLKOUT	O	System clock output, 1/4 crystal/CLKIN frequency
D15/LD15-D0/LD0	I/O	16-bit parallel data bus/data lines for coprocessor latch
$\overline{\text{DEN}}$/$\overline{\text{RD}}$	I/O	Data enable for device input data/external read for output latch
DR1, DR0	I	Serial-port receive-channel inputs
DX1, DX0	O	Serial-port transmit-channel outputs
$\overline{\text{EXINT}}$	I	External interrupt input
FR	O	Internal serial-port framing output
$\overline{\text{FSR}}$	I	External serial-port receive framing input
$\overline{\text{FSX}}$	I	External serial-port transmit framing input
MC	I	Microcomputer select (must be same state as MC/$\overline{\text{PM}}$)
MC/$\overline{\text{PM}}$	I	Microcomputer/peripheral coprocessor select (must be same state as MC)
PA0/HI/$\overline{\text{LO}}$	I/O	I/O port address output/latch byte select pin
PA1/$\overline{\text{RBLE}}$	O	I/O port address output/receive buffer latch empty flag
PA2/$\overline{\text{TBLF}}$	O	I/O port address output/transmit buffer latch full flag
$\overline{\text{RS}}$	I	Reset for initializing the device
SCLK	I/O	Serial-port clock
V_{CC}	I	+ 5 V Supply
V_{SS}	I	Ground
$\overline{\text{WE}}$/$\overline{\text{WR}}$	O	Write enable for device output data/external write for input latch
X1	O	Crystal output for internal oscillator
X2/CLKIN	I	Crystal input for internal oscillator or external oscillator system clock input
XF	O	External-flag output pin

† See EPROM programming section.
‡ Input/Output/High-impedance state.

functional block diagram



Legend:

ACC	=	Accumulator
PC	=	Program Counter
ARP	=	Auxiliary Register Pointer
P	=	P Register
AR0	=	Auxiliary Register 0
T	=	T Register
AR1	=	Auxiliary Register 1
TR	=	Transmit Register
DP	=	Data Page Pointer
RR	=	Receive Register

electrical specifications

This section contains the electrical specifications for all versions of the ′C17/E17/P17 digital signal processors, including test parameter measurement information. Parameters with $_{PP}$ subscripts apply only to the ′E17/P17 in the EPROM programming mode (see Note 11).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, except for the ′320LC17 (see Note 6) . . . . . –0.3 V to 7 V
Supply voltage range, V_{PP} . . . . . –0.6 V to 14 V
Input voltage range . . . . . –0.3 V to 14 V
Output voltage range . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . 1.5 W
Operating free-air temperature: L suffix . . . . . 0°C to 70°C
A suffix . . . . . – 40°C to 85°C
Storage temperature . . . . . –55 °C to 150 °C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	EPROM devices	4.75	5	5.25	V
		All other devices	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 11)		12.25	12.5	12.75	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2			V
		CLKIN	3			V
V_{IL}	Low-level input voltage	All inputs except MC/$\overline{MP}$			0.8	V
		MC/$\overline{MP}$			0.6	V
I_{OH}	High-level output current, all outputs				–300	µA
I_{OL}	Low-level output current (All outputs)				2	mA
T_A	Operating free-air temperature	L suffix	0		70	°C
		A suffix	– 40		85	°C

NOTE 11: V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡ Supply current	TMS320C17	f = 20.5 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		50	65	mA
	TMS320E17/P17	f = 25.6 MHz, V_{CC} = 5.5 V, T_A = – 40°C to 85°C		55	75	

† All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡ I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependance on temperature, frequency, and loading, see Figure 3.

CLOCK CHARACTERISTICS AND TIMING

The ′C17/E17/P17 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and should be specified at a load capacitance of 20 pF.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_x	TMS320C17	T_A = 0°C to 70°C	6.7		20.5	MHz
	TMS320E17/P17	T_A = – 40°C to 85°C	6.7		20.5	
C1, C2		T_A = 0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time§	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	195.12	200		ns
$t_{r(C)}$	CLKOUT rise time			10¶		ns
$t_{f(C)}$	CLKOUT fall time			8¶		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92¶		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90¶		ns
$t_{d(MCC)}$	Delay time, CLKIN↑ to CLKOUT↓		25¶		60¶	ns

§ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
¶ Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	ns
$t_{r(MC)}$	Rise time, master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time, master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.45t_{c(MC)}$†		$0.6t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration, master clock low		20†		ns
$t_{w(MCH)}$	Pulse duration, master clock high		20†		ns

† Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	10†		50	ns
t_{d4}	Delay time, CLKOUT↓ to $\overline{DEN}$↓		$1/4t_{c(C)} - 5$†		$1/4t_{c(C)} + 15$	ns
t_{d5}	Delay time, CLKOUT↓ to $\overline{DEN}$↑		–10†		15	ns
t_{d6}	Delay time, CLKOUT↓ to $\overline{WE}$↓		$1/2t_{c(C)} - 5$†		$1/2t_{c(C)} + 15$	ns
t_{d7}	Delay time, CLKOUT↓ to $\overline{WE}$↑		–10†		15	ns
t_{d8}	Delay time, CLKOUT↓ to data bus OUT valid				$1/4t_{c(C)} + 65$	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$1/4t_{c(C)} - 5$†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops bieng driven				$1/4t_{c(C)}+70$†	ns
t_v	Data bus OUT valid after CLKOUT↓		$1/4t_{c(C)}-10$			ns
$t_{h(A-WMD)}$	Address hold time after $\overline{WE}$↑, or $\overline{DEN}$↑ (see Note 14)		0†	2†		ns
$t_{su(A-MD)}$	Address bus setup time prior to $\overline{DEN}$↓		$1/4t_{c(C)}-45$			ns

† Values derived from characterization data and not tested.
NOTE 14: Address bus will be valid upon $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)}$	Setup time, data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF (see Figure 2)	50			ns
$t_{h(D)}$	Hold time, data bus held valid after CLKOUT↓ (see Note 16)		0			ns

NOTE 16: Data may be removed from the data bus upon $\overline{DEN}$↑ preceding CLKOUT↓.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time, $\overline{DEN}\uparrow$, and $\overline{WE}\uparrow$ from $\overline{RS}$	R_L 825 Ω, C_L = 100 pF, (see Figure 2)		$1/2t_{c(C)}+50$†		ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$			$1/4t_{c(C)}+50$†		ns
t_{d12}	Delay time from $\overline{RS}\downarrow$ to high-impedance SCLK			200†		ns
t_{d13}	Delay time from $\overline{RS}\downarrow$ to high-impedance DX1, DX0			200†		ns

† Values derived form characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 10)	50			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{EXINT}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(INT)}$	Fall time, $\overline{EXINT}$			15	ns
$t_{w(INT)}$	Pulse duration, $\overline{EXINT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time, $\overline{EXINT}\downarrow$ before CLKOUT$\downarrow$	50			ns

IO ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(IO)}$	Fall time, $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration, $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time, $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	50			ns

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(XF)}$	Delay time CLOCKOUT$\uparrow$ to valid XF	R_L 825 Ω, C_L = 100 pF, (see Figure 2)	5†		115	ns

† Values derived form characterization data and not tested.

SERIAL PORT TIMING

switching characteristics over recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
$t_{d(CH-FR)}$	Internal framing (FR) delay from SCLK rising edge			70	ns
$t_{d(DX1-XL)}$	DX bit 1 valid before SCLK falling edge	20			ns
$t_{d(DX2-XL)}$	DX bit 2 valid before SCLK falling edge	20			ns
$t_{h(DX)}$	DX hold time after SCLK falling edge	$t_{c(SCLK)}/2$			ns

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(SCLK)}$	Serial port clock (SCLK) cycle time (see Note 17)	390		4770	ns
$t_{f(SCLK)}$	Serial port clock (SCLK) fall time			30†	ns
$t_{r(SCLK)}$	Serial port clock (SCLK) rise time			30†	ns
$t_{w(SCLKL)}$	Serial port clock (SCLK) low-pulse duration (see Note 17)	185		2500	ns
$t_{w(SCLKH)}$	Serial port clock (SCLK) high-pulse duration (see Note 17)	185		2500	ns
$t_{su(FS)}$	$\overline{FSX}/\overline{FSR}$ setup time before SCLK falling edge	100			ns
$t_{su(DR)}$	DR setup time before SCLK falling edge	20			ns
$t_{h(DR)}$	DR hold time after SCLK falling edge	20			ns

† Values derived from characterization data and not tested.

NOTES: 17. Minimum cycle time is $2t_{c(C)}$ where $t_{c(C)}$ is CLKOUT cycle time.
18. The duty cycle of the serial port clock must be within 45 to 55 percent.

COPROCESSOR INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
$t_{d(R-A)}$	$\overline{RD}$ low to $\overline{TBLF}$ high			75	ns
$t_{d(W-A)}$	$\overline{WR}$ low to $\overline{RBLE}$ high			75	ns
$t_{a(RD)}$	$\overline{RD}$ low to data valid			80	ns
$t_{h(RD)}$	Data hold time after $\overline{RD}$ high	25			ns

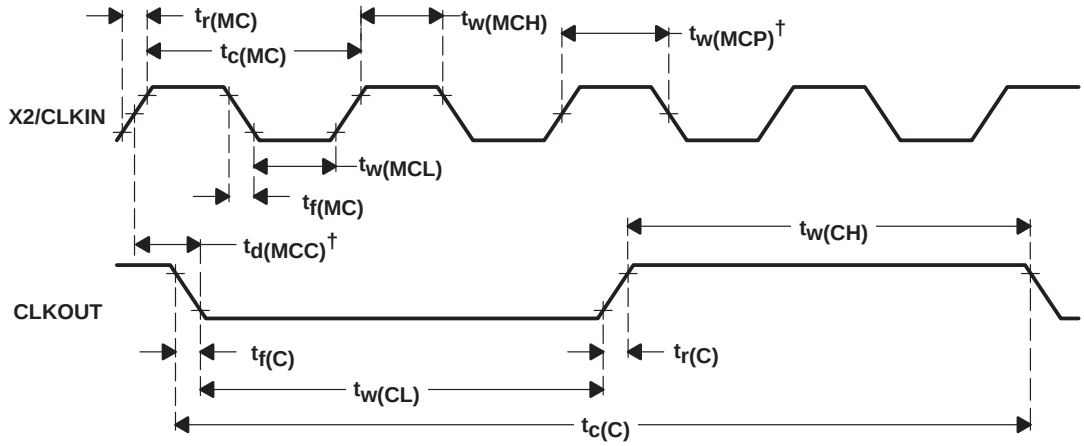
timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{h(HL)}$	HI/$\overline{LO}$ hold time after $\overline{WR}$ or $\overline{RD}$ high	25			ns
$t_{su(HL)}$	HI/$\overline{LO}$ setup time after $\overline{WR}$ or $\overline{RD}$ low	40			ns
$t_{su(WR)}$	Data setup time prior to $\overline{WR}$ high	30			ns
$t_{h(WR)}$	Data hold time after $\overline{WR}$ high	25			ns
$t_{w(RDL)}$	$\overline{RD}$ low-pulse duration	80			ns
$t_{w(WRL)}$	$\overline{WR}$ low-pulse duration	60			ns

TIMING DIAGRAMS

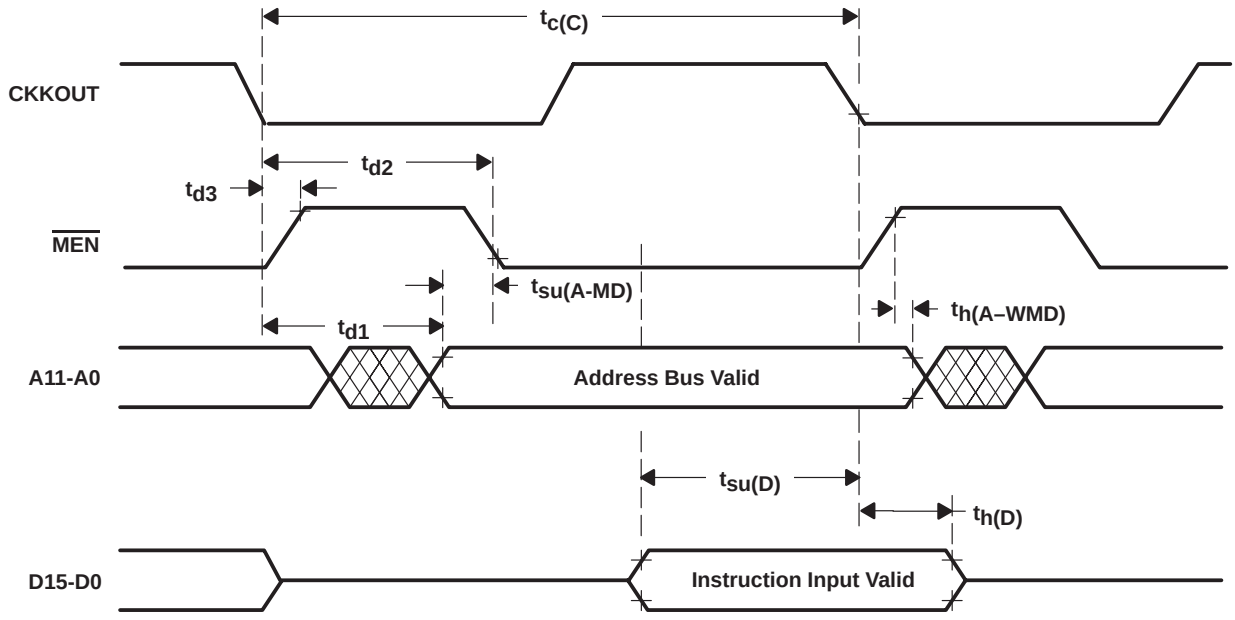
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2 volts, unless otherwise noted.

clock timing

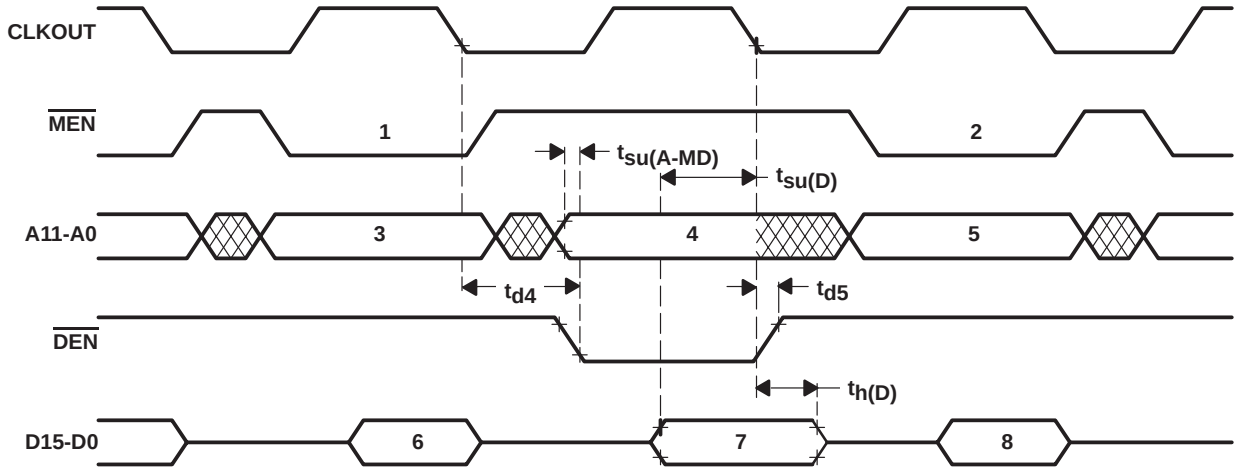


† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

memory read timing



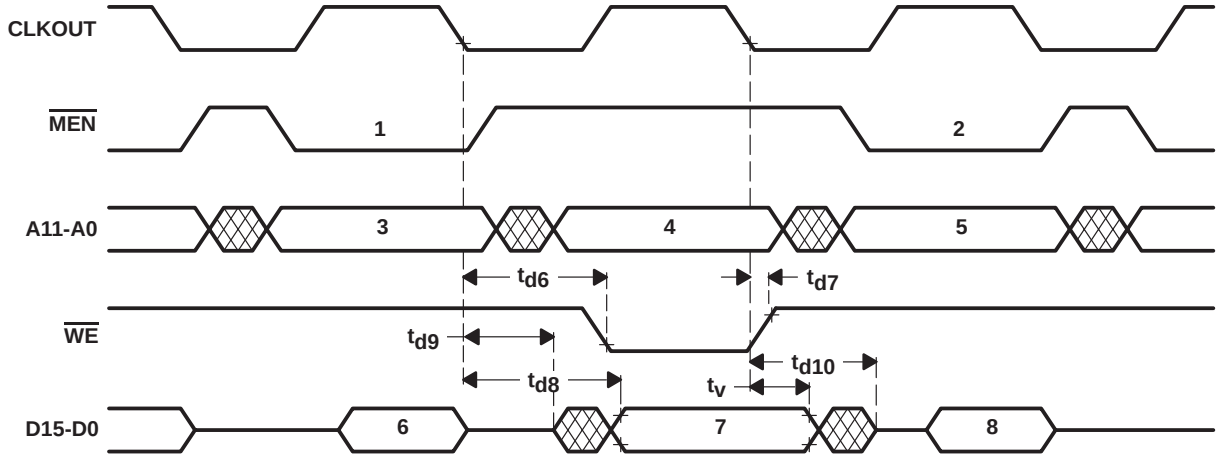
IN instruction timing



Legend:

1. IN Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Input Valid
7. Data Input Valid
8. Instruction Valid

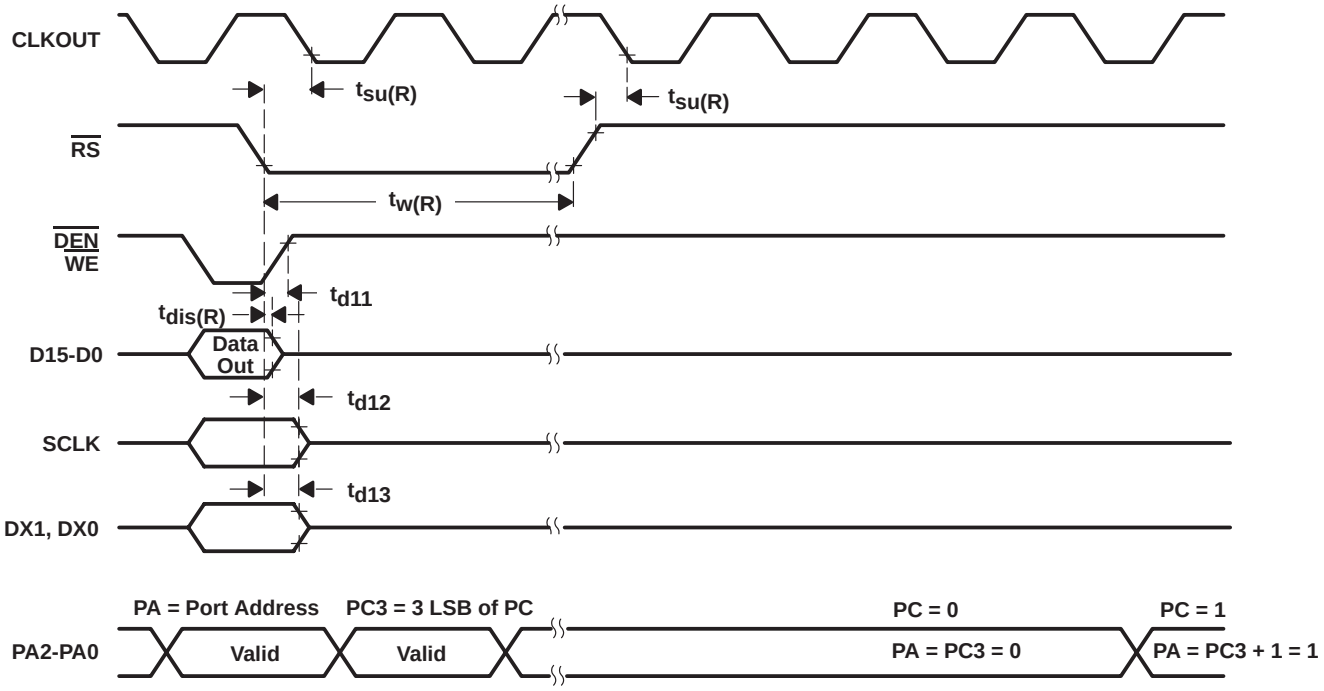
OUT instruction timing



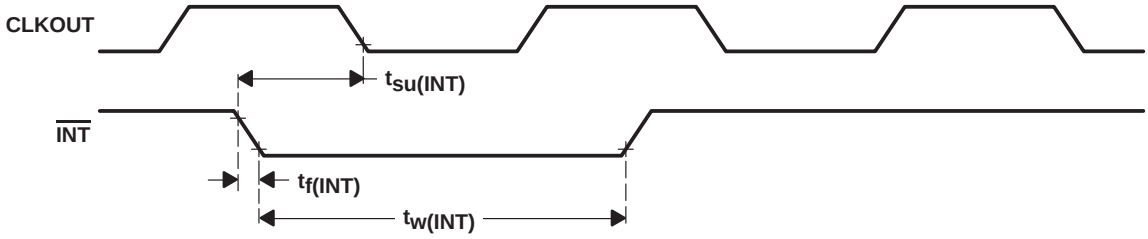
Legend:

1. OUT Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Input Valid
7. Data Output Valid
8. Instruction Valid

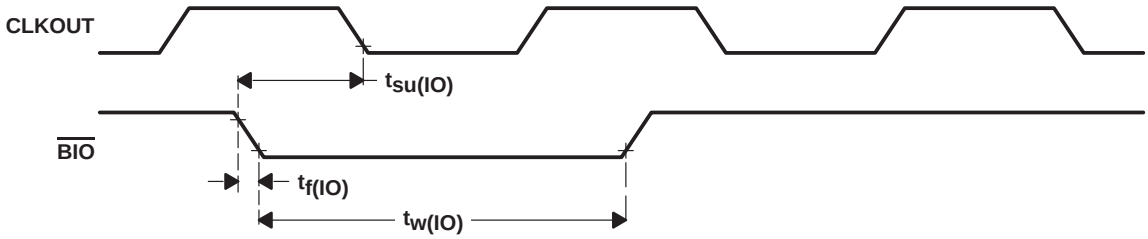
reset timing



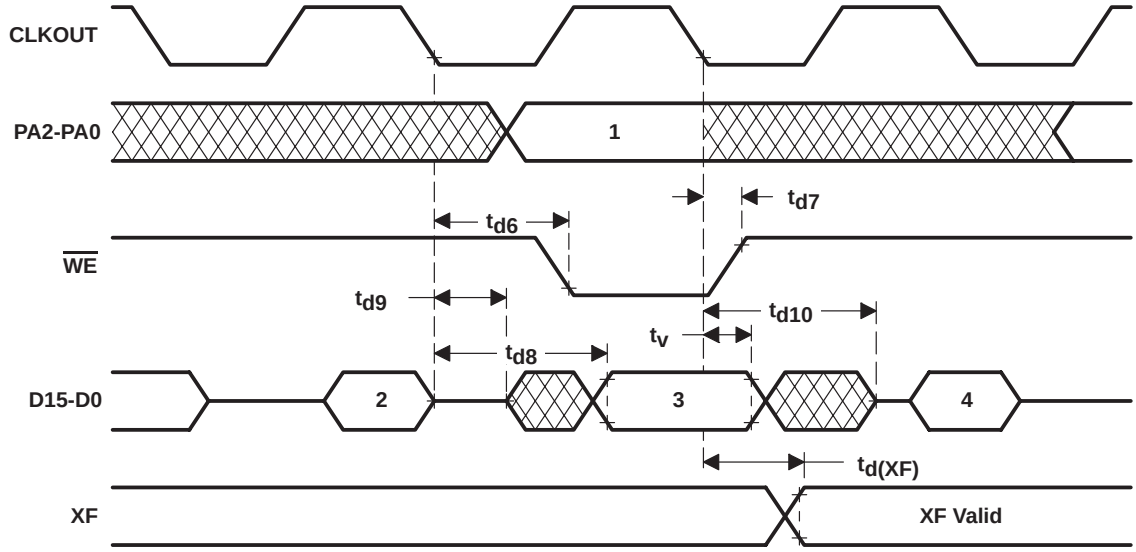
interrupt timing



$\overline{BIO}$ timing



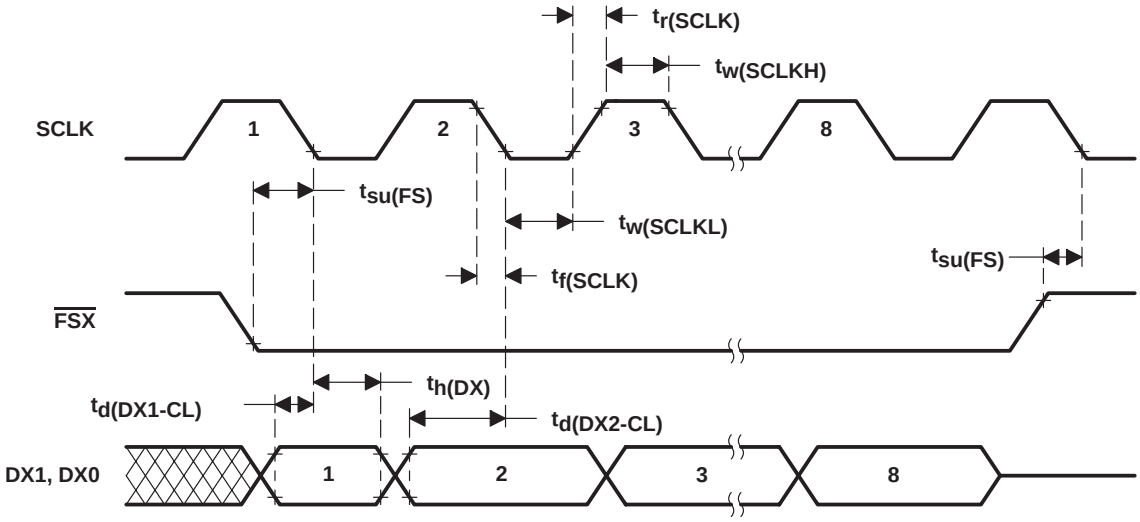
XF timing



Legend:

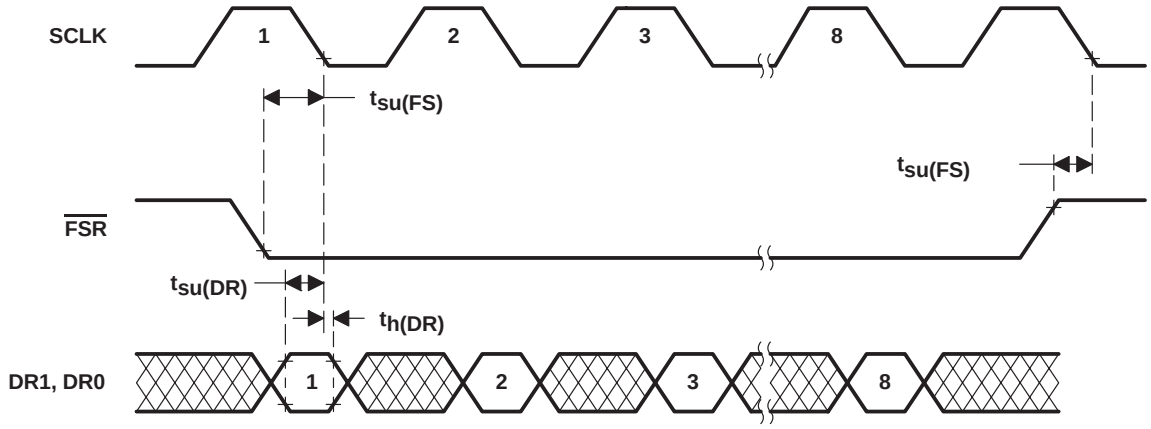
1. Port Address Valid
2. Out Opcode Valid
3. Port Data Valid
4. Next Instruction Opcode Valid

external framing: transmit timing



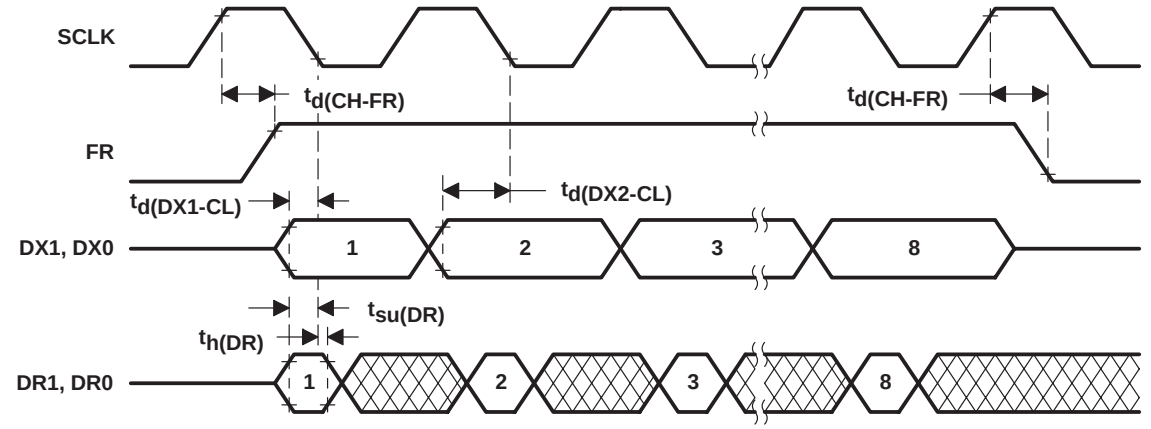
NOTES: A. Data valid on transmit output until SCLK rises.
B. The most significant bit is shifted first.

external framing: receive timing



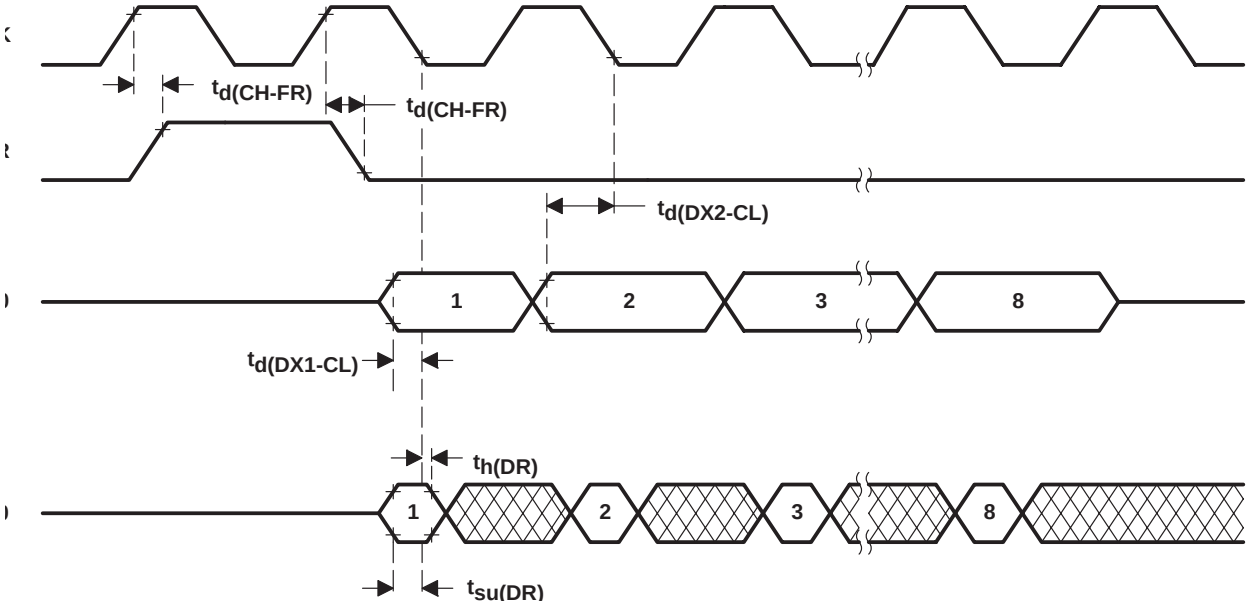
NOTE: The most significant bit is shifted first.

internal framing: variable-data rate



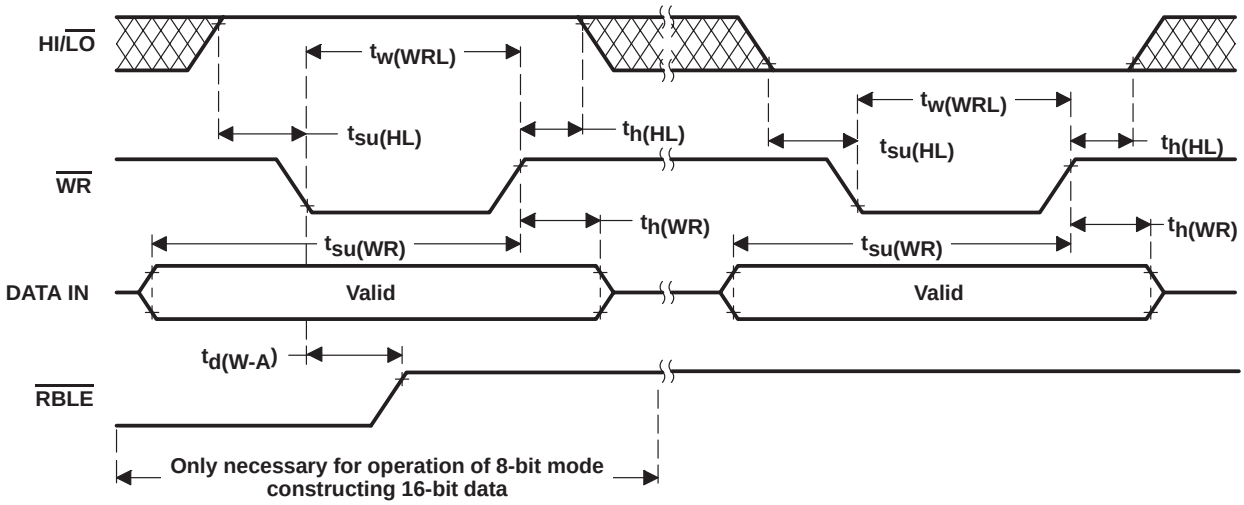
NOTE: The most significant bit is shifted first.

internal framing: fixed-data rate

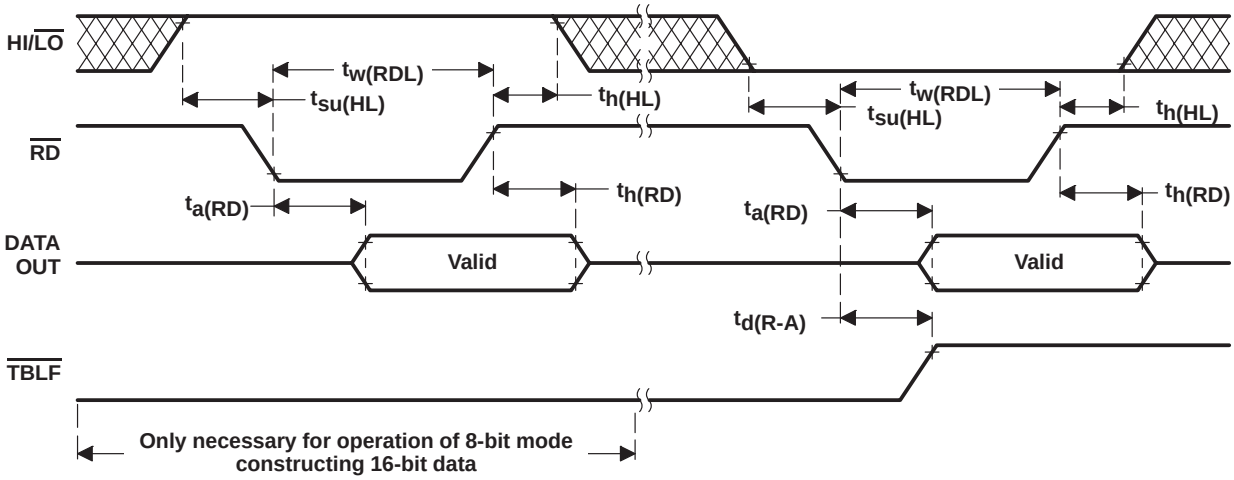


NOTE: The most significant bit is shifted first.

coprocessor timing: external write to coprocessor port



coprocessor timing: external read to coprocessor port



EPROM PROGRAMMING

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{PP} (see Note 6) . . . . . –0.6 V to 14 V

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{PP}	Supply voltage (see Note 11)		12.5	12.75	V

NOTE 11: V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{PP1}	V_{PP} supply current	$V_{PP} = V_{CC} = 5.5$ V			100	µA
I_{PP2}	V_{PP} supply current (during program pulse)	$V_{PP} = 12.75$ V, $V_{CC} = 5.5$ V		30	50	mA

recommended timing requirements for programming, $T_A = 25°C$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V, (see Note 13)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	3.8		63	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$ (see Note 15)	0		130‡	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150‡	ns
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

† Values derived from characterization data and not tested.

NOTES: 13. For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V and $V_{PP} = 12.5 \text{ V} \pm 0.25$ V during programming.

15. Common test conditions apply for $t_{dis(G)}$ except during programming.

PROGRAMMING THE TMS320E17/P17 EPROM CELL

Each ′E17/P17 devices include a 4K × 16-bit industry-standard EPROM cell for prototyping, early field testing, and low-volume production. In conjunction with this EPROM, the TMS320C17 with a 4K-word masked ROM, then, provides more migration paths for cost-effective production.

Note: The TMS320P17 is a one-time programmable (OTP) EPROM device.

EPROM adapter sockets are available that provide pin-to-pin conversions for programming any ′E17/P17 devices. One adapter socket (part number RTC/PGM320C-06), shown in Figure 19, converts a 40-pin DIP into an equivalent 28-pin device. Another socket (part number RTC/PGM320C-06), not shown, permits 44- to 28-pin conversion.

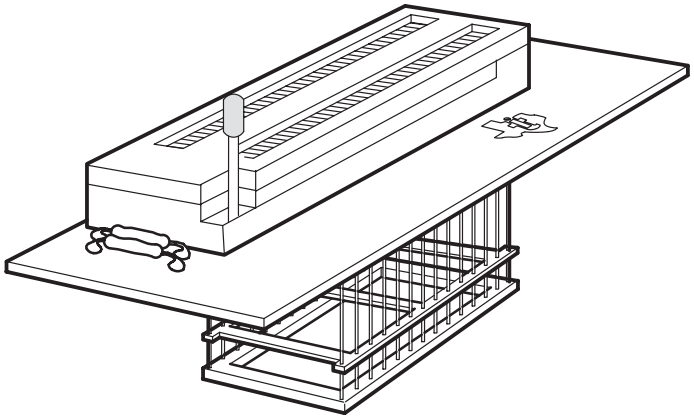
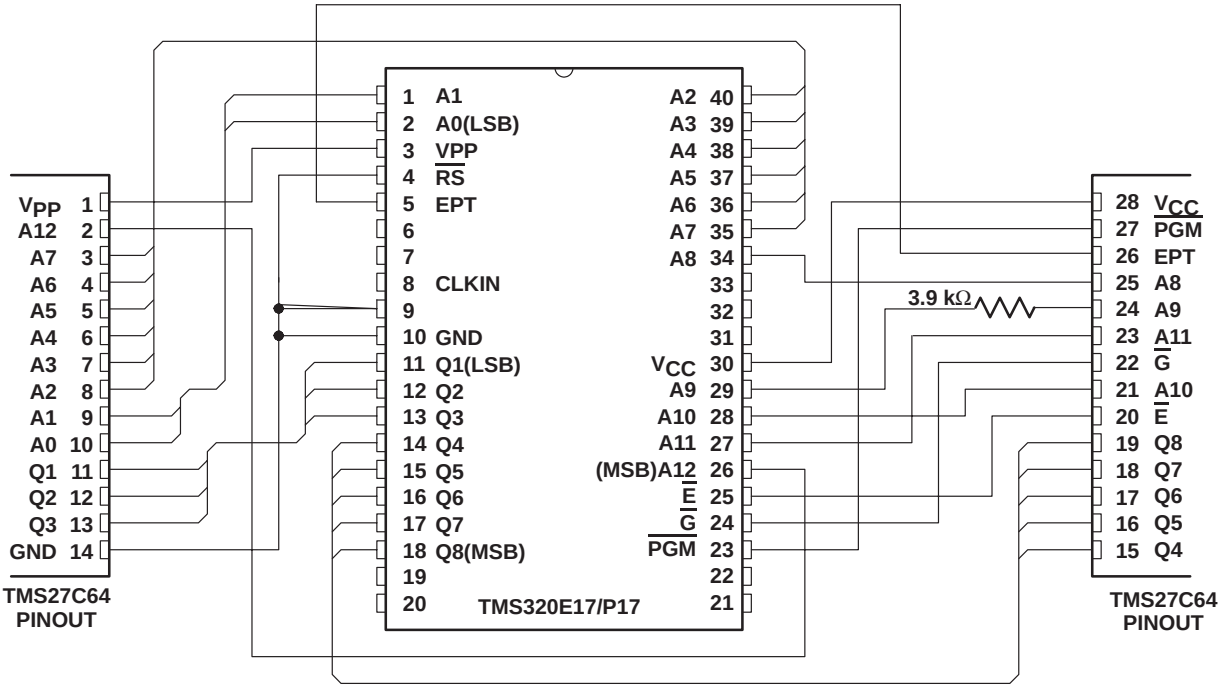


Figure 19. EPROM Adapter Socket (40-Pin to 28-Pin DIP Conversion)

Key features of the EPROM cell include the normal programming operation as well as verification. The EPROM cell also includes a code protection feature that allows code to be protected against copyright violations.

The ′E17/P17 EPROM cell is programmed using the same family and device pinout codes as the TMS27C64 8K × 8-bit EPROM. The TMS27C64 EPROM series are unltraviolet-light erasable, electrically programmable, read-only memories, fabricated using HVCMOS technology. They are pin-compatible with existing 28-pin ROMs and EPROMs. These EPROMs operate from a single 5-V supply in the read mode; however, a 12.5-V supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

Figure 20 shows the wiring conversion to program the ′E17/P17 using the 28-pin pinout of the TMS27C64. Table 8 on pin nomenclature provides a description of the TMS27C64 pins. The code to be programmed into the device should be in serial mode. The ′E17/P17 devices use 13 address lines to address 4K-word memory in byte format.



CAUTION

Although acceptable by some EPROM programmers, the signature mode cannot be used on any TMS320E1x device. The signature mode will input a high-level voltage (12.5 V_{dc}) onto pin A9. Since this pin is not designed for high voltage, the cell will be damaged. To prevent an accidental application of voltage, Texas Instruments has inserted a 3.9 kΩ resistor between pin A9 of the TI programmer socket and the programmer itself.

Pin Nomenclature (TMS320E17/P17)

NAME	I/O	DEFINITION
A0-A12	I	On-chip EPROM programming address lines
CLKIN	I	Clock oscillator input
$\overline{E}$	I	EPROM chip select
EPT	I	EPROM test mode select
$\overline{G}$	I	EPROM read/verify select
GND	I	Ground
$\overline{PGM}$	I	EPROM write/program select
Q1-Q8	I/O	Data lines for byte-wide programming of on-chip 8K bytes of EPROM
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	5-V power supply
V_{PP}	I	12.5-V power supply

Figure 20. TMS320E17/P17 EPROM Programming Conversion to TMS27C64 EPROM Pinout

Table 8 shows the programming levels required for programming, verifying, reading, and protecting the EPROM cell.

Table 8. TMS320E17/P17 Programming Mode Levels

SIGNAL NAME	TMS320E17 PIN	TMS27C64 PIN	PROGRAM	VERIFY	READ	PROTECT VERIFY	EPROM PROTECT
$\overline{E}$	25	20	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$	24	22	V_{IH}	$\overline{PULSE}$	$\overline{PULSE}$	V_{IL}	V_{IH}
$\overline{PGM}$	23	27	$\overline{PULSE}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}
V_{PP}	3	1	V_{PP}	V_{PP}	V_{CC}	V_{CC} + 1	V_{PP}
V_{CC}	30	28	V_{CC}	V_{CC}	V_{CC}	V_{CC} + 1	V_{CC} + 1
V_{SS}	10	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
CLKIN	8	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
$\overline{RS}$	4	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
EPT	5	26	V_{SS}	V_{SS}	V_{SS}	V_{PP}	V_{PP}
Q1-Q8	11-18	11-13, 15-19	D_{IN}	Q_{OUT}	Q_{OUT}	Q8=RBIT	Q8=$\overline{PULSE}$
A0-A3	2, 1, 40, 39	10-7	ADDR	ADDR	ADDR	X	X
A4	38	6	ADDR	ADDR	ADDR	X	V_{IH}
A5	37	5	ADDR	ADDR	ADDR	X	X
A6	36	4	ADDR	ADDR	ADDR	V_{IL}	X
A7-A9	35, 34, 29	3, 25, 24	ADDR	ADDR	ADDR	X	X
A10-A12	28-26	21, 23, 2	ADDR	ADDR	ADDR	X	X

Legend:

V_{IH} = TTL high level; V_{IL} = TTL low level; ADDR = byte address bit
V_{PP} = 12.5 V ± 0.25 V; V_{CC} = 5 V ± 0.25 V; X = don't care
$\overline{PULSE}$ = low-going TTL level pulse; D_{IN} = byte to be programmed at ADDR
Q_{OUT} = byte stored at ADDR; RBIT = ROM protect bit.

programming

Since every memory bit in the cell is a logic 1, the programming operation reprograms certain bits to 0. Once programmed, these bits can be erased only by using ultraviolet light. The correct byte is placed on the data bus with V_{PP} set to the 12.5 V level. The $\overline{PGM}$ pin is then pulsed low to program in the zeroes.

erasure

Before programming, the device must be erased by exposing it to ultraviolet light. The recommended minimum exposure dose (UV-intensity × exposure-time) is 15 W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After exposure, all bits are in the high state.

verify/read

To verify correct programming, the EPROM cell can be read using either the verify or read line definitions shown in Table 8 assuming the inhibit bit has not been programmed.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

read

The EPROM contents may be read independent of the programming cycle, provided the RBIT (ROM protect bit) has not been programmed. The read is accomplished by setting $\overline{E}$ to zero and pulsing $\overline{G}$ low. The contents of the EPROM location selected by the value on the address inputs appear on Q8-Q1.

output disable

During the EPROM programming process, the EPROM data outputs may be disabled, if desired, by establishing the output disable state. This state is selected by setting $\overline{G}$ and $\overline{E}$ pins high. While output disable is selected, Q8-Q1are placed in the high-impedance state.

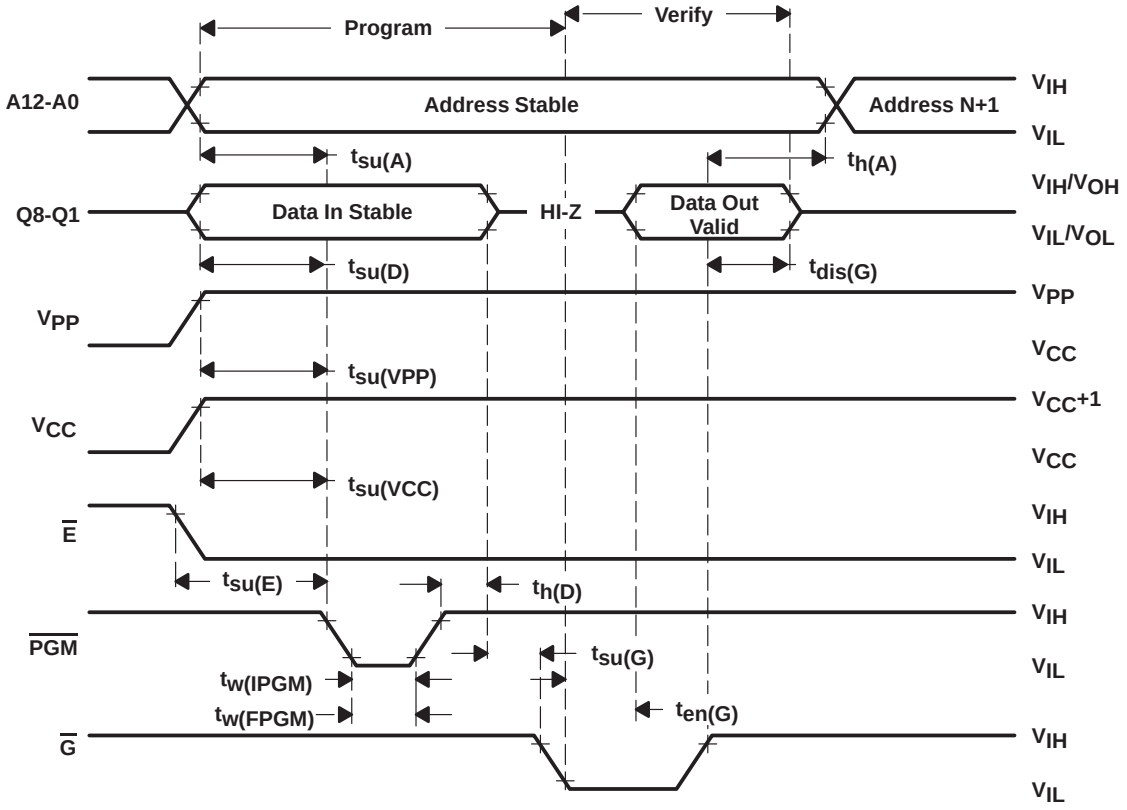
EPROM protection

To protect the proprietary algorithms existing in the code programmed on-chip, the ability to read or verify code from external accesses can be completely disabled. Programming the RBIT disables external access of the EPROM cell, making it impossible to access the code resident in the EPROM cell. The only way to remove this protection is to erase the entire EPROM cell, thus removing the proprietary information. The signal requirements for programming this bit are shown in Table 8. The cell can be determined as protected by verifying the programming of the RBIT shown in the table.

standard programming procedure

Before programming, the device must first be completely erased. The device can then be programmed with the correct code. It is advisable to program unused sections with zeroes as a further security measure. After the programming is complete, the code programmed into the cell should be verified. If the cell passes verification, the next step is to program the ROM protect bit (RBIT). Once the RBIT programming is verified, an opaque label should be placed over the window to protect the EPROM cell from inadvertent erasure by ambient light. At this point, the programming is complete, and the device is ready to be placed into its destination circuit.

program cycle timing



absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 6) . . . . . –0.3 V to 4.6 V
Input voltage range . . . . . –0.3 V to V_{CC} to 0.5 V
Output voltage range . . . . . –0.3 V to V_{CC} to 0.5 V
Continuous power dissipation . . . . . 75 mW
Air temperature range above operating devices: L version . . . . . 0°C to 70°C
A version . . . . . –40°C to 85°C
Storage temperature range . . . . . –55°C to +150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2.0			V
		CLKIN	2.5			V
V_{IL}	Low-level input voltage	All inputs			0.55	V
I_{OH}	High-level output current (all outputs)				–300	µA
I_{OL}	Low-level output current (all outputs)				1.5	mA
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C

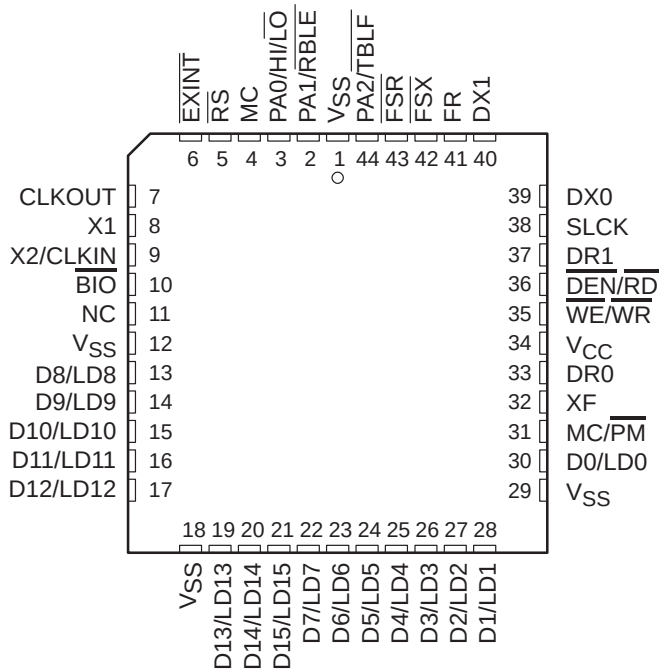
electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX	2.0			V
			I_{OH} = 20 µA (see Note 19)	V_{CC}–0.4¶			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.5	V
I_{OZ}	Off-state ouput current		V_{CC} = MAX, V_O = V_{CC}			20	µA
			V_O = V_{SS}			–20	
I_I	Input current		V_I = V_{SS} to V_{CC}, All inputs except CLKIN			±20	µA
			V_I = V_{SS} to V_{CC}, CLKIN			±50	
C_i	Input capacitance	Data bus	f = 1 MHz, All other pins 0 V		25¶		pF
		All others			15¶		
C_o	Output capacitance	Data bus			25¶		pF
		All others			10¶		

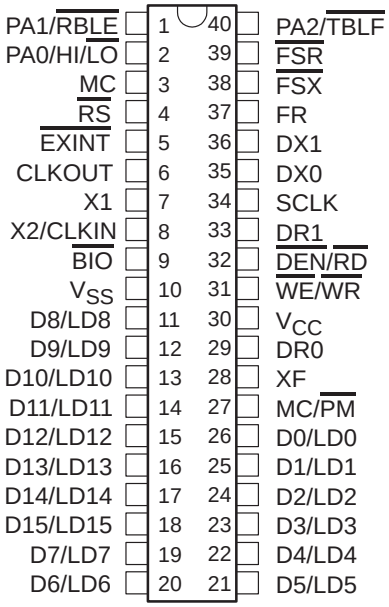
§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
¶ Values derived from characterization data and not tested.

NOTE 19: This voltage specification is included for interface to HC logic. All other timing parameters defined in this data sheet are specified for the test load circuit shown in Figure 2.

**TMS320LC17
FN PACKAGE
(TOP VIEW)**



**TMS320LC17
N PACKAGE
(TOP VIEW)**



electrical characteristics over specified ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡	Supply current	f = 14.4 MHz, V_{CC} = 3.6 V, T_A = 0°C to 70°C		15	20	mA

† All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡ I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependence on frequency, see Figure 3.

clock characteristics and timing

The TMS320LC17 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency f_X	T_A = – 40°C to 85°C	4.0		14.4	MHz
C1, C2			10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time§	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	277.78		1000	ns
$t_{r(C)}$	CLKOUT rise time			10¶		ns
$t_{f(C)}$	CLKOUT fall time			8¶		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			131		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			129		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓		25		75	ns

§ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
¶ Values derived from characterization data and not tested

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	69.5		150	ns
$t_{r(MC)}$	Rise time, master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time, master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration, master clock	$0.4t_{c(MC)}$†		$0.6t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration, master clock low at $t_{c(MC)}$ min		30		ns
$t_{w(MCH)}$	Pulse duration, master clock high at $t_{c(MC)}$ min		30		ns

† Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	10†	100	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		$1/4\ t_{c(C)}-5$†	$1/4\ t_{c(C)}+25$	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		–10†	30	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		$1/2\ t_{c(C)}-5$†	$1/2\ t_{c(C)}+25$	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		–10†	30	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid			$1/4\ t_{c(C)}+130$	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$1/4\ t_{c(C)}-5$†		ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven			$1/4\ t_{c(C)}+90$	ns
t_v	Data bus OUT valid after CLKOUT↓		$1/4\ t_{c(C)}-10$		ns
$t_{h(A\text{-}WMD)}$	Address hold time after WE↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 14)		0†		ns
$t_{su(A\text{-}MD)}$	Address bus setup time or $\overline{DEN}$↓		0		ns

† Values derived from characterization data and not tested.
NOTE 14: Address bus will be valid upon $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	80			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↓ (see Note 9)		0			ns

NOTE 9: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{d11}	Delay time $\overline{DEN}$↑, $\overline{WE}$↑, and $\overline{MEN}$↑ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)			$1/2t_{c(C)}$+75	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$1/4t_{c(C)}$+75	ns
t_{d12}	Delay time from $\overline{RS}$↓ to high-impedance SCLK				200†	ns
t_{d13}	Delay time from $\overline{RS}$↓ to high-impedance DX1, DX0				200†	ns

† These values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 10)	85			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

NOTE 10: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{EXINT}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(INT)}$	Fall time $\overline{EXINT}$			15	ns
$t_{w(INT)}$	Pulse duration $\overline{EXINT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{EXINT}$↓ before CLKOUT↓	85			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(IO)}$	Fall time $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	85			ns

I/O ($\overline{BIO}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{d(XF)}$	Delay time CLKOUT↓ to valid XF	R_L = 825 Ω, C_L = 100 pF, (see Figure 2)	5†		115	ns

† Values derived from characterization data and not tested.

SERIAL PORT TIMING

switching characteristics over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{d(CH-FR)}$	Internal framing (FR) delay from SCLK rising edge			120	ns
$t_{d(DX1-CL)}$	DX bit 1 valid before SCLK falling edge	20			ns
$t_{d(DX2-CL)}$	DX bit 2 valid before SCLK falling edge	20			ns
$t_{h(DX)}$	DX hold time after SCLK falling edge	$t_{c(SCLK)}/2$			ns

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(SCLK)}$	Serial port clock (SCLK) cycle time‡	555		8000	ns
$t_{f(SCLK)}$	Serial port clock (SCLK) fall time			30†	ns
$t_{r(SCLK)}$	Serial port clock (SCLK) rise time			30†	ns
$t_{w(SCLK)}$	Serial port clock (SCLK) low, pulse duration§	250		4400	ns
$t_{w(SCLKH)}$	Serial port clock (SCLK) high, pulse duration§	250		4400	ns
$t_{su(FS)}$	$\overline{FSX}$/$\overline{FSR}$ setup time before SCLK falling edge	130			ns
$t_{su(DR)}$	DR setup time before SCLK falling edge	20			ns
$t_{h(DR)}$	DR hold time after SCLK falling edge	20			ns

† Values derived from characterization data and not tested.
‡ Minimum cycle time is $2t_{c(C)}$ where $t_{c(C)}$ is CLKOUT cycle time.
§ The duty cycle of the serial port clock must be within 45 to 55%.

COPROCESSOR INTERFACE TIMING

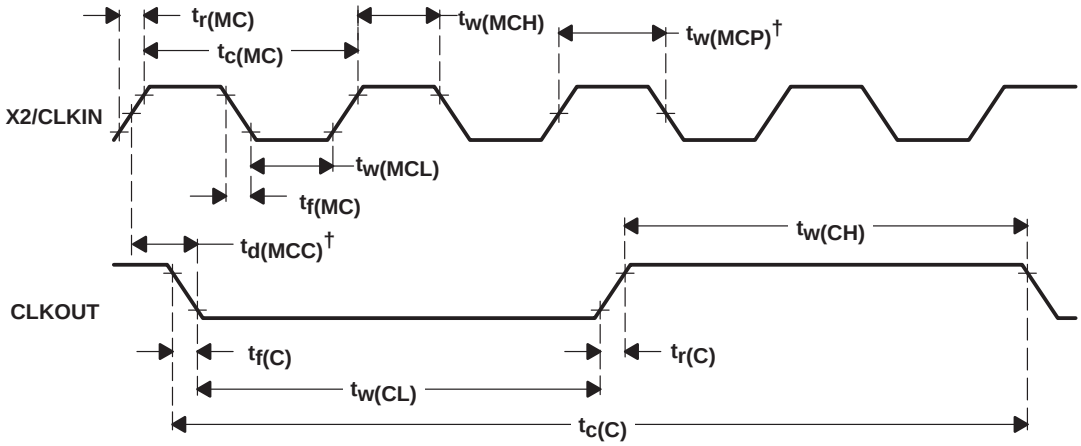
switching characteristics over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{d(R-A)}$	$\overline{RD}$ low to $\overline{TBLF}$ high			150	ns
$t_{d(W-A)}$	$\overline{WR}$ low to $\overline{RBLF}$ high			150	ns
$t_{a(RD)}$	$\overline{RD}$ low to data valid			150	ns
$t_{h(RD)}$	Data hold time after $\overline{RD}$ high	25			

timing requirements over recommended operating conditions

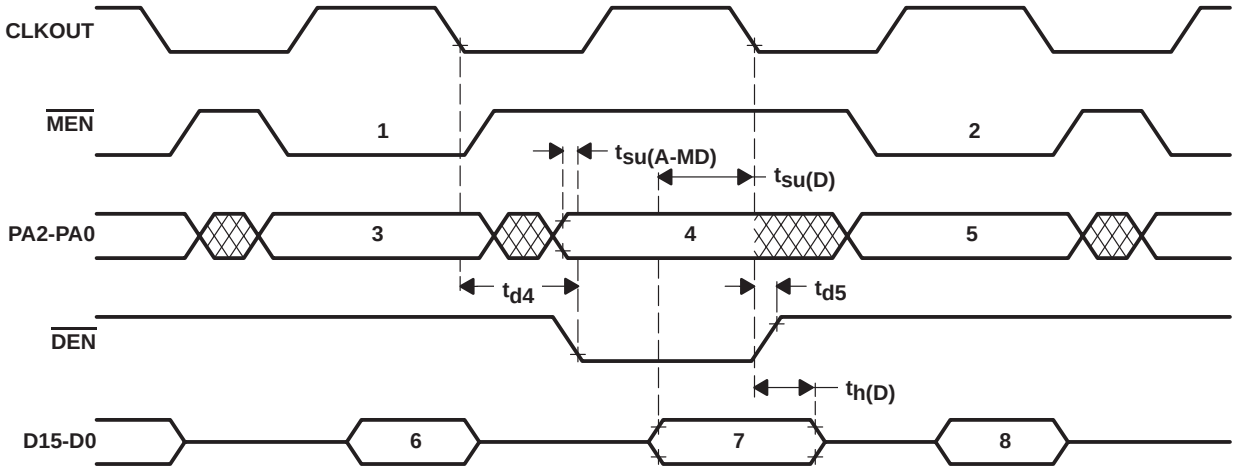
		MIN	NOM	MAX	UNIT
$t_{h(HL)}$	HI/$\overline{RD}$ hold time after $\overline{WR}$ or $\overline{RD}$ high	25			ns
$t_{su(HL)}$	HI/$\overline{RD}$ setup time prior to $\overline{WR}$ or $\overline{RD}$ low	40			ns
$t_{su(WR)}$	Data setup time prior to $\overline{WR}$ high	50			ns
$t_{h(WR)}$	Data hold time after $\overline{WR}$ high	35			ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low	150			ns
$t_{w(WRL)}$	Pulse duration, $\overline{WR}$ low	150			ns

clock timing



† $t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

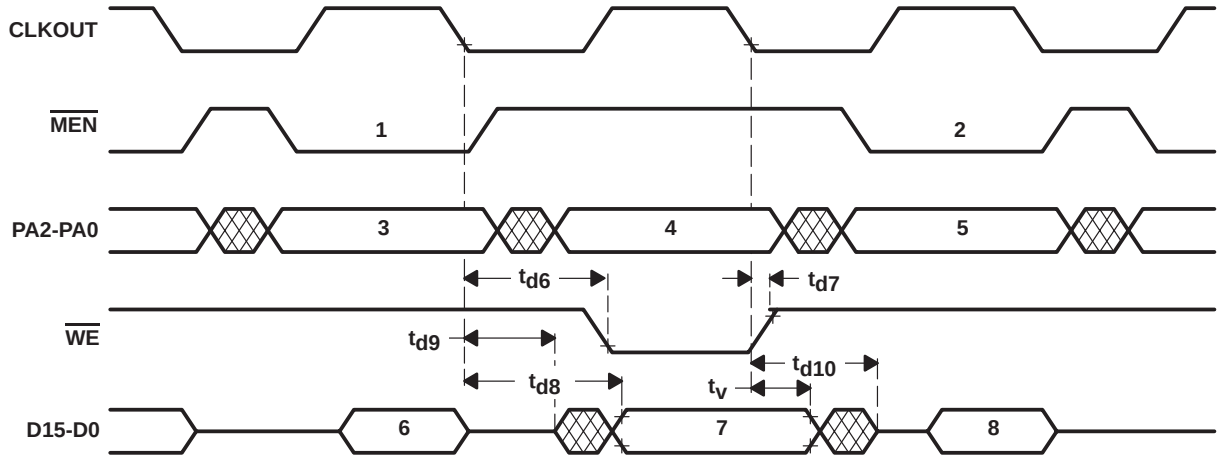
IN instruction timing



Legend:

1. IN Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Input Valid
8. Instruction Valid

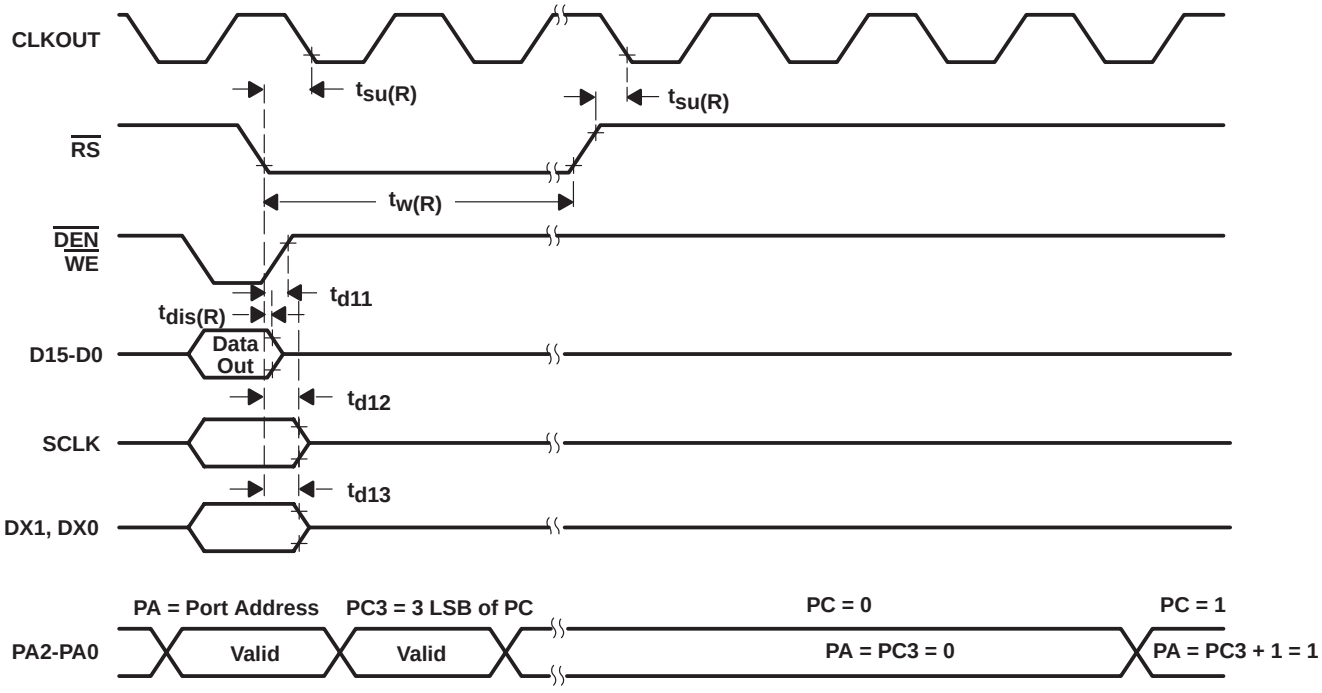
OUT instruction timing



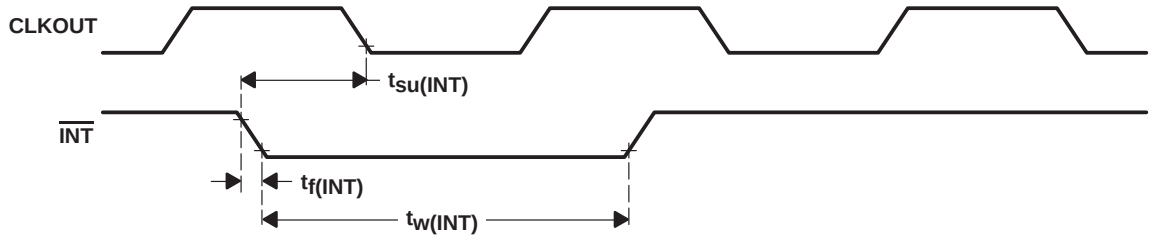
Legend:

1. OUT Instruction Prefetch
2. Next Instruction Prefetch
3. Address Bus Valid
4. Peripheral Address Valid
5. Address Bus Valid
6. Instruction Valid
7. Data Output Valid
8. Instruction Valid

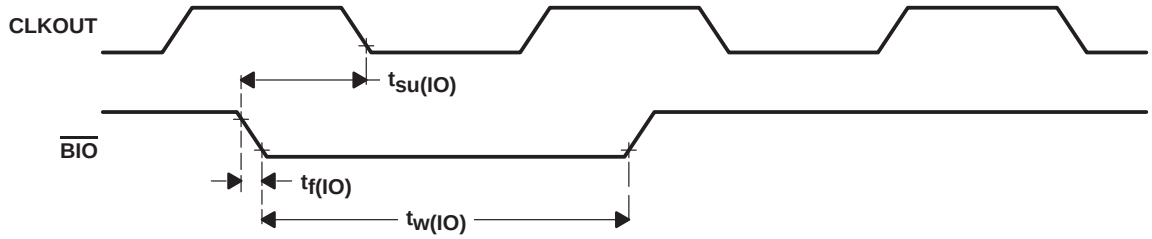
reset timing



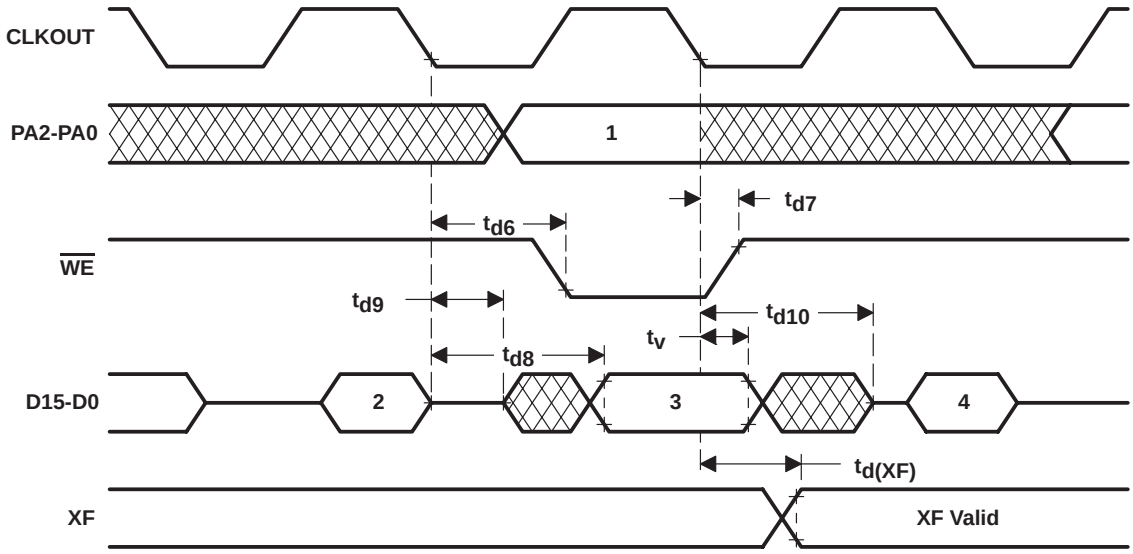
interrupt timing



$\overline{BIO}$ timing



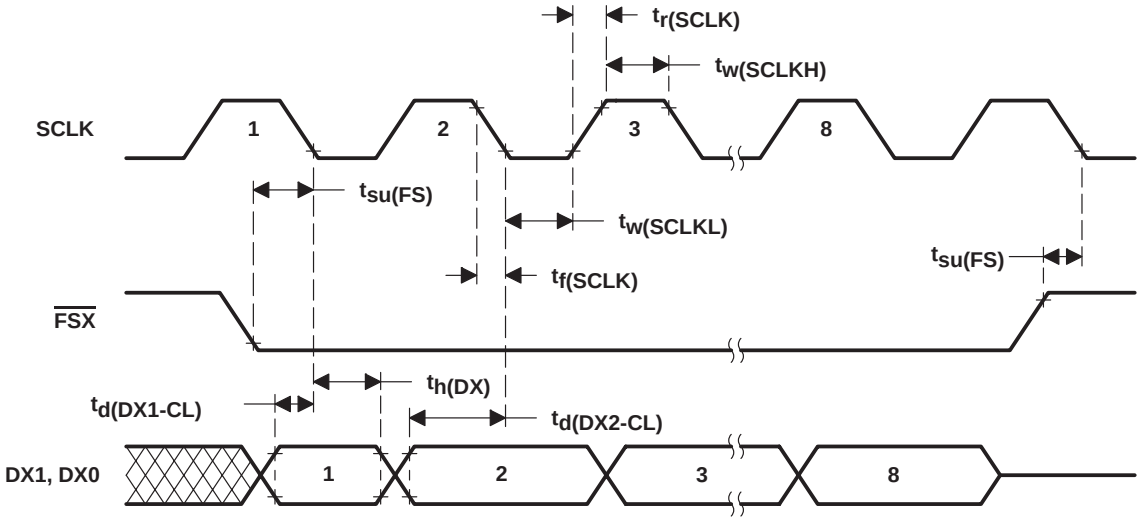
XF timing



Legend:

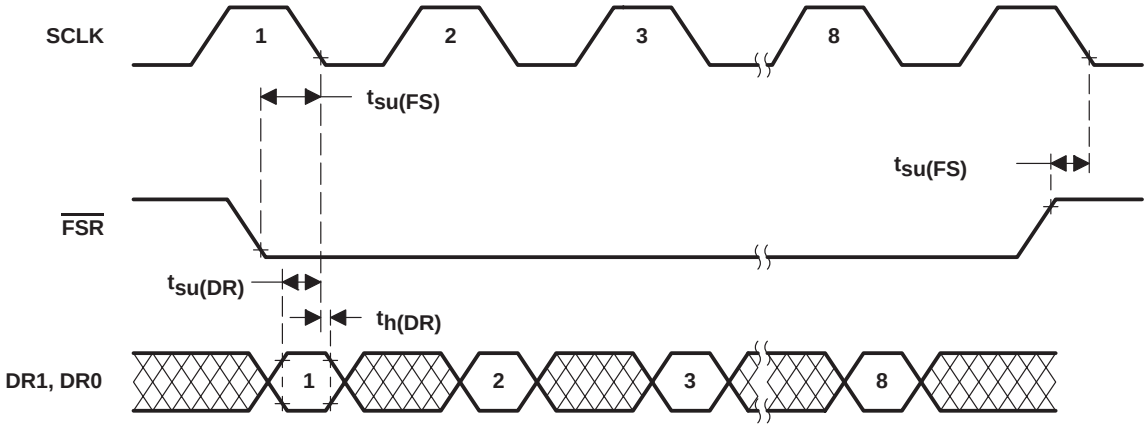
1. Port Address Valid
2. Out Opcode Valid
3. Port Data Valid
4. Next Instruction Opcode Valid

external framing: transmit timing



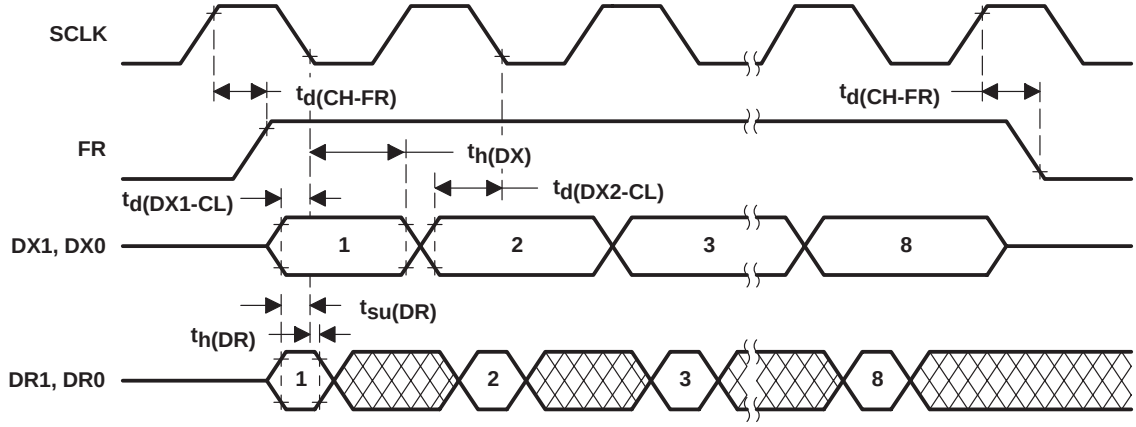
NOTES: A. Data valid on transmit output until SCLK rises.
B. The most significant bit is shifted first.

external framing: receive timing



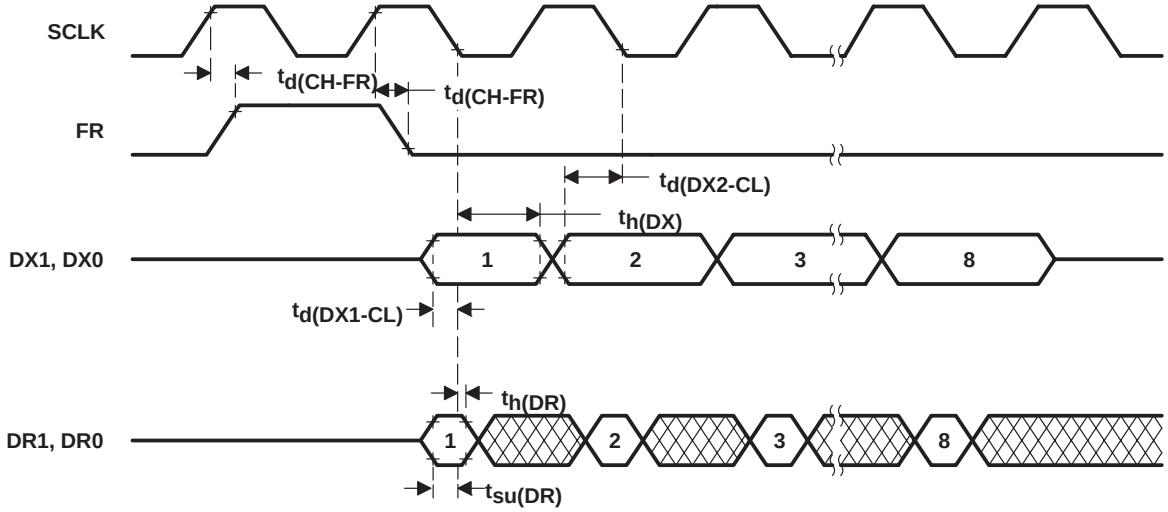
NOTE B: The most significant bit is shifted first.

internal framing: variable-data rate



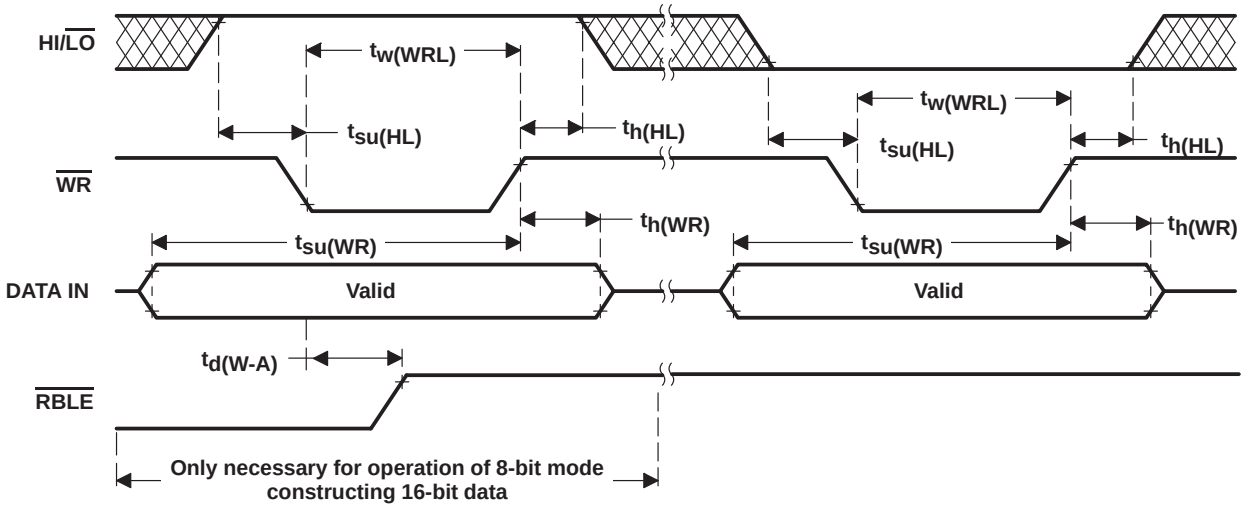
NOTE: The most significant bit is shifted first.

internal framing: fixed-data rate

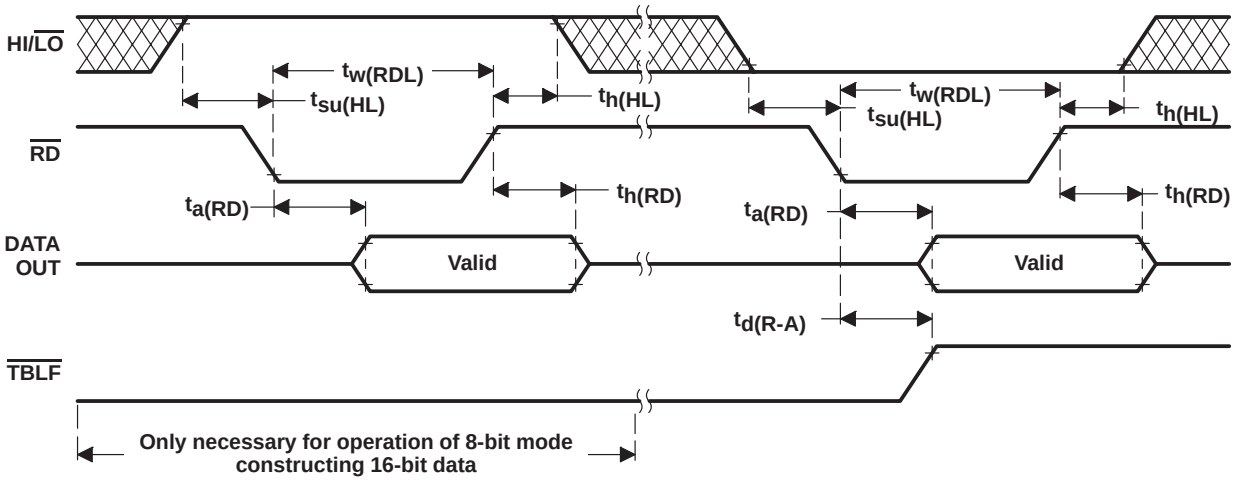


NOTE: The most significant bit is shifted first.

coprocessor timing: external write to coprocessor port



coprocessor timing: external read to coprocessor port



THERMAL RESISTANCE CHARACTERISTICS

Commercial Devices
Device/Package Thermal Resistance
Junction To Case

DEVICE	$R_{\theta JC}$ (°C/W)				
	PDIP (N)	CDIP (JD)	PLCC (FN)	CLCC (FZ)	QFP (PG)
TMS320C10	26		17		
TMS320C10-14	26		17		
TMS320C10-25	26		17		
TMS320C14			11		
TMS320E14				8	
TMS320P14			11		
TMS320C15	26		17		
TMS320C15-25	26		17		
TMS320E15		8		8	
TMS320E15-25		8		8	
TMS320LC15	26		17		
TMS320P15	13		13		
TMS320C16					25
TMS320C17	26		17		
TMS320E17		8		8	
TMS320LC17	26		17		
TMS320P17	13		13		

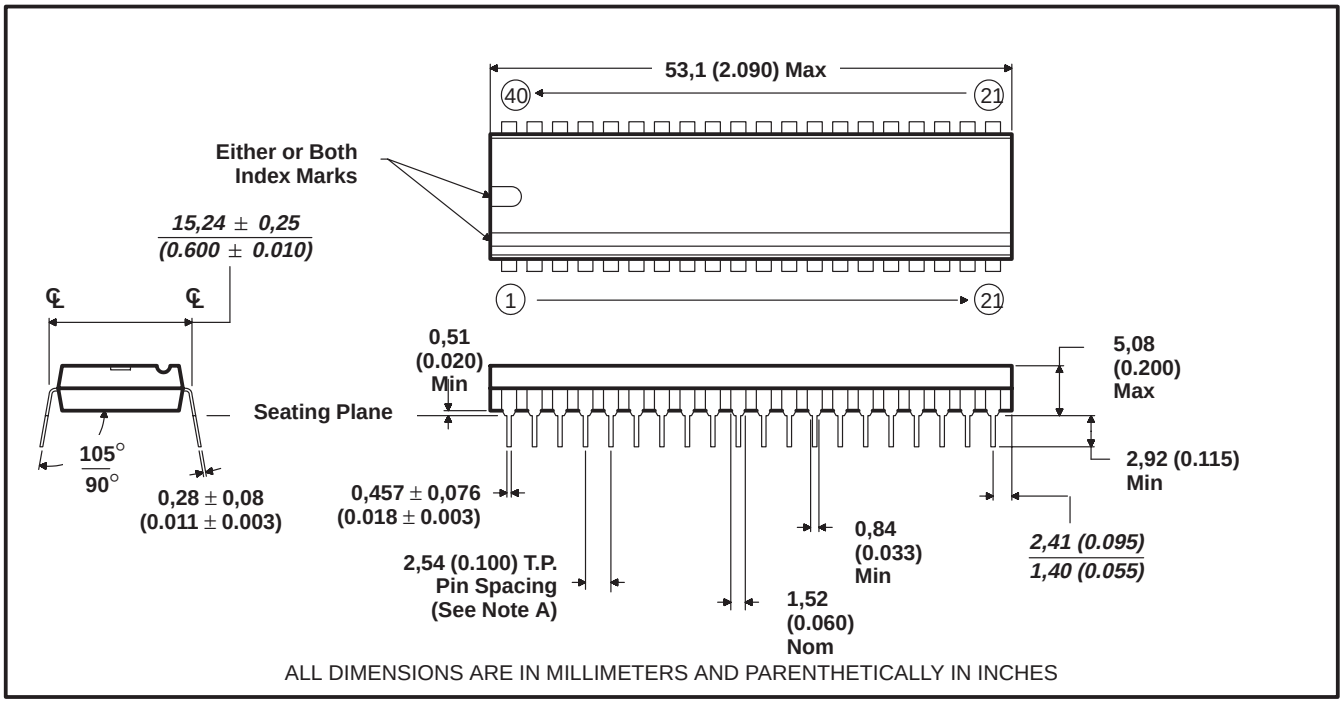
THERMAL RESISTANCE CHARACTERISTICS

Commercial Devices
Device/Package Thermal Resistance
Junction To Ambient

DEVICE	$R_{\theta JA}$ (°C/W)				
	PDIP (N)	CDIP (JD)	PLCC (FN)	CLCC (FZ)	QFP (PG)
TMS320C10	84		60		
TMS320C10-14	84		60		
TMS320C10-25	84		60		
TMS320C14			46		
TMS320E14				49	
TMS320P14			46		
TMS320C15	84		60		
TMS320C15-25	84		60		
TMS320E15		40		64	
TMS320E15-25		40		64	
TMS320LC15	84		60		
TMS320P15	40		55		
TMS320C16					120
TMS320C17	84		60		
TMS320E17		40		64	
TMS320LC17	84		60		
TMS320P17	40		55		

MECHANICAL DATA

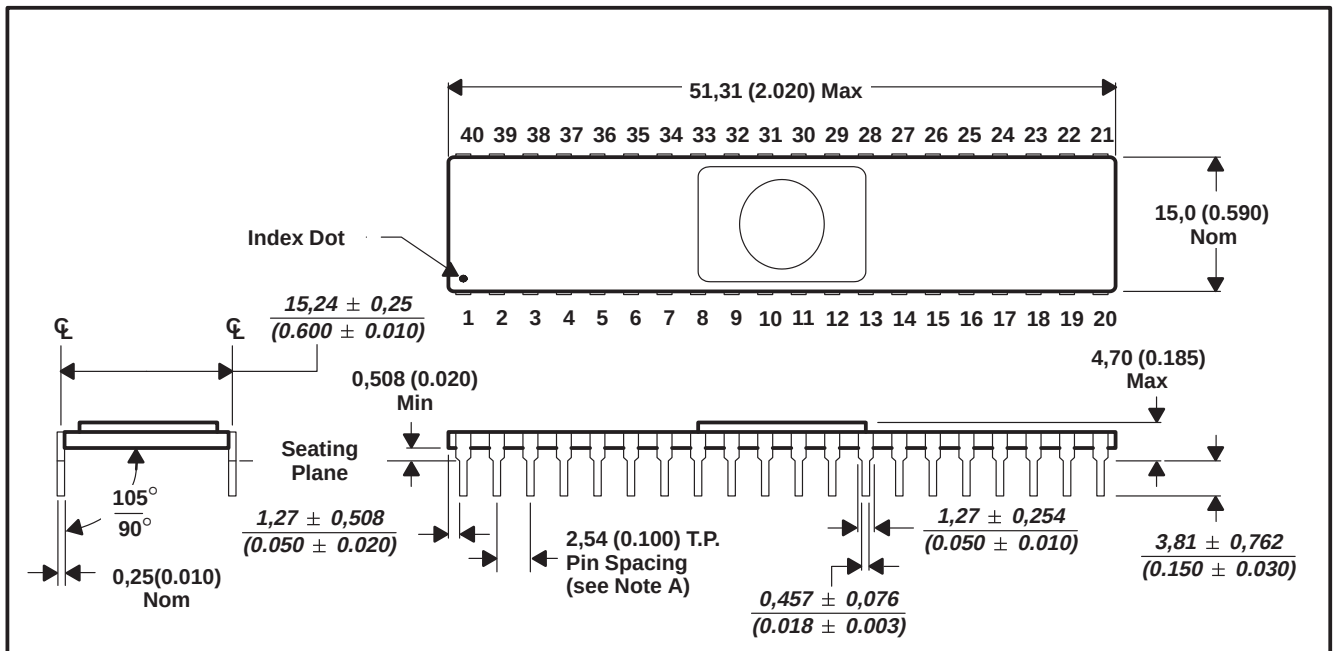
40-pin plastic dual-in-line package



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

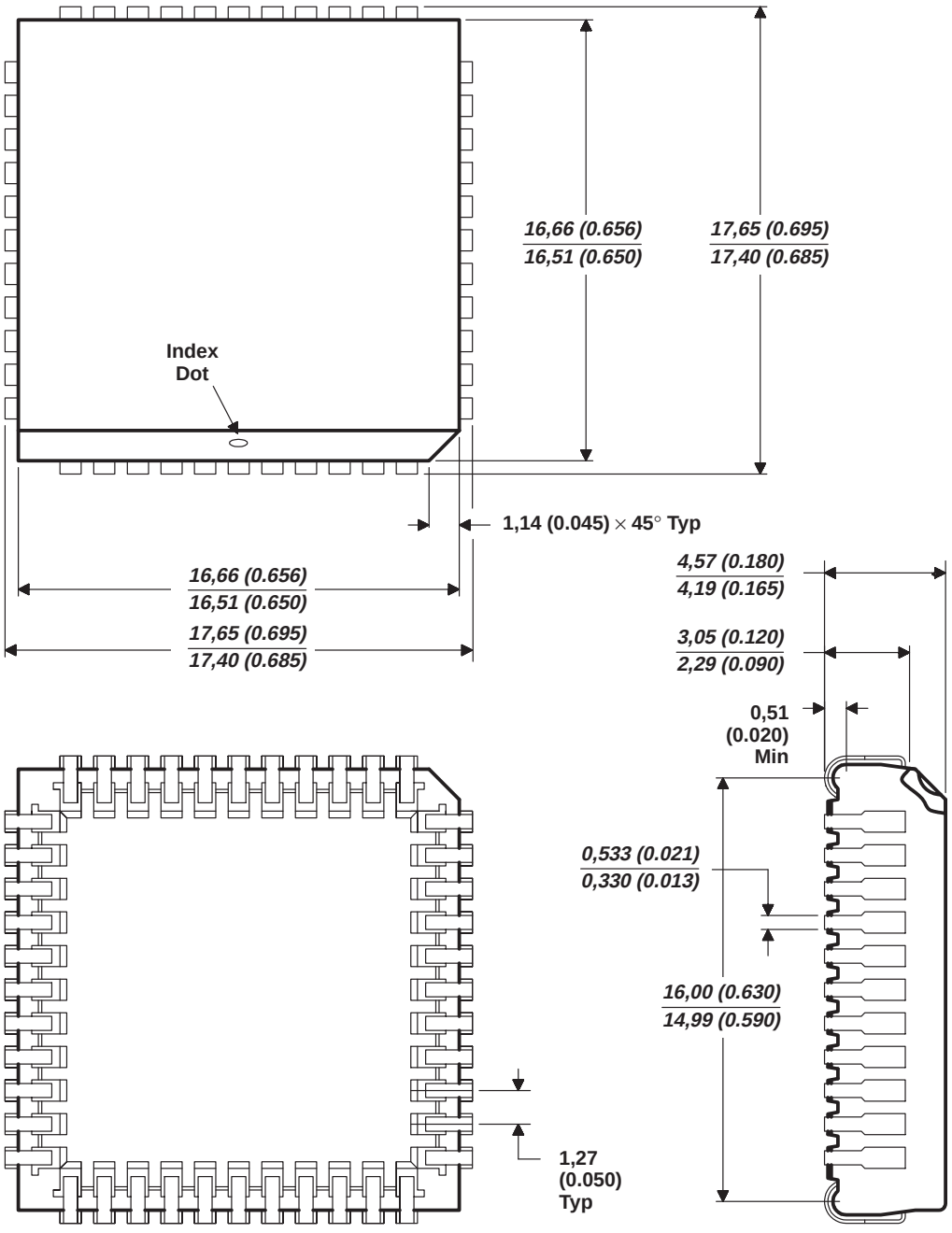
40-pin windowed ceramic dual-in-line package



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

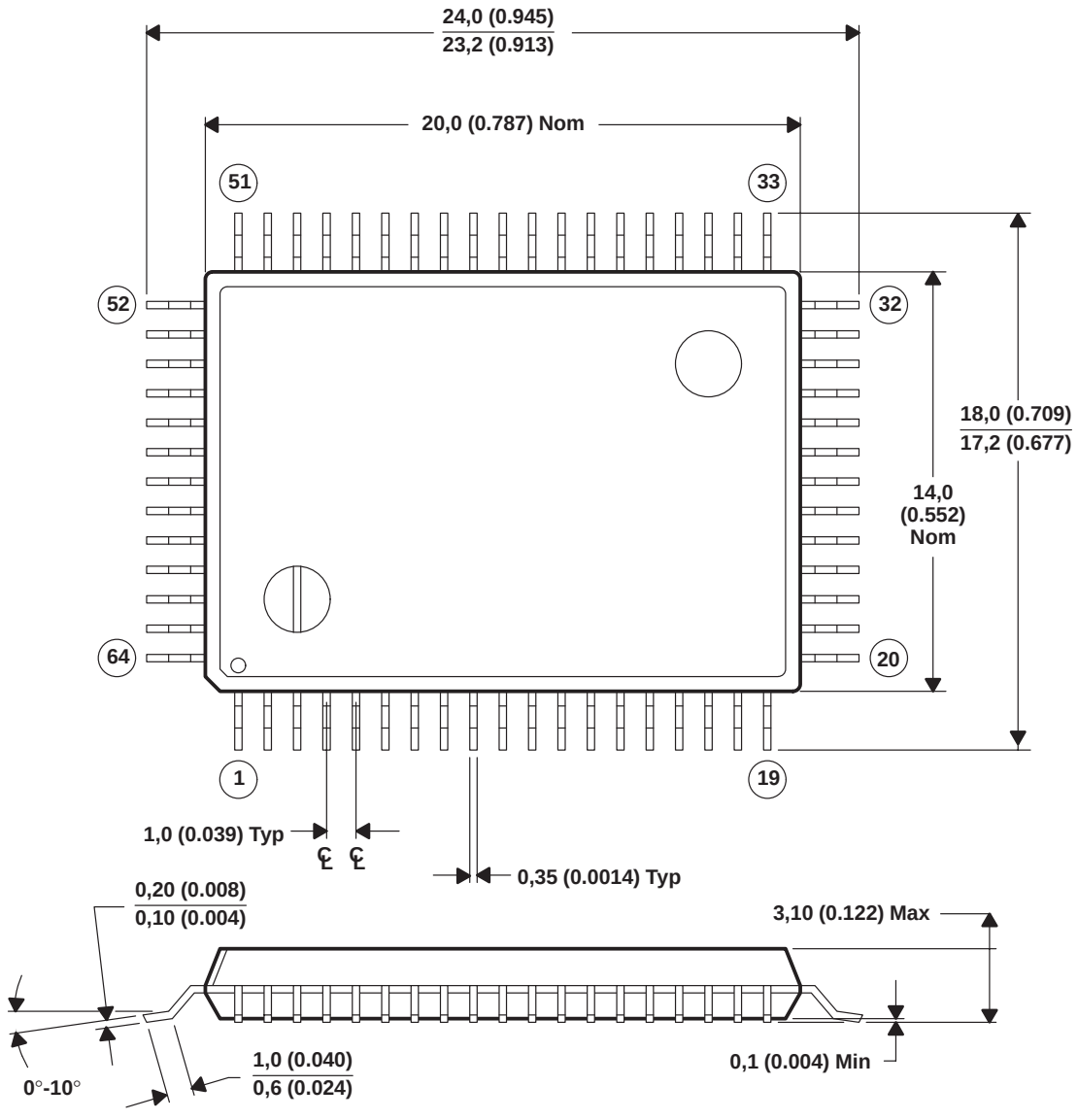
NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

44-lead plastic chip carrier (FN suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

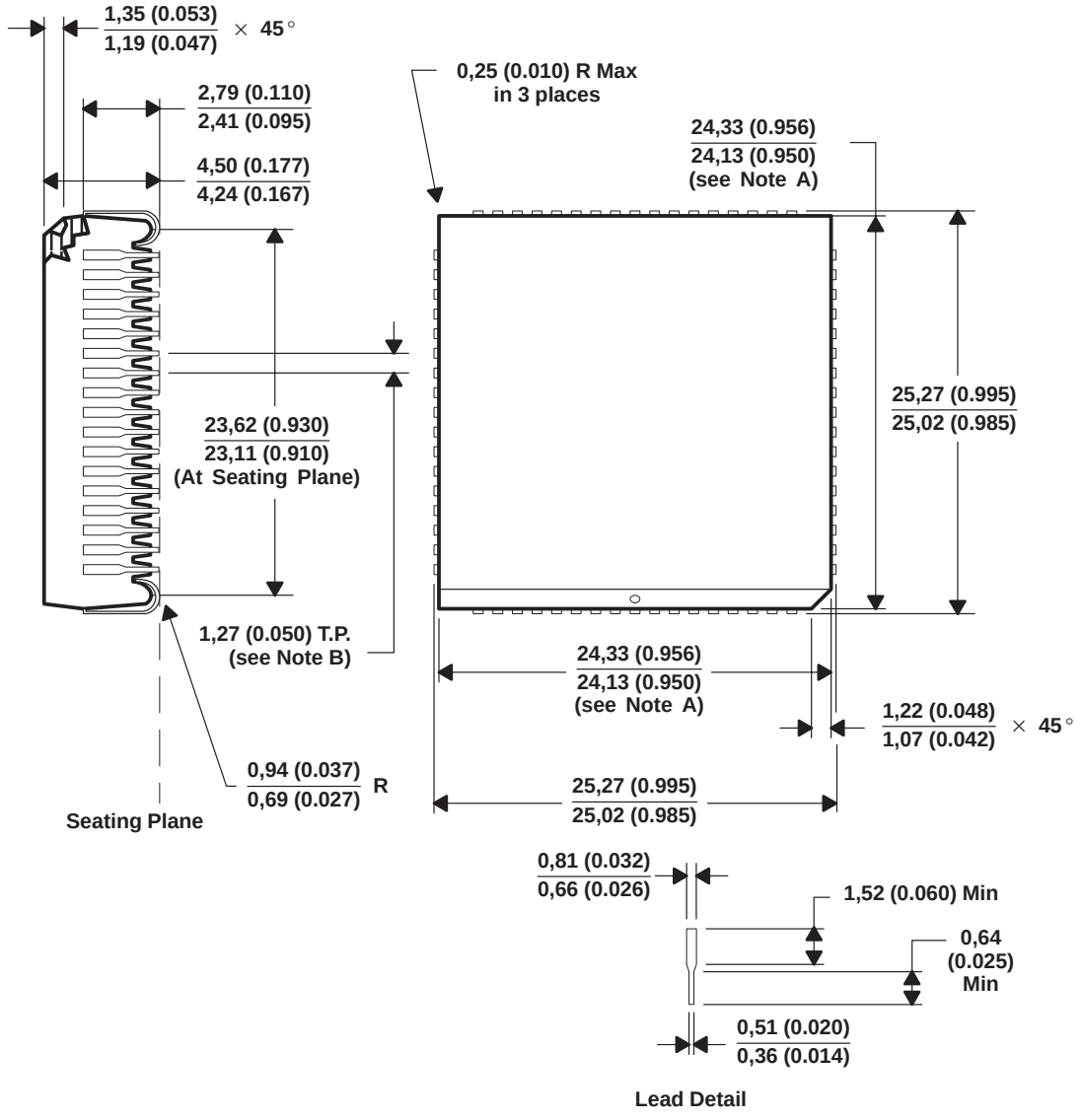
64-pin quad flat pack (PG suffix) (TMS320C16)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

68-lead plastic chip carrier package (FN suffix)

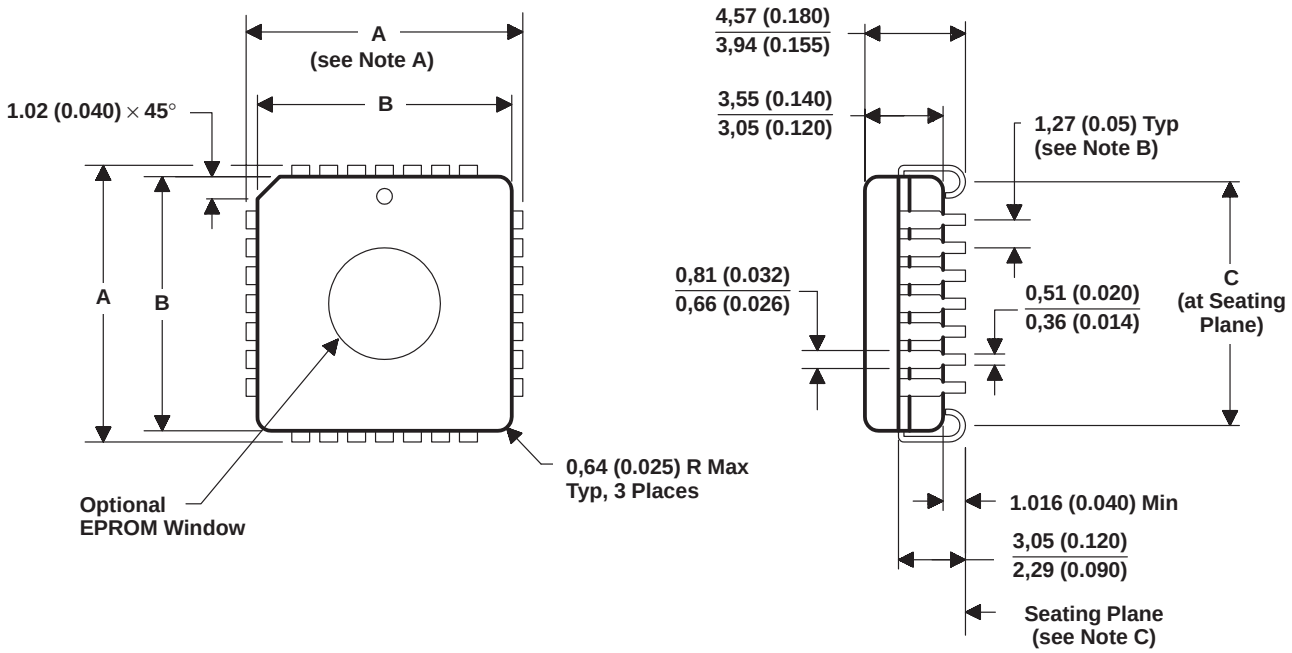


NOTES: A. Centerline of center pin, each side, is within 0,10 (0.004) of package centerline as determined by this deminsion.
B. Location of each pin is within 0,27 (0.005) of true position with respect to center pin on each side.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

68-lead ceramic chip carrier package (FZ suffix)



		A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
M0-087AA	28	12,32 (0.485)	12,57 (0.495)	10,92 (0.430)	11,56 (0.455)	10,41 (0.410)	10.92 (0.430)
M0-087AB	44	17,40 (0.685)	17,65 (0.695)	16,00 (0.630)	16,64 (0.655)	15,49 0.610)	16,00 (0.630)
M0-087AD	68	25,02 (0.985)	25,27 (0.995)	23,62 (0.930)	24,26 (0.955)	23.11 (0.910)	23,62 (0.930)

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,27 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,15 (0.006)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8763308QA	OBSOLETE	CDIP SB	JD	40		TBD	Call TI	Call TI	-55 to 125	5962-8763308QA SMJ320C15-25JD M	
5962-8763308YA	OBSOLETE	JLCC	FJ	44		TBD	Call TI	Call TI	-55 to 125		
SMJ320C15-25FJM	OBSOLETE	JLCC	FJ	44		TBD	Call TI	Call TI	-55 to 125	5962-8763308YA SMJ320C15-25FJ M	
SMJ320C15-25JDM	OBSOLETE	CDIP SB	JD	40		TBD	Call TI	Call TI	-55 to 125	5962-8763308QA SMJ320C15-25JD M	
TMS320C10FNA	OBSOLETE			44		TBD	Call TI	Call TI			
TMS320C10FNL	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70	@1987 TI	
TMS320C10FNL25	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70	-25 @1987 TI TMS320C10FNL	
TMS320C10FNLR25	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI		-25 @1987 TI TMS320C10FNL	
TMS320C10NA	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI	-40 to 85	TMS320C10NA @1987 TI	
TMS320C10NL	NRND	PDIP	N	40		TBD	Call TI	Call TI	0 to 0	@1987 TI	
TMS320C10NL-25	NRND	PDIP	N	40		TBD	Call TI	Call TI	0 to 70	@1987 TI	
TMS320C10NL25	OBSOLETE			0		TBD	Call TI	Call TI	0 to 0		
TMS320C14FNL	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI	0 to 70	@1991 TI TMS320C14FNL	
TMS320C14FNLR	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI		@1991 TI TMS320C14FNL	
TMS320C15FNA	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	-40 to 85		
TMS320C15FNL	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320C15FNL25	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320C15NA	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI	-40 to 85		
TMS320C15NL	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI			
TMS320C15NL-25	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320C15NL25	OBSOLETE	PLCC	NL	40		TBD	Call TI	Call TI	0 to 0		
TMS320C15PEL	OBSOLETE	QFP	PE	44		TBD	Call TI	Call TI	0 to 70		
TMS320C16PGL	OBSOLETE	QFP	PG	64		TBD	Call TI	Call TI	0 to 70		
TMS320C17FNL	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320C17NL	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI			
TMS320LC15FNL	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320LC15NL	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI			
TMS320P14FNL	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI	0 to 70		
TMS320P14FNLG4	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI			
TMS320P15FNL	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320P15FNL25	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320P15NA	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI	-40 to 85		
TMS320P15NL	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI			
TMS320P15NL25	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI	0 to 70		
TMS320P17FNA	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	-40 to 85		
TMS320P17FNL	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320P17FNLR	OBSOLETE	PLCC	FN	44		TBD	Call TI	Call TI	0 to 70		
TMS320P17NL	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI			
TMS320SS16NL	OBSOLETE	PDIP	N	40		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SMJ320C15, TMS320C15 :

- Catalog: TMS320C15
- Military: SMJ320C15

NOTE: Qualified Version Definitions:

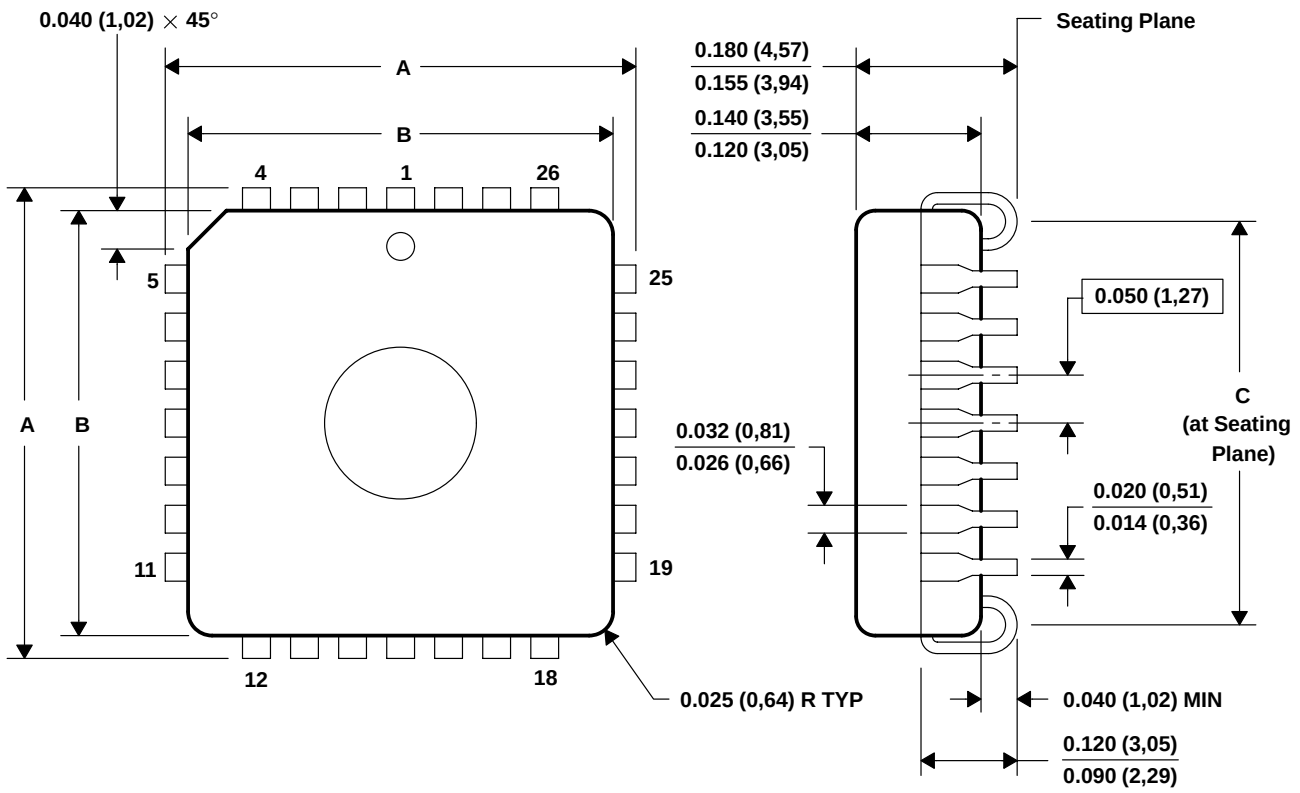
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

MJLC003A – FEBRUARY 1995

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



JEDEC OUTLINE	NO. OF PINS**	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	0.485 (12,32)	0.495 (12,57)	0.430 (10,92)	0.455 (11,56)	0.410 (10,41)	0.430 (10,92)
MO-087AB	44	0.685 (17,40)	0.695 (17,65)	0.630 (16,00)	0.655 (16,64)	0.610 (15,49)	0.630 (16,00)
MO-087AC	52	0.785 (19,94)	0.795 (20,19)	0.730 (18,54)	0.765 (19,43)	0.680 (17,28)	0.740 (18,79)
MO-087AD	68	0.985 (25,02)	0.995 (25,27)	0.930 (23,62)	0.955 (24,26)	0.910 (23,11)	0.930 (23,62)

4040219/B 03/95

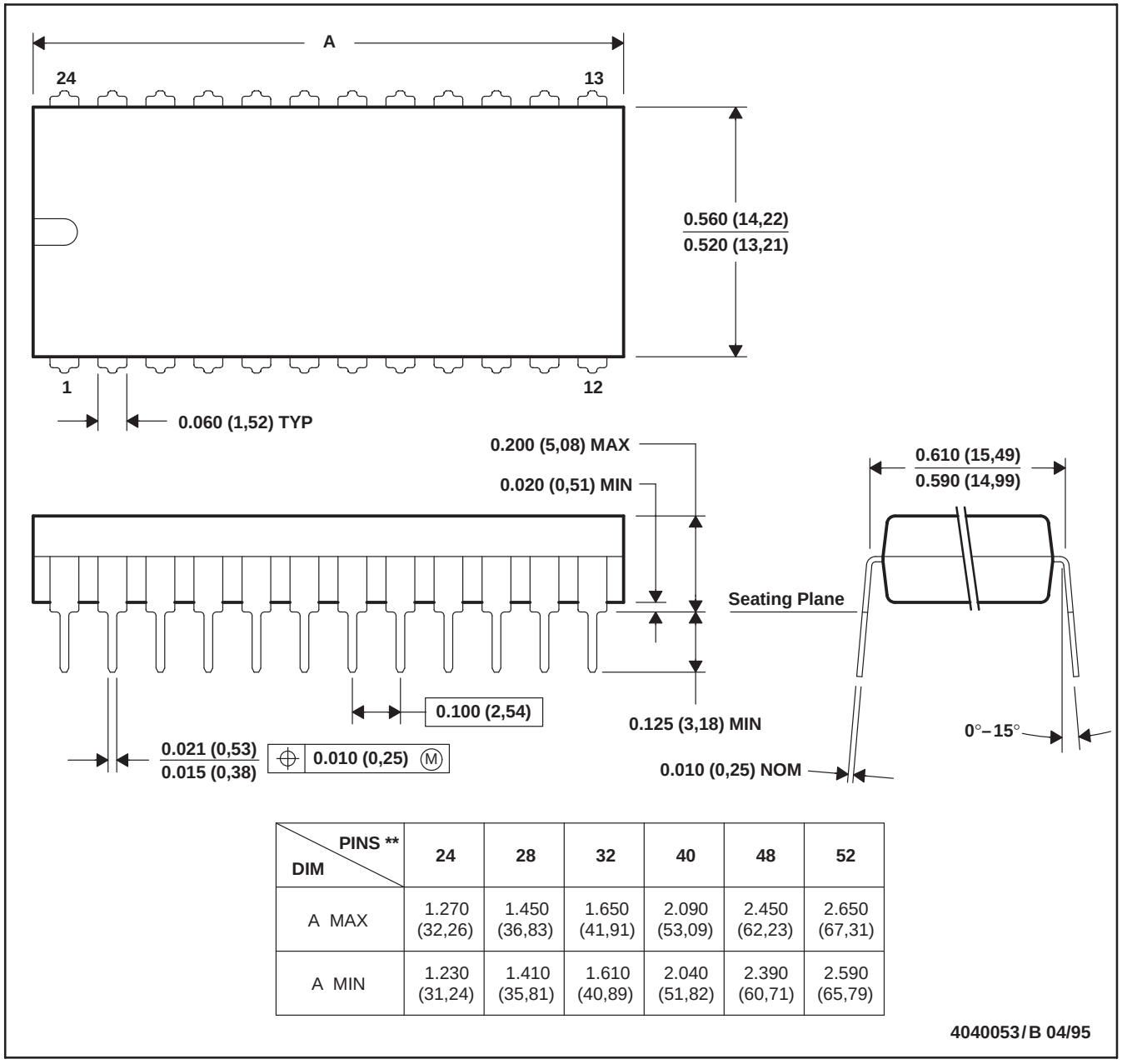
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

MPDI008 – OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

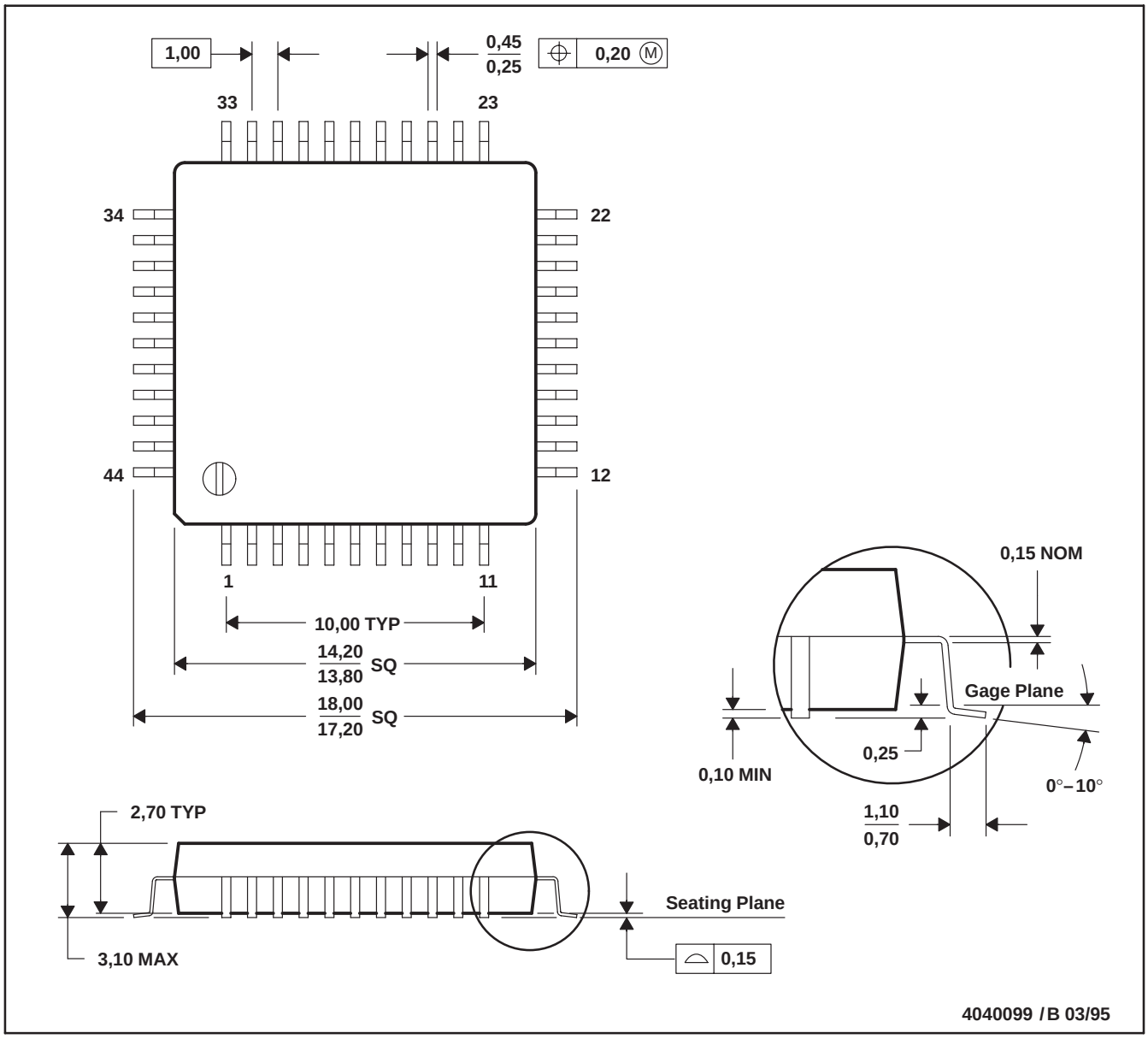


DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

PE (S-PQFP-G44) **PLASTIC QUAD FLATPACK**



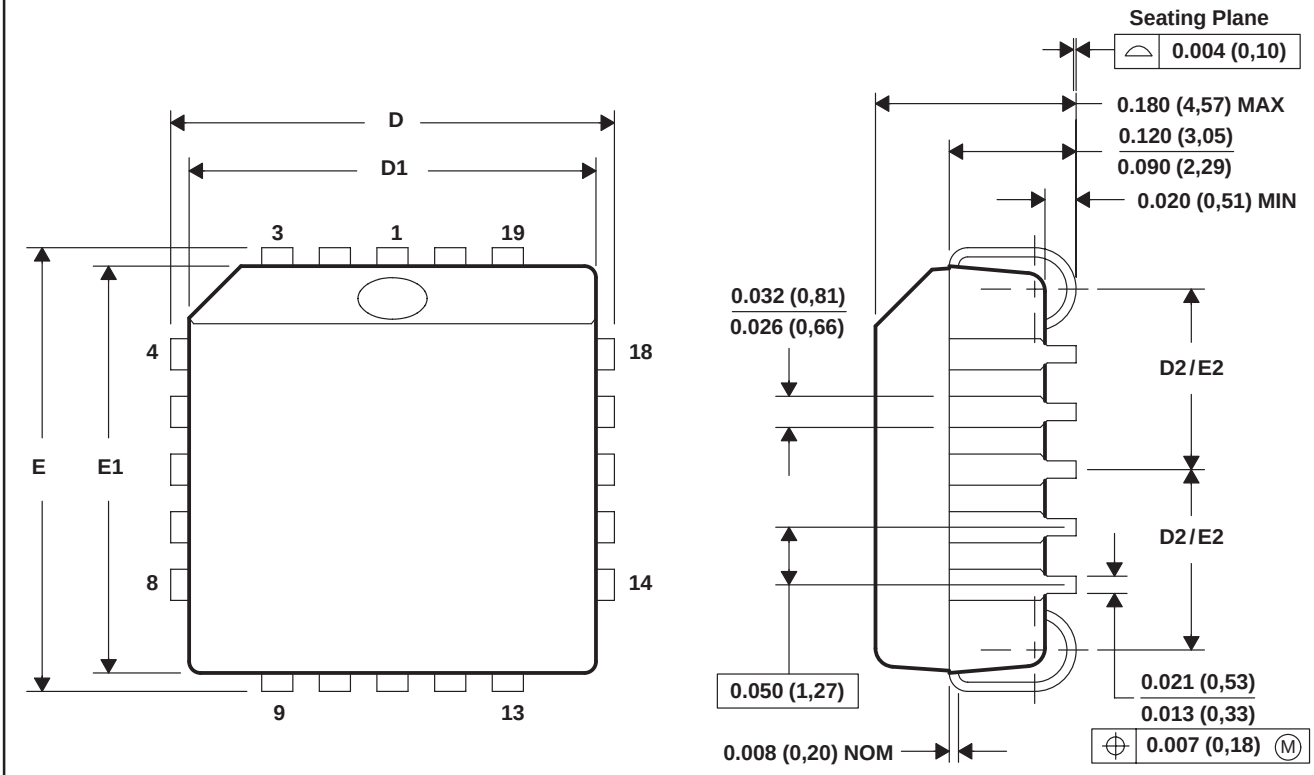
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



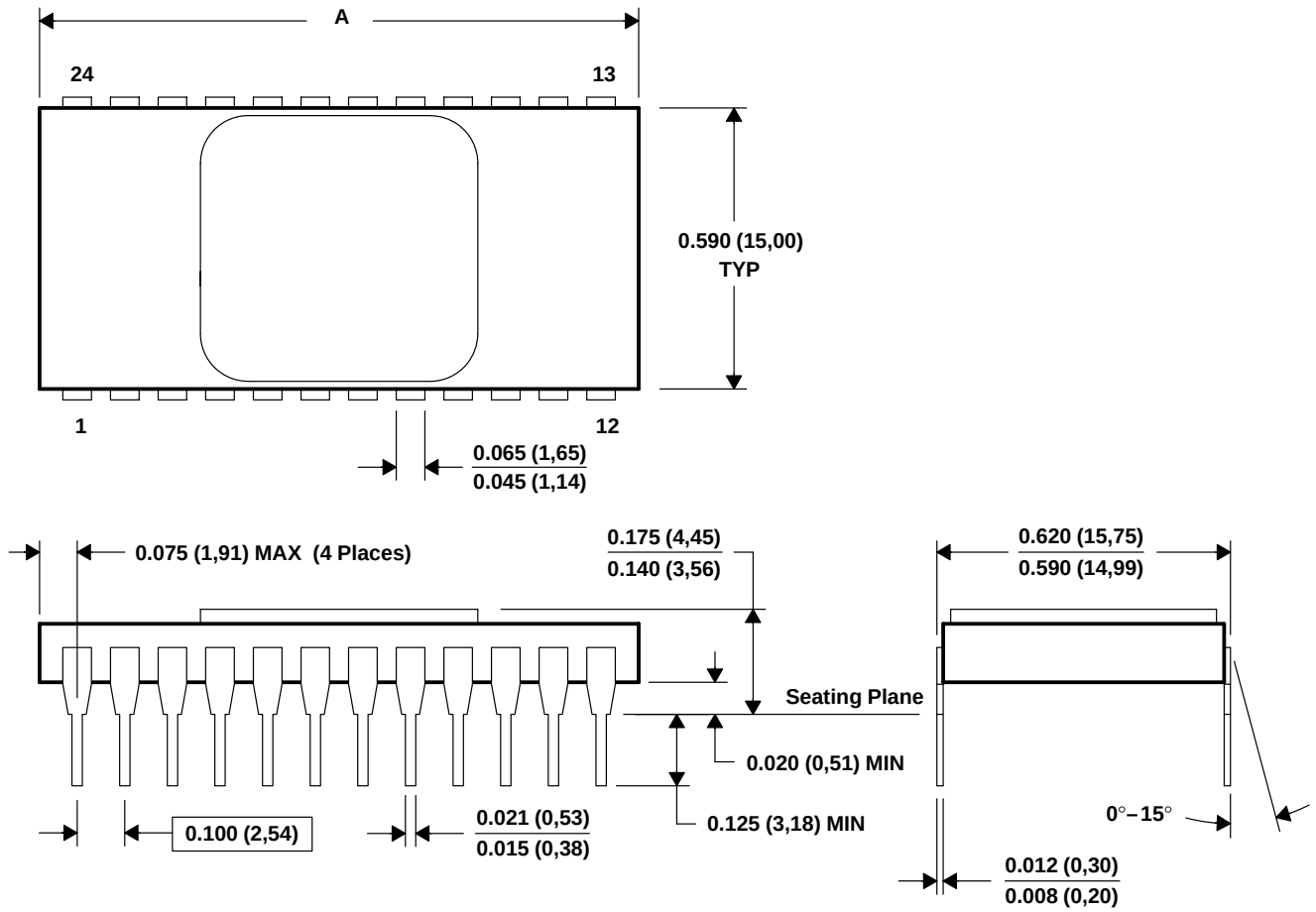
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

JD (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**

24 PINS SHOWN



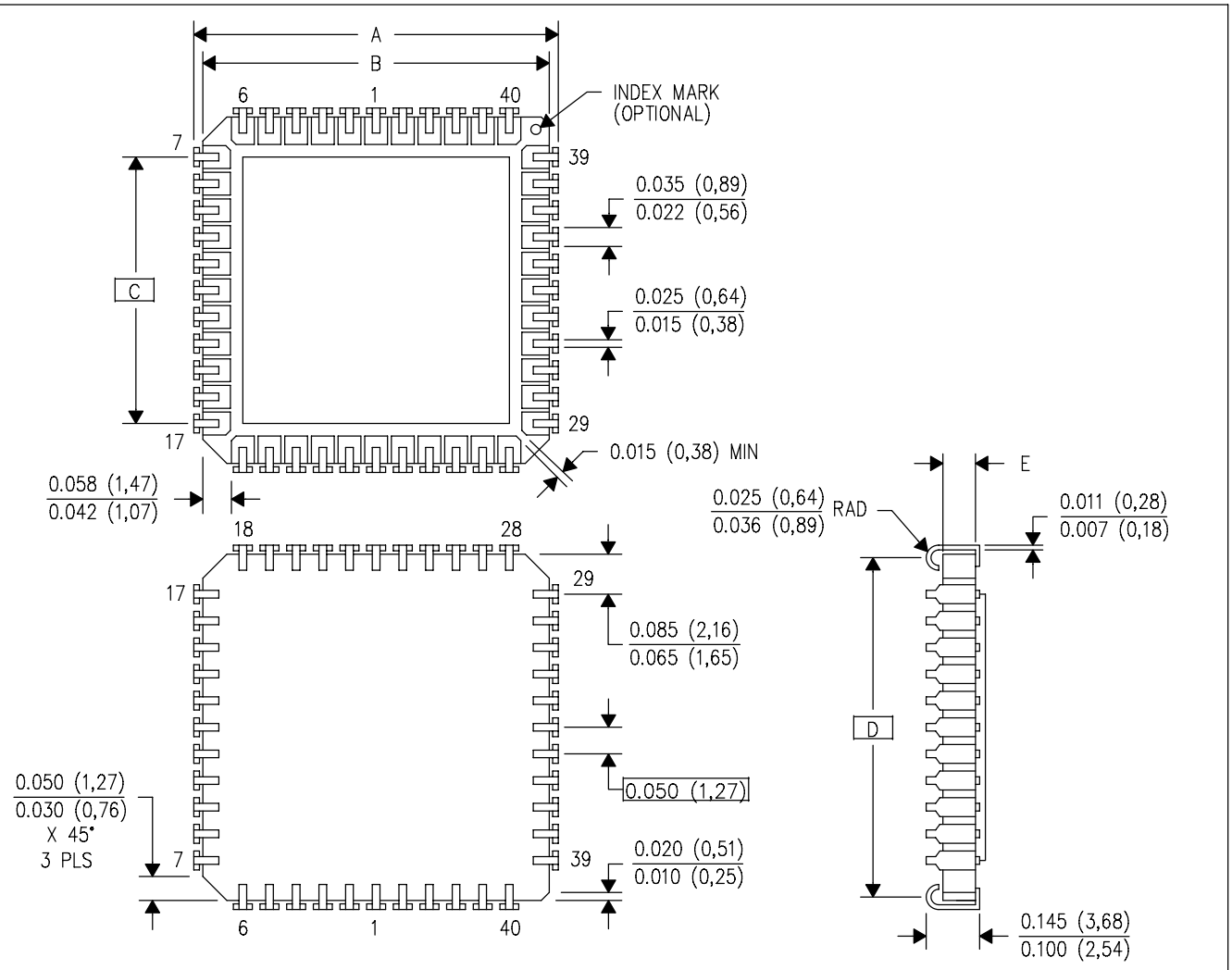
DIM \ PINS **	24	28	40	48	52
A MAX	1.250 (31,75)	1.450 (36,83)	2.050 (52,07)	2.435 (61,85)	2.650 (67,31)

4040087/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold-plated.

FJ (S–CQCC–J**) J–LEADED CERAMIC CHIP CARRIER

44 PINS SHOWN

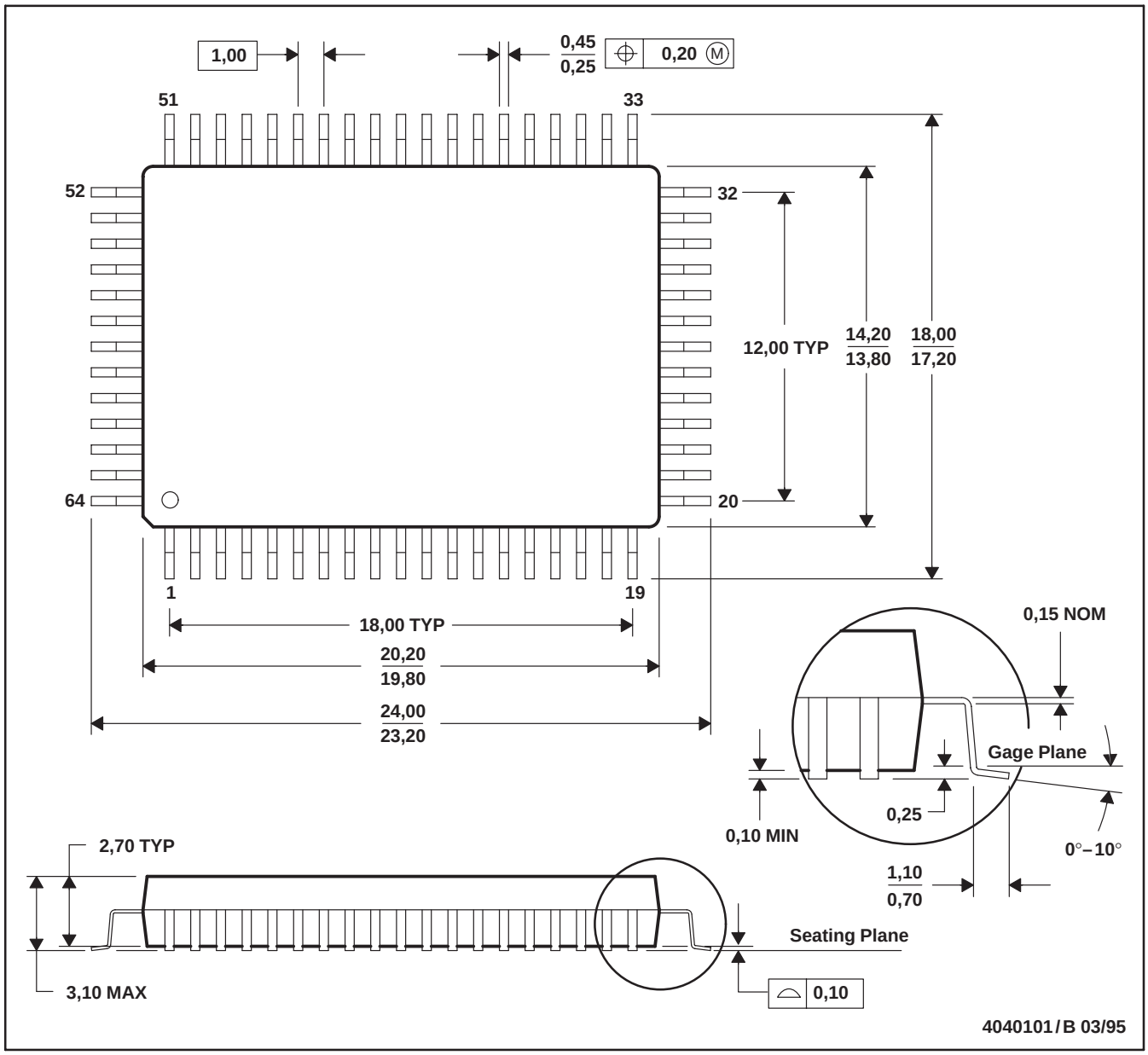


DIM / PINS **	A MAX	A MIN	B MAX	B MIN	C BSC	D BSC	E MAX	E MIN
44	0.700 (17,78)	0.680 (17,27)	0.659 (16,74)	0.641 (16,28)	0.500 (12,70)	0.630 (16,00)	0.080 (2,03)	0.058 (1,47)
68	1.000 (25,40)	0.980 (24,89)	0.960 (24,38)	0.940 (23,88)	0.800 (20,32)	0.930 (23,62)	0.095 (2,41)	0.072 (1,83)

4040139/D 04/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending on package vendor.
D. This package is hermetically sealed with a metal lid.

PG (R-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

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