

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

The SN54F299 is obsolete and no longer supplied.

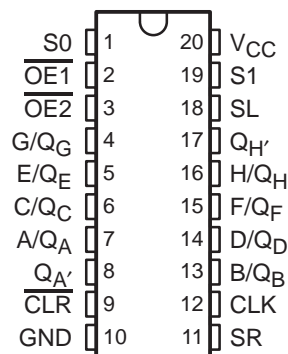
- **Four Modes of Operation:**
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- **Operates With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - Stacked or Pushdown Registers
  - Buffer Storage
  - Accumulator Registers

## description/ordering information

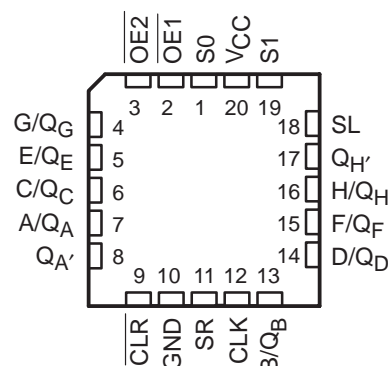
These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0, S_1$ ) inputs and two output-enable ( $\overline{OE1}, \overline{OE2}$ ) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE1}$  or  $\overline{OE2}$  high disables the outputs but has no effect on clearing, shifting, or storage of data.

SN54F299 . . . J PACKAGE  
SN74F299 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54F299 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN74F299N	SN74F299N
	SOIC – DW	Tube of 25	SN74F299DW	F299
		Reel of 2000	SN74F299DWR	
	SOP – NS	Reel of 2000	SN74F299NSR	74F299

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

# SN54F299, SN74F299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

The SN54F299 is obsolete and no longer supplied.

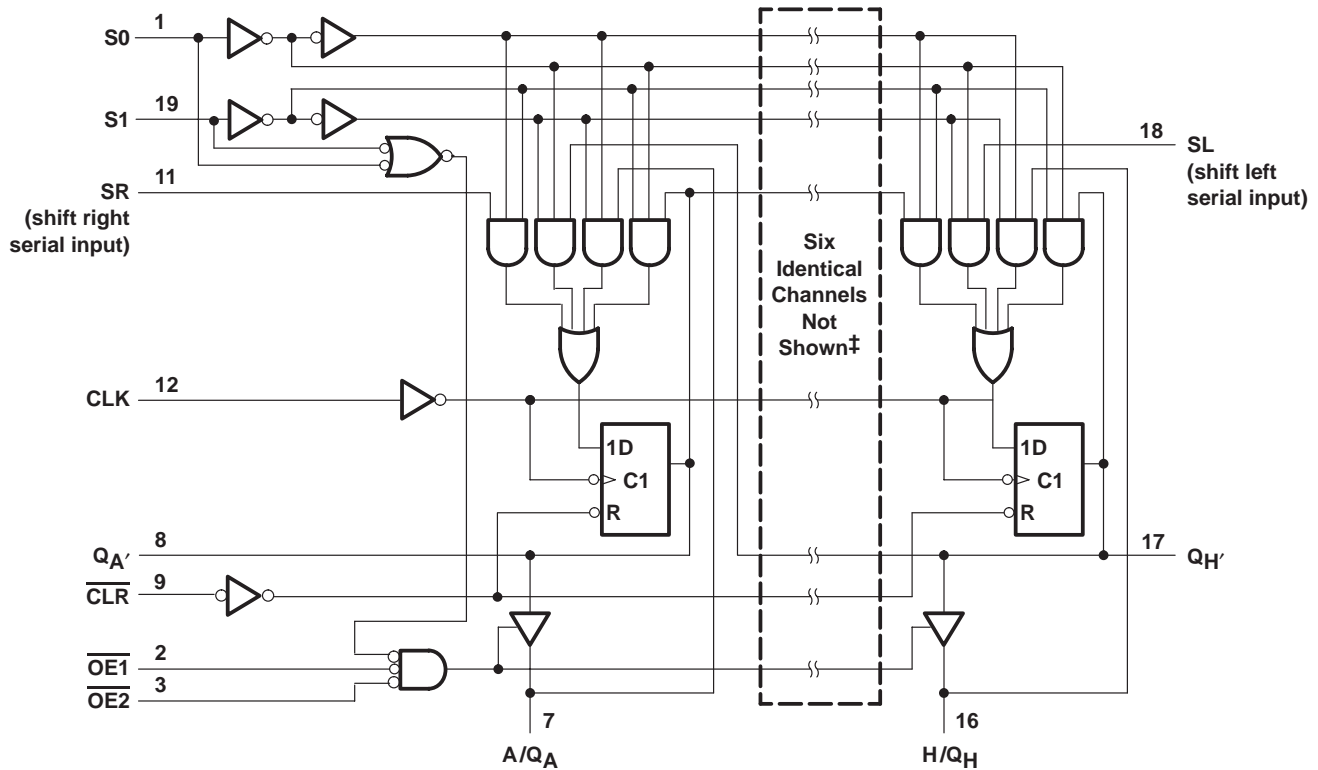
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	L	L	
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

### logic diagram (positive logic)



‡ I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

The SN54F299 is obsolete and no longer supplied.

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	–0.5 V to 5.5 V
Voltage range applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state: $Q_{A'}$ or $Q_{H'}$	40 mA
SN54F299 ( $Q_A$ thru $Q_H$ )	40 mA
SN74F299 ( $Q_A$ thru $Q_H$ )	48 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54F299			SN74F299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current	$Q_{A'}$ or $Q_{H'}$		–1	$Q_A$ thru $Q_H$		–1	mA
		$Q_A$ thru $Q_H$		–3	$Q_{A'}$ or $Q_{H'}$		–3	
$I_{OL}$	Low-level output current	$Q_{A'}$ or $Q_{H'}$		20	$Q_A$ thru $Q_H$		20	mA
		$Q_A$ thru $Q_H$		20	$Q_{A'}$ or $Q_{H'}$		24	
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54F299, SN74F299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

The SN54F299 is obsolete and no longer supplied.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F299			SN74F299			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V
$V_{OH}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$		2.5	3.4	2.5	3.4	V
	$Q_A$ thru $Q_H$		$I_{OH} = -1\text{ mA}$		2.5	3.4	2.5	3.4	
			$I_{OH} = -3\text{ mA}$		2.4	3.3	2.4	3.3	
Any output	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -1\text{ mA to } -3\text{ mA}$		2.7					
$V_{OL}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$		0.3	0.5	0.3	0.5	V
	$Q_A$ thru $Q_H$		$I_{OL} = 20\text{ mA}$		0.3	0.5			
			$I_{OL} = 24\text{ mA}$				0.35	0.5	
$I_I$	A thru H	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$		1			1	mA
	Any other		$V_I = 7\text{ V}$		0.1			0.1	
$I_{IH}^\ddagger$	A thru H	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		70			70	$\mu\text{A}$
	Any other				20			20	
$I_{IL}^\ddagger$	A thru H	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$		-0.65			-0.65	mA
	S0 or S1				-1.2			-1.2	
	Any other				-0.6			-0.6	
$I_{OS}^\S$	$V_{CC} = 5.5\text{ V}$ ,		$V_O = 0$		-60	-150	-60	-150	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ ,		See Note 4		68	95	68	95	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports ( $Q_A$  thru  $Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with  $\overline{OE1}$ ,  $\overline{OE2}$ , and CLK at 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54F299		SN74F299		UNIT	
			'F299		MIN	MAX	MIN	MAX		
			MIN	MAX						
$f_{\text{clock}}$	Clock frequency		70		65		70		MHz	
$t_w$	Pulse duration	CLK high or low		7		8		7		ns
		$\overline{\text{CLR}}$ low		7		8		7		
$t_{su}$	Setup time before CLK $\uparrow$	S0 or S1	High or low	8.5		9.5		8.5		ns
		A/ $Q_A$ thru H/ $Q_H$ , SR, or SL		High or low		5.5		6.5		
	Inactive-state setup time before CLK $\uparrow$ $\uparrow$	$\overline{\text{CLR}}$	High	7		13		7		
$t_h$	Hold time after CLK $\uparrow$	S0 or S1		High or low		0		0		ns
		A/ $Q_A$ thru H/ $Q_H$ , SR, or SL		High or low		2		2		

$\uparrow$  Inactive-state setup time also is referred to as recovery time.



The SN54F299 is obsolete and no longer supplied.

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			70	100		65		70	MHz	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.2	6.6	9	2.7	10.5	3.2	10	ns
t <sub>PHL</sub>			2.7	6.1	8.5	2.2	10	2.7	9.5	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	3.2	6.6	9	2.7	11	3.2	10	ns
t <sub>PHL</sub>			4.2	8.1	11	3.7	12.5	4.2	12	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q <sub>A</sub> thru Q <sub>H</sub>	5.7	10.6	14	5	15.5	5.7	15	
t <sub>PZH</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	2.7	5.6	8	2.2	10.5	2.7	9	ns
t <sub>PZL</sub>			3.2	6.6	10	2.7	12	3.2	11	
t <sub>PHZ</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	1.7	4.1	6	1.7	9	1.7	7	ns
t <sub>PLZ</sub>			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

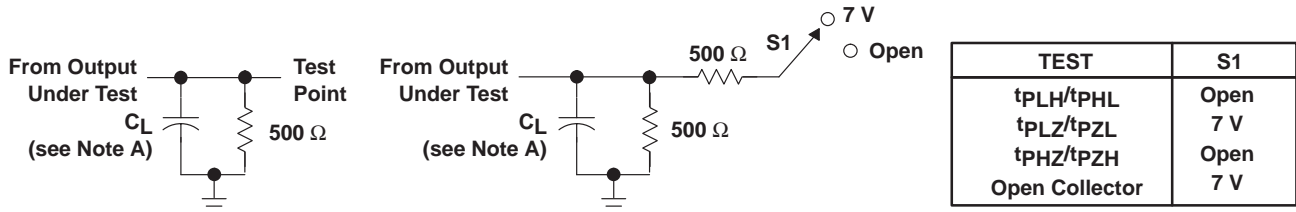
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

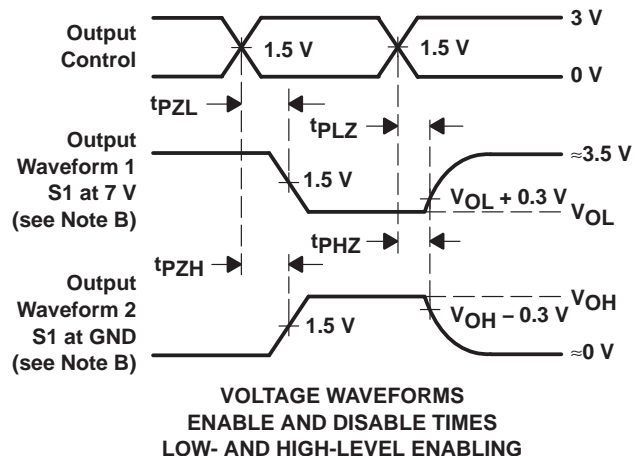
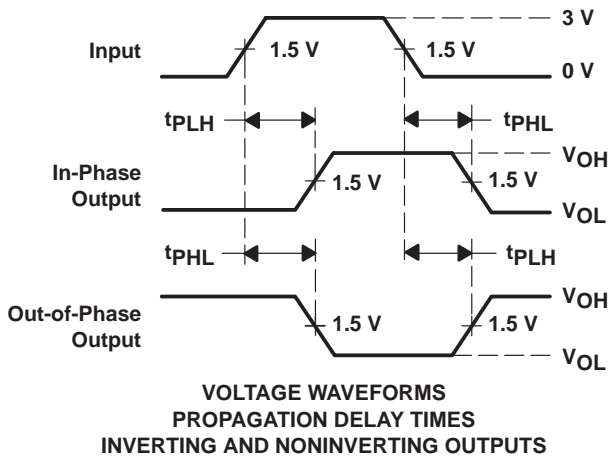
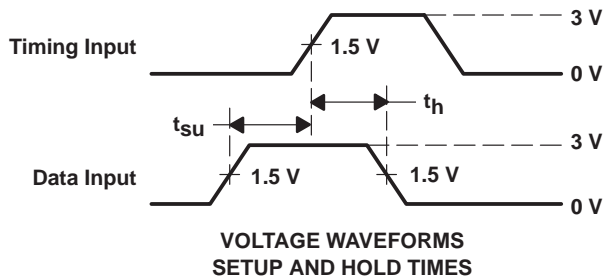
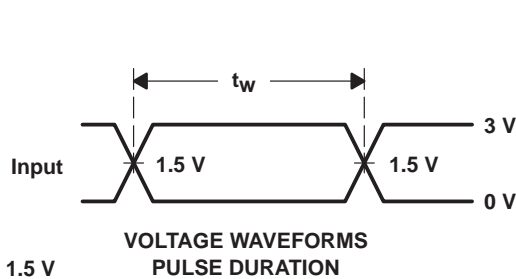
The SN54F299 is obsolete and no longer supplied.

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.  
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F299DW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	
SN74F299DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	Samples
SN74F299N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F299N	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F299DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F299DWR	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74F299N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated