- Very Low-Dropout Voltage . . . Less Than 400 mV at 300 mA
- Standby Mode Reduces Current to a Maximum of 150 μA
- Output Regulated to Within ±2% Over Full Temperature Range
- Packaged in Thin Shrink Small-Outline Package
- Only 10-µF Load Capacitor Required to Maintain Regulation at I<sub>O</sub> = 300 mA

## description

The TL75LPxxQ devices are low-dropout voltage regulators specifically targeted for use in portable applications. These devices generate fixed output voltages at loads of up to 300 mA with only 400-mV dropout over the full temperature range.

Low-dropout voltage regulators are commonly used in battery-powered systems such as analog and digital cellular phones. The TL75LPxx family of regulators feature a TTL/CMOS-compatible enable terminal, which can be used to switch the device into standby mode. This feature reduces power consumption when the instrument is not active. Less that 150  $\mu$ A is required when the unit is disabled.

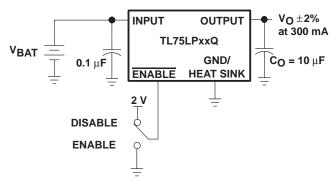
A concern in many new designs is conservation of board space and overall reduction in equipment size. The thin shrink small-outline package (TSSOP) minimizes board area and reduces

PW PACKAGE (TOP VIEW)					
GND/HEAT SINK	1	E	NC NC		
GND/HEAT SINK	2	18	NC		
NC [ NC [	4 5		NC NC		
ENABLE	6	Γ E	OUTPUT		
	7	<b>6</b>	OUTPUT		
	8 9	6	NC NC		
	9 10	6			

GND/HEAT SINK – These terminals have an internal connection to ground and must be grounded. NC – No internal connection

<sup>†</sup> The PW package is only available in left-end taped and reeled (order device TL75LPxxQPWLE).

# typical application schematic



component height. This package has a maximum height of less than 1.1 mm (compared to the 1.75 mm of a standard 8-pin SO package) and dimensions of only 6.5 mm by 4.4 mm.

All low-dropout regulators require an external capacitor at the output to maintain regulation and stability. To further reduce board area and cost, the TL75LPxx devices are designed to require a minimum capacitor of only 10  $\mu$ F. This is 1/10 the typical value used by many other low-dropout regulators. To simplify the task of choosing a suitable capacitor, TI has included in this datasheet a list of recommended capacitors for use with these devices.

The TL75LPxxQ devices are characterized for operation over  $T_J = -40^{\circ}C$  to  $125^{\circ}C$ .

AVAILABLE OPTIONS										
	Vo		PACKAGED DEVICES							
+0			TSSOP	CHIP FORM						
MIN			(Y)							
4.75	4.85	4.95	TL75LP48QPWLE	TL75LP48Y						
4.9	5	5.1	TL75LP05QPWLE	TL75LP05Y						
7.84	8	8.16	TL75LP08QPWLE	TL75LP08Y						
9.8	10	10.2	TL75LP10QPWLE	TL75LP10Y						
11.76	12	12.24	TL75LP12QPWLE	TL75LP12Y						
	4.75 4.9 7.84 9.8	Vo           MIN         TYP           4.75         4.85           4.9         5           7.84         8           9.8         10	Vo           MIN         TYP         MAX           4.75         4.85         4.95           4.9         5         5.1           7.84         8         8.16           9.8         10         10.2	VO         PACKAGED DEVICES           MIN         TYP         MAX         TSSOP (PW)           4.75         4.85         4.95         TL75LP48QPWLE           4.9         5         5.1         TL75LP05QPWLE           7.84         8         8.16         TL75LP08QPWLE           9.8         10         10.2         TL75LP10QPWLE						

**AVAILABLE OPTIONS** 

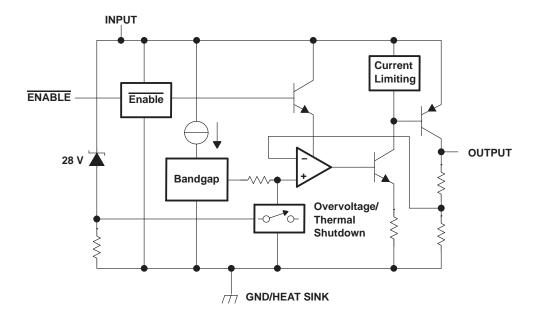
The PW package is available only in tape and reel. Chip forms are tested at 25°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



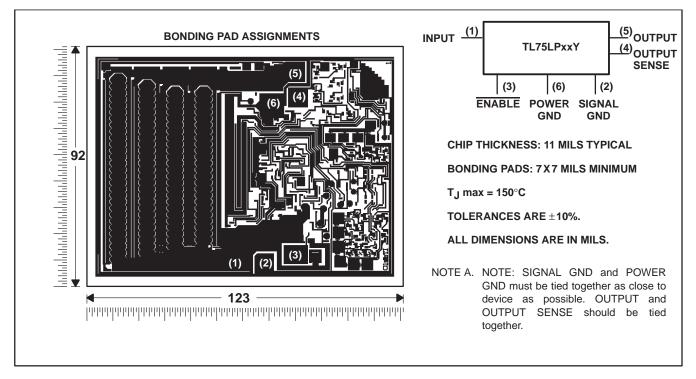
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#### functional block diagram



## TL75LPxxY chip information

This chip, when properly assembled, displays characteristics similar to the TL75LPxx. Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.





#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub> , (See Note 1)	25 V
Output current, I <sub>O</sub>	את כ
Operating virtual junction temperature range, T <sub>J</sub>	50°C
Continuous total power dissipation (see Note 2) See Dissipation Rating	Fable
Storage temperature range, T <sub>stg</sub> –65°C to 1	50°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	60°C

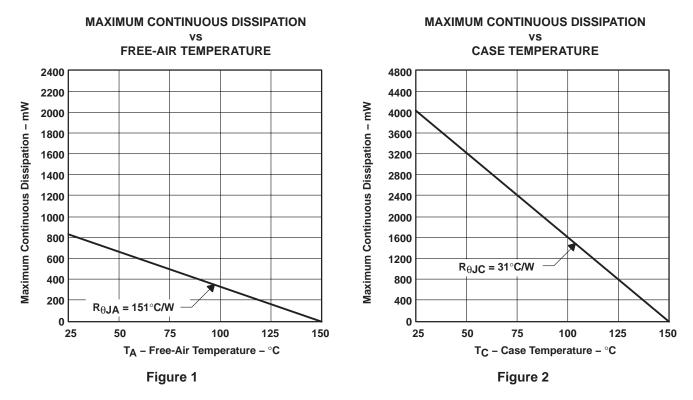
<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network terminal ground.

2. Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

		I	DISSIPATION RATING T	ABLE		
PACKAGE	POWER RATING	$T \le 25^{\circ}C$	DERATING FACTOR	T = 70°C	T = 85°C	T = 125°C
	AT	POWER RATING	ABOVE T = 25°C	POWER RATING	POWER RATING	POWER RATING
PW	T <sub>A</sub>	828 mW	6.62 mW/°C	530 mW	431 mW	166 mW
	T <sub>C</sub>	4032 mW	32.2 mW/°C	2583 mW	2100 mW	812 mW
	TP <sup>‡</sup>	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

 $R_{A,IP}$  is the thermal resistance between the junction and the device pin. To determine the virtual junction temperature (T, ) relative to the device pin temperature, the following calculations should be used:  $T_J = P_D x R_{\theta,JP} + T_P$ , where  $P_D$  is the internal power dissipation of the device and  $T_P$ is the device pin temperature at the point of contact to the printed wiring board. The R<sub>0.JP</sub> for the TL75LPxx series is 50.5°C/W.





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#### recommended operating conditions

		MIN	MAX	UNIT
	TL75LP48	5.15	23.0	
Input voltage, Vi	TL75LP05	5.3	23.0	
	TL75LP08	8.4	23.0	V
	TL75LP10	10.4	23.0	
	TL75LP12	12.5	23.0	
High-level input voltage, ENABLE, VIH		2.0	15.0	V
Low-level input voltage, ENABLE, VIL		0	0.8	V
Output current range, IO		5	300	mA
Operating virtual junction temperature range, TJ		-40	125	°C

### electrical characteristics over operating virtual junction temperature range, V<sub>I</sub> = 10 V, I<sub>O</sub> = 300 mA, ENABLE = 0 V (unless otherwise noted)

		TL	75LP48	Q	
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT
Output voltage	V <sub>I</sub> = 5.35 V to 10 V	4.75	4.85	4.95	V
Input voltage regulation	$V_{I} = 5.35 V$ to 10 V, $T_{J} = 25^{\circ}C$		10	25	mV
Ripple rejection	$V_{I} = 5.6 V$ to 15.6 V, f = 120 Hz, $T_{J} = 25^{\circ}C$	50	55		dB
Output voltage regulation	$I_O = 5 \text{ mA to } 300 \text{ mA}, T_J = 25^{\circ}C$		12	30	mV
	I <sub>O</sub> = 100 mA		0.12	0.2	
Dropout voltage	I <sub>O</sub> = 200 mA		0.17	0.3	V
	I <sub>O</sub> = 300 mA		0.22	5       4.95         5       25         5       2         2       0.2         7       0.3         2       0.4         0	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}, \text{ T}_{J} = 25^{\circ}\text{C}$		500		μV
	I <sub>O</sub> = 10 mA		2.5	4	
	I <sub>O</sub> = 100 mA		4	10	
Bias current	I <sub>O</sub> = 200 mA		6	20	mA
	I <sub>O</sub> = 300 mA		9	30	
High-level input current, ENABLE	ENABLE = 0.8 V		7	25	μΑ
Low-level input current, ENABLE	ENABLE = 2 V		0.05	6	μΑ
Standby current	ENABLE = 2 V		100	150	μΑ



# <u>electrical</u> characteristics over operating virtual junction temperature range, $V_I = 10 V$ , $I_O = 300 mA$ , ENABLE = 0 V (unless otherwise noted)

		TL	75LP05	Q	
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT
Output voltage	V <sub>I</sub> = 5.5 V to 10 V	4.9	5	5.1	V
Input voltage regulation	$V_{I} = 5.5 V$ to 10 V, $T_{J} = 25^{\circ}C$		10	25	mV
Ripple rejection	$V_{I} = 6 V$ to 16 V, $f = 120 Hz$ , $T_{J} = 25^{\circ}C$	50	55		dB
Output voltage regulation	$I_{O} = 5 \text{ mA to } 300 \text{ mA}, T_{J} = 25^{\circ}C$		12	30	mV
	I <sub>O</sub> = 100 mA		0.12	0.2	
Dropout voltage	I <sub>O</sub> = 200 mA		0.17	0.3	V
	I <sub>O</sub> = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T <sub>J</sub> = 25°C		500		μV
	I <sub>O</sub> = 10 mA				
	I <sub>O</sub> = 100 mA		4	10	
Bias current	I <sub>O</sub> = 200 mA		6	20	mA
	I <sub>O</sub> = 300 mA		9	30	
High-level input current, ENABLE	ENABLE = 0.8 V		7	25	μΑ
Low-level input current, ENABLE	ENABLE = 2 V		0.05	6	μΑ
Standby current	ENABLE = 2 V		100	150	μΑ

<sup>†</sup> Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

# <u>electrical</u> characteristics over operating virtual junction temperature range, $V_I = 10 V$ , $I_O = 300 mA$ , ENABLE = 0 V (unless otherwise noted)

	+	TL	75LP08	Q	
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT
Output voltage	V <sub>I</sub> = 8.6 V to 15 V	7.84	8	8.16	V
Input voltage regulation	$V_{I} = 8.6 V$ to 15 V, $T_{J} = 25^{\circ}C$		12	40	mV
Ripple rejection	$V_{I} = 9 V$ to 19 V, $f = 120 Hz$ , $T_{J} = 25^{\circ}C$	50	55		dB
Output voltage regulation	$I_{O} = 5 \text{ mA to } 300 \text{ mA}, T_{J} = 25^{\circ}\text{C}$		12	40	mV
	I <sub>O</sub> = 100 mA		0.12	0.2	
Dropout voltage	I <sub>O</sub> = 200 mA		0.17	0.3	V
utput voltage put voltage regulation pple rejection utput voltage regulation ropout voltage utput noise voltage as current gh-level input current, ENABLE pw-level input current, ENABLE	I <sub>O</sub> = 300 mA		0.22	0.4	
Output noise voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}, \text{ T}_{J} = 25^{\circ}\text{C}$		500		μV
	I <sub>O</sub> = 10 mA		2.5	4	
	I <sub>O</sub> = 100 mA		4	10	
Blas current	I <sub>O</sub> = 200 mA		6	20	mA
	I <sub>O</sub> = 300 mA		9	30	
High-level input current, ENABLE	ENABLE = 0.8 V		7	25	μΑ
Low-level input current, ENABLE	ENABLE = 2 V		0.05	6	μΑ
Standby current	ENABLE = 2 V		100	150	μΑ



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#### electrical characteristics over operating virtual junction temperature range, VI = 14 V, IO = 300 mA, ENABLE = 0 V (unless otherwise noted)

PARAMETER		TL			
	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	V <sub>I</sub> = 10.6 V to 17 V	9.8	10	10.2	V
Input voltage regulation	$V_{I} = 10.6 V$ to 17 V, $T_{J} = 25^{\circ}C$		15	43	mV
Ripple rejection	$V_{I} = 11 V \text{ to } 21 V$ , $f = 120 \text{ Hz}$ , $T_{J} = 25^{\circ}\text{C}$	50	55		dB
Output voltage regulation	$I_{O} = 5 \text{ mA to } 300 \text{ mA}, T_{J} = 25^{\circ}C$		15	50	mV
opout voltage	I <sub>O</sub> = 100 mA		0.12	0.2	
Dropout voltage	I <sub>O</sub> = 200 mA		0.17	$\begin{array}{c cccc}  & 10.2 \\  & 5 & 43 \\  & 5 & 50 \\  & 2 & 0.2 \\  & 7 & 0.3 \\  & 2 & 0.4 \\  & 0 & & \\  & 5 & 4 \\  & 4 & 10 \\  & 6 & 20 \\  & 9 & 30 \\  & 7 & 25 \\  & 5 & 6 \\  \end{array}$	V
	I <sub>O</sub> = 300 mA	MIN         TYP         M. $17 \vee$ 9.8         10         1 $17 \vee$ $12 = 25^{\circ}$ C         15         15 $1 \vee$ $1 = 25^{\circ}$ C         15         15 $0.0 \text{ mA}$ , $T_J = 25^{\circ}$ C         15         0.12         10 $0.12$ 0.17         0.22         10 $00 \text{ kHz}$ , $T_J = 25^{\circ}$ C         1000         2.5         1000 $0.225$ 4         6         9 $3 \vee$ 7         7         7 $7 \vee$ 0.05         1005         1000	0.4		
Output noise voltage	f = 10 Hz to 100 kHz, T <sub>J</sub> = 25°C		1000		μV
	I <sub>O</sub> = 10 mA		2.5	4	
	I <sub>O</sub> = 100 mA		4	10	
Bias current	I <sub>O</sub> = 200 mA		6	20	mA
	I <sub>O</sub> = 300 mA		9	30	
High-level input current, ENABLE	ENABLE = 0.8 V		7	25	μΑ
Low-level input current, ENABLE	ENABLE = 2 V		0.05	6	μΑ
Standby current	ENABLE = 2 V		100	150	μΑ

<sup>†</sup> Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

#### electrical characteristics over operating virtual junction temperature range, VI = 14 V, IO = 300 mA, ENABLE = 0 V (unless otherwise noted)

	t	TL75LP12Q		Q	
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT
Output voltage	V <sub>I</sub> = 12.7 V to 18 V	11.76	12	12.24	V
Input voltage regulation	$V_{I} = 12.7 V \text{ to } 18 V$ , $T_{J} = 25^{\circ}C$		15	43	mV
Ripple rejection	$V_{I} = 13 V \text{ to } 23 V$ , $f = 120 \text{ Hz}$ , $T_{J} = 25^{\circ}\text{C}$	50	55		dB
Output voltage regulation	$I_{O} = 5 \text{ mA to } 300 \text{ mA}, T_{J} = 25^{\circ}\text{C}$		15	60	mV
	I <sub>O</sub> = 100 mA		0.12	0.2	
Dropout voltage	I <sub>O</sub> = 200 mA		0.17	0.3	V
	I <sub>O</sub> = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T <sub>J</sub> = 25°C		1000		μV
	I <sub>O</sub> = 10 mA		2.5	4	
	I <sub>O</sub> = 100 mA		4	10	
Bias current	I <sub>O</sub> = 200 mA		6	20	mA
	I <sub>O</sub> = 300 mA		9	30	
High-level input current, ENABLE	ENABLE = 0.8 V		7	25	μA
Low-level input current, ENABLE	ENABLE = 2 V		0.05	6	μA
Standby current	ENABLE = 2 V		100	150	μA



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## electrical characteristics at V<sub>I</sub> = 10 V, I<sub>O</sub> = 300 mA, ENABLE = 0 V, T<sub>J</sub> = 25°C (unless otherwise noted)

DADAMETED		TL7	TL75LP48Y			
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT	
Output voltage			4.85		V	
Input voltage regulation			10		mV	
Ripple rejection	f = 120 Hz		55		dB	
Output voltage regulation			12		mV	
Dropout voltage			0.22		V	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV	
Bias current			9		mA	
High-level input current, ENABLE	ENABLE = 0.8 V		7		μA	
Low-level input current, ENABLE	ENABLE = 2 V		0.05		μA	
Standby current	ENABLE = 2 V		100		μA	

<sup>†</sup> Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

### electrical characteristics at V<sub>I</sub> = 10 V, I<sub>O</sub> = 300 mA, ENABLE = 0 V, T<sub>J</sub> = 25°C (unless otherwise noted)

		TL			
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN         TYP           5         10           55         12           0.22         0.22	MAX	UNIT	
Output voltage			5		V
Input voltage regulation			10		mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12		mV
Dropout voltage			0.22		V
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current			9		mA
High-level input current, ENABLE	ENABLE = 0.8 V		7		μΑ
Low-level input current, ENABLE	ENABLE = 2 V		0.05		μA
Standby current	ENABLE = 2 V		100		μA



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# electrical characteristics at V<sub>I</sub> = 10 V, I<sub>O</sub> = 300 mA, ENABLE = 0 V, T<sub>J</sub> = 25°C (unless otherwise noted)

		TL	TL75LP08Y		
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT
Output voltage			8		V
Input voltage regulation			12		mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12		mV
Dropout voltage			0.22		V
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current			9		mA
High-level input current, ENABLE	ENABLE = 0.8 V		7		μA
Low-level input current, ENABLE	ENABLE = 2 V		0.05		μA
Standby current	ENABLE = 2 V		100		μA

<sup>†</sup> Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

### electrical characteristics at V<sub>I</sub> = 14 V, I<sub>O</sub> = 300 mA, ENABLE = 0 V, T<sub>J</sub> = 25°C (unless otherwise noted)

		TL75LP10Y				
PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT	
Output voltage			10		V	
Input voltage regulation			15		mV	
Ripple rejection	f = 120 Hz		55		dB	
Output voltage regulation			15		mV	
Dropout voltage			0.22		V	
Output noise voltage	f = 10 Hz to 100 kHz		1000		μV	
Bias current			9		mA	
High-level input current, ENABLE	ENABLE = 0.8 V		7		μA	
Low-level input current, ENABLE	ENABLE = 2 V		0.05		μA	
Standby current	ENABLE = 2 V		100		μΑ	



## electrical characteristics at V<sub>I</sub> = 14 V, I<sub>O</sub> = 300 mA, ENABLE = 0 V, T<sub>J</sub> = 25°C (unless otherwise noted)

PARAMETER	+	TL	TL75LP12Y		
	TEST CONDITIONS <sup>†</sup>	MIN	TYP	MAX	UNIT
Output voltage		11.76	12	12.24	V
Input voltage regulation			15	43	mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12	60	mV
Dropout voltage			0.22	0.4	V
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current			9	30	mA
High-level input current, ENABLE	ENABLE = 0.8 V		7	25	μA
Low-level input current, ENABLE	ENABLE = 2 V		0.05	6	μA
Standby current	ENABLE = 2 V		100	150	μA



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## PARAMETER MEASUREMENT INFORMATION

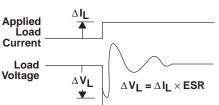
The TL75LPxx series are low-dropout voltage regulators. This means that the capacitance is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can establish the capacitance value and ESR range for optimum regulator performance.

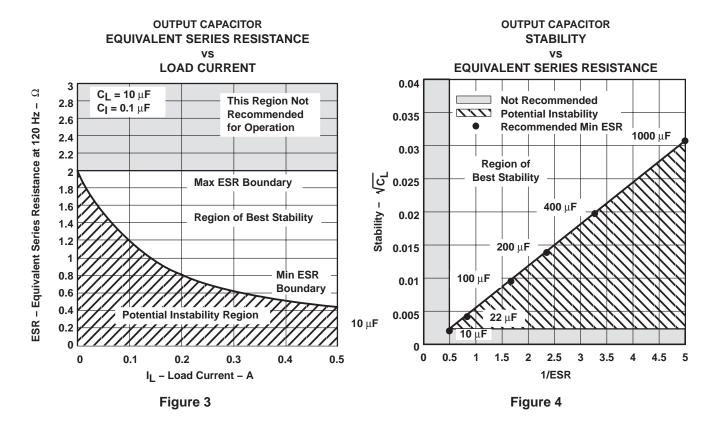
Figure 3 shows the recommended range of ESR, measured at 120 Hz, for a given load with a 10-µF capacitor on the output. In addition, it shows a maximum ESR limit of 2  $\Omega$  and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 4 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 μF and a maximum ESR limit of 2 Ω. Figure 4 establishes the amount that the minimum ESR limit of Figure 3 can be adjusted for different capacitor values. For example, when the minimum load needed is 200 mA, Figure 3 suggests an ESR range of 0.8  $\Omega$  to 2  $\Omega$  for 10  $\mu$ F. Figure 4 shows that changing the capacitor from 10 µF to 400 µF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13  $\Omega$ ). This now allows an ESR range of 0.13  $\Omega$  to 2  $\Omega$ . This expanded ESR range is achieved by using a larger capacitor at the output. For better stability in low-current applications, it is recommended that a small resistance be placed in series with the capacitor (see Table 1) so that the ESR better approximates those in Figures 3 and 4.



MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 μF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 μF	0.6 Ω	T491D336M010AS	0.5 Ω







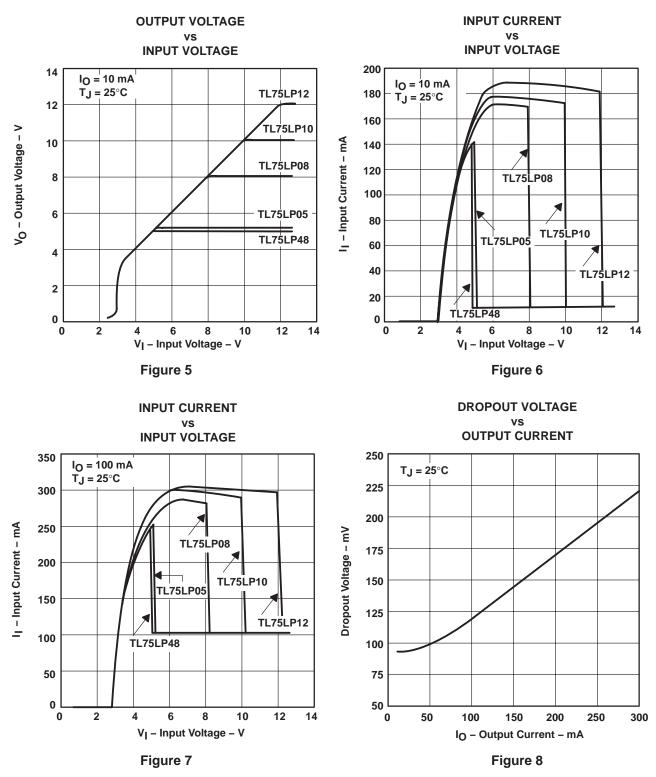
## **TYPICAL CHARACTERISTICS**

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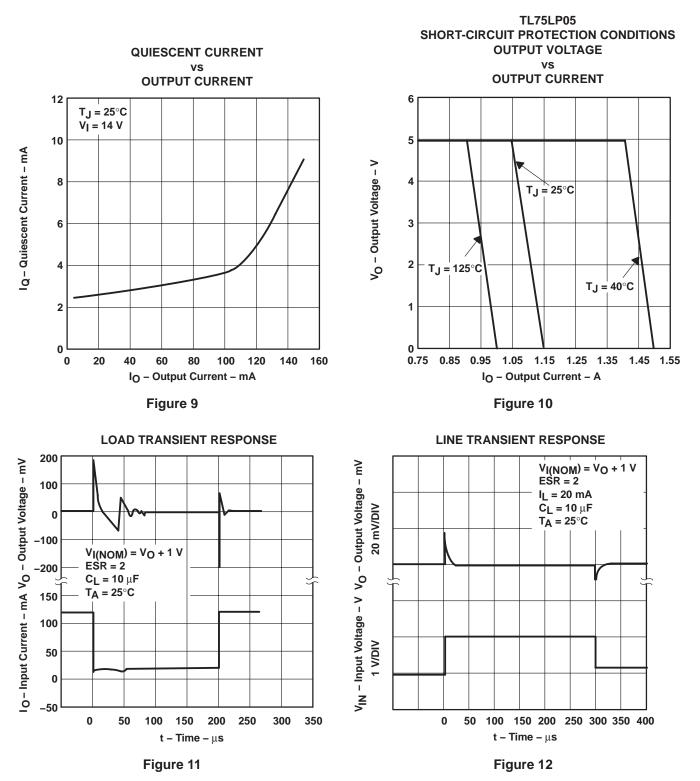








#### **TYPICAL CHARACTERISTICS**





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