100 mV from rail

# LMV921/LMV922/LMV924

# Single, Dual and Quad 1.8V, 1MHz, Low Power Operational Amplifiers with Rail-To-Rail Input and Output

# **General Description**

The LMV921 Single/LMV922 Dual/LMV924 Quad are guaranteed to operate from +1.8V to +5.0V supply voltages and have rail-to-rail input and output. This rail-to-rail operation enables the user to make full use of the entire supply voltage range. The input common mode voltage range extends 300mV beyond the supplies and the output can swing rail-to-rail unloaded and within 100mV from the rail with 600 $\Omega$  load at 1.8V supply. The LMV921/LMV922/LMV924 are optimized to work at 1.8V which make them ideal for portable two-cell battery-powered systems and single cell Li-lon systems.

The LMV921/LMV922/LMV924 exhibit excellent speed-power ratio, achieving 1MHz gain bandwidth product at 1.8V supply voltage with very low supply current. The LMV921/LMV922/LMV924 are capable of driving  $600\Omega$  load and up to 1000pF capacitive load with minimal ringing. The LMV921/LMV922/LMV924's high DC gain of 100dB makes them suitable for low frequency applications.

The LMV921 (Single) is offered in a space saving SC70–5 and SOT23–5 packages. The SC70–5 package is only 2.0X2.1X1.0mm. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellphones and PDAs.

# **Features**

(Typical 1.8V Supply Values; Unless Otherwise Noted)

- Guaranteed 1.8V, 2.7V and 5V specifications
- Rail-to-Rail input & output swing
   w/600Ω load

- w/2kΩ load 30 mV from rail V<sub>CM</sub> 300mV beyond rails Supply current 145μA/amplifier

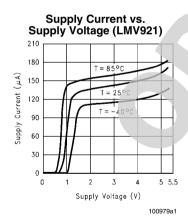
Supply current 145µA/amplifier
Gain bandwidth product 1MHz
LMV921 Maximum V<sub>OS</sub> 6mV

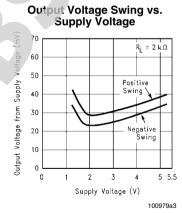
■ 90dB gain w/600Ω load

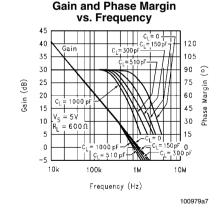
- LMV921 available in Ultra Tiny, SC70-5 package
- LMV922 available in MSOP-8 package
- LMV924 available in TSSOP-14 package

# **Applications**

- Cordless/cellular phones
- Laptops
- PDAs
- PCMCIA
- Portable/battery-powered electronic Equipment
- Supply current Monitoring
- Battery monitoring







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100979

# **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)

Machine Model 100V Human Body Model 2000V Differential Input Voltage  $\pm$  Supply Voltage Supply Voltage (V+-V-) 5.5V Output Short Circuit to V+ (*Note 3*)

Output Short Circuit to V- (*Note 3*)

Storage Temperature Range -65°C to 150°C Junction Temperature (*Note 4*) 150°C

Mounting Temp.

Infrared or Convection (20 sec) 235°C

# Operating Ratings (Note 1)

Supply Voltage 1.5V to 5.0V Temperature Range  $-40^{\circ}\text{C} \le T_{\text{J}} \le 85^{\circ}\text{C}$ 

Thermal Resistance ( $\theta_{JA}$ )

Ultra Tiny SC70-5 Package 5-Pin

Surface Mount 440 °C/W

Tiny SOT23-5 Package

5-Pin Surface Mount 265 °C/W

**MSOP** Package

8-Pin Surface Mount 235°C/W

TSSOP Package

14-Pin Surface Mount 155°C/W

SOIC Package

8-Pin Surface Mount 175°C/W 14-Pin Surface Mount 127°C/W

# 1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J$  = 25°C. V+ = 1.8V, V = 0V,  $V_{CM}$  = V+/2,  $V_O$  = V+/2 and  $R_I$  > 1 M $\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V <sub>OS</sub>	Input Offset Voltage	LMV921 (Single)	-1.8	6 <b>8</b>	mV max
		LMV922 (Dual) LMV924 (Quad)	-1.8	8 <b>9.5</b>	mV max
TCV <sub>OS</sub>	Input Offset Voltage Average Drift		1		μV/°C
I <sub>B</sub>	Input Bias Current		12	35 <b>50</b>	nA max
I <sub>os</sub>	Input Offset Current		2	25 <b>40</b>	nA max
I <sub>S</sub>	Supply Current	LMV921 (Single)	145	185 <b>205</b>	
		LMV922 (Dual)	330	400 <b>550</b>	μA max
		LMV924 (Quad)	560	700 <b>850</b>	
CMRR	Common Mode Rejection Ratio	0 ≤ V <sub>CM</sub> ≤ 0.6V	82	62 <b>60</b>	dB
		$-0.2V \le V_{CM} \le 0V$ $1.8V \le V_{CM} \le 2.0V$	74	50	min
PSRR	Power Supply Rejection Ratio	$1.8V \le V^{+} \le 5V,$ $V_{CM} = 0.5V$	78	67 <b>62</b>	dB min
V <sub>CM</sub>	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 <b>0</b>	V min
			2.15	2.0 <b>1.8</b>	V max

Symbol	Parameter	Condition	<b>Typ</b> ( <i>Note 5</i> )	Limits (Note 6)	Units
A <sub>V</sub>	Large Signal Voltage Gain	$R_{L} = 600\Omega$ to 0.9V,	91	77	
	LMV921 (Single)	$V_{O} = 0.2V$ to 1.6V, $V_{CM} = 0.5V$		73	dB
		$R_L = 2k\Omega$ to 0.9V,	95	80	min
		$V_{O} = 0.2V \text{ to } 1.6V, V_{CM} = 0.5V$		75	
	Large Signal Voltage Gain	$R_1 = 600\Omega$ to 0.9V,	79	65	
	LMV922 (Dual)	$V_0 = 0.2V \text{ to } 1.6V, V_{CM} = 0.5V$		61	dB
	LMV924 (Quad)	$R_1 = 2k\Omega$ to 0.9V,	83	68	min
		$V_0 = 0.2V \text{ to } 1.6V, V_{CM} = 0.5V$		63	
$\overline{V_0}$	Output Swing	$R_L = 600\Omega$ to 0.9V	1.7	1.65	V
		$V_{IN} = \pm 100 \text{mV}$		1.63	min
			0.075	0.090	V
				0.105	max
		$R_L = 2k\Omega$ to 0.9V	1.77	1.75	V
		$V_{IN} = \pm 100 \text{mV}$		1.74	min
			0.025	0.035	V
				0.040	max
Io	Output Short Circuit Current	Sourcing, V <sub>O</sub> = 0V	6	4	mA
		V <sub>IN</sub> = 100mV		3.3	min
		Sinking, V <sub>O</sub> = 1.8V	10	7	mA
		$V_{IN} = -100 \text{mV}$		5	min

# **1.8V AC Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for  $T_J$  = 25°C.  $V^+$  = 1.8V,  $V^-$  = 0V,  $V_{CM}$  = V+/2,  $V_O$  = V+/2 and  $R_L$  > 1 M $\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	<b>Typ</b> ( <i>Note 5</i> )	Units
SR	Slew Rate	(Note 7)	0.39	V/µs
GBW	Gain-Bandwidth Product		1	MHz
$\Phi_{m}$	Phase Margin		60	Deg
G <sub>m</sub>	Gain Margin		10	dB
e <sub>n</sub>	Input-Referred Voltage Noise	$f = 1 \text{ kHz}, V_{CM} = 0.5V$	45	nV √Hz
i <sub>n</sub>	Input-Referred Current Noise	f = 1 kHz	0.1	pA √Hz
THD	Total Harmonic Distortion	f = 1kHz, A <sub>V</sub> = +1		
		$R_L = 600k\Omega$ , $V_{IN} = 1 V_{PP}$	0.089	%
	Amp-to-Amp Isolation	(Note 8)	140	dB

# 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J$  = 25°C.  $V^+$  = 2.7V,  $V^-$  = 0V,  $V_{CM}$  = V+/2,  $V_O$  = V+/2 and  $R_L$  > 1 M $\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	<b>Typ</b> ( <i>Note 5</i> )	Limits (Note 6)	Units
V <sub>OS</sub>	Input Offset Voltage	LMV921 (Single)	-1.6	6 <b>8</b>	mV max
		LMV922 (Dual) LMV924 (Quad)	-1.6	8 <b>9.5</b>	mV max
TCV <sub>OS</sub>	Input Offset Voltage Average Drift		1		μV/°C
I <sub>B</sub>	Input Bias Current		12	35 <b>50</b>	nA max

Symbol	Parameter	Condition	<b>Typ</b> ( <i>Note 5</i> )	Limits (Note 6)	Units
I <sub>os</sub>	Input Offset Current		2	25 <b>40</b>	nA max
I <sub>S</sub>	Supply Current	LMV921 (Single)	147	190 <b>210</b>	
		LMV922 (Dual)	380	450 <b>600</b>	uA max
		LMV924 (Quad)	580	750 <b>900</b>	]
CMRR	Common Mode Rejection Ratio	0V ≤ V <sub>CM</sub> ≤ 1.5V	84	62 <b>60</b>	dB
		$-0.2V \le V_{CM} \le 0V$ 2.7V $\le V_{CM} < 2.9V$	73	50	min
PSRR	Power Supply Rejection Ratio	$1.8V \le V^{+} \le 5V$ , $V_{CM} = 0.5V$	78	67 <b>62</b>	dB min
V <sub>CM</sub>	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 <b>0</b>	V min
			3.050	2.9 <b>2.7</b>	V max
$A_V$	Large Signal Voltage Gain LMV921 (Single)	$R_L = 600\Omega$ to 1.35V, $V_O = 0.2V$ to 2.5V	98	80 <b>75</b>	dB
		$R_L = 2k\Omega \text{ to } 1.35V,$ $V_O = 0.2V \text{ to } 2.5V$	103	83 <b>77</b>	min
	Large Signal Voltage Gain LMV922 (Dual)	$R_L = 600\Omega$ to 1.35V, $V_O = 0.2V$ to 2.5V	86	68 <b>63</b>	dB
	LMV924 (Quad)	$R_L = 2k\Omega \text{ to } 1.35V,$ $V_O = 0.2V \text{ to } 2.5V$	91	71 <b>65</b>	min
V <sub>O</sub>	Output Swing	$R_L = 600\Omega \text{ to } 1.35V$ $V_{IN} = \pm 100 \text{mV}$	2.62	2.550 <b>2.530</b>	V min
			0.075	0.095 <b>0.115</b>	V max
		$R_L = 2k\Omega$ to 1.35V $V_{IN} = \pm 100$ mV	2.675	2.650 <b>2.640</b>	V min
			0.025	0.040 <b>0.045</b>	V max
lo	Output Short Circuit Current	Sourcing, $V_O = 0V$ $V_{IN} = 100 \text{mV}$	27	20 <b>15</b>	mA min
		Sinking, $V_O = 2.7V$ $V_{IN} = -100 \text{mV}$	28	22 <b>16</b>	mA min

# 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J$  = 25°C. V+ = 2.7V, V = 0V,  $V_{CM}$  = 1.0V,  $V_O$  = 1.35V and  $R_L$  > 1 M $\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ ( <i>Note 5</i> )	Units
SR	Slew Rate	(Note 7)	0.41	V/µs
GBW	Gain-Bandwidth Product		1	MHz
$\Phi_{m}$	Phase Margin		65	Deg.
G <sub>m</sub>	Gain Margin		10	dB
e <sub>n</sub>	Input-Referred Voltage Noise	f = 1 kHz, V <sub>CM</sub> = 0.5V	45	nV √Hz

Symbol	Parameter	Conditions	<b>Typ</b> ( <i>Note 5</i> )	Units
i <sub>n</sub>	Input-Referred Current Noise	f = 1 kHz	0.1	pA √Hz
THD	Total Harmonic Distortion	$f = 1 \text{ kHz}, A_V = +1$ $R_L = 600 \text{k}\Omega, V_{IN} = 1 \text{ V}_{PP}$	0.077	%
	Amp-to-Amp Isolation	(Note 8)	140	dB

# **5V DC Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for  $T_J$  = 25°C. V+ = 5V, V = 0V,  $V_{CM}$  = V+/2,  $V_O$  = V+/2 and  $R_L$  > 1 M $\Omega$ .**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits ( <i>Note 6</i> )	Units
V <sub>OS</sub>	Input Offset Voltage	LMV921 (Single)	-1.5	6 <b>8</b>	mV max
		LMV922 (Dual) LMV924 (Quad)	-1.5	8 <b>9.5</b>	mV max
TCV <sub>OS</sub>	Input Offset Voltage Average Drift	t	1/		μV/°C
I <sub>B</sub>	Input Bias Current		12	35 <b>50</b>	nA max
I <sub>OS</sub>	Input Offset Current	44	2	25 <b>40</b>	nA max
I <sub>S</sub>	Supply Current	LMV921 (Single)	160	210 <b>230</b>	
		LMV922 (Dual)	400	500 <b>700</b>	μA max
		LMV924 (Quad)	750	850 <b>980</b>	
CMRR	Common Mode Rejection Ratio	0V ≤ V <sub>CM</sub> ≤ 3.8V	86	62 <b>61</b>	dB
		$-0.2V \le V_{CM} \le 0V$ $5.0V \le V_{CM} \le 5.2V$	72	50	min
PSRR	Power Supply Rejection Ratio	$1.8V \le V + \le 5V$ $V_{CM} = 0.5V$	78	67 <b>62</b>	dB min
V <sub>CM</sub>	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 <b>0</b>	V min
			5.350	5.2 <b>5.0</b>	V max
A <sub>V</sub>	Voltage Gain LMV921 (Single)	$R_L = 600\Omega \text{ to } 2.5V$ $V_O = 0.2V \text{ to } 4.8V$	104	86 <b>82</b>	dB
		$R_L = 2k\Omega \text{ to } 2.5V$ $V_O = 0.2V \text{ to } 4.8V$	108	89 <b>85</b>	min
	Voltage Gain LMV922 (Dual)	$R_L = 600\Omega$ to 2.5V $V_O = 0.2V$ to 4.8V	90	72 68	dB
	LMV924 (Quad)	$R_L = 2k\Omega \text{ to } 2.5V$ $V_O = 0.2V \text{ to } 4.8V$	96	77 73	min

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V <sub>O</sub>	Output Swing	$R_L = 600\Omega$ to 2.5V $V_{IN} = \pm 100$ mV	4.895	4.865 <b>4.840</b>	V min
		IIV	0.1	0.135 <b>0.160</b>	V max
		$R_L = 2k\Omega$ to 2.5V $V_{IN} = \pm 100$ mV	4.965	4.945 <b>4.935</b>	V min
			0.035	0.065 <b>0.075</b>	V max
I <sub>O</sub>	Output Short Circuit Current	LMV921 Sourcing, $V_O = 0V$ $V_{IN} = 100$ mV	98	85 <b>68</b>	mA
		LMV922, LMV924 Sourcing, $V_O = 0V$ $V_{IN} = 100$ mV	60	35	min
		Sinking, $V_O = 5V$ $V_{IN} = -100 \text{mV}$	75	65 <b>45</b>	mA min

# **5V AC Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for  $T_J = 25$ °C.  $V^+ = 5V$ ,  $V_C = 0V$ ,  $V_{CM} = V^+/2$ ,  $V_O = 2.5V$  and  $R_L > 1$  M $\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.45	V/µs
GBW	Gain-Bandwidth Product		1	MHz
Φ <sub>m</sub>	Phase Margin		70	Deg
G <sub>m</sub>	Gain Margin		15	dB
e <sub>n</sub>	Input-Referred Voltage Noise	$f = 1 \text{ kHz}, V_{CM} = 1V$	45	nV √Hz
i <sub>n</sub>	Input-Referred Current Noise	f = 1 kHz	0.1	pA √Hz
THD	Total Harmonic Distortion	$f = 1 \text{ kHz}, A_V = +1$ $R_L = 600\Omega, V_O = 1 V_{PP}$	0.069	%
	Amp-to-Amp Isolation	(Note 8)	140	dB

**Note 1:** Absolute Maximum Ratings indicate limits beyond v hich damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k $\Omega$  in series with 100pF. Machine model, 200 $\Omega$  in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_{A}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

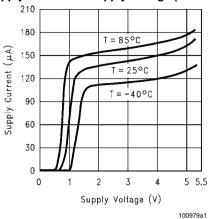
Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

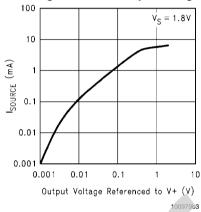
Note 8: Input referred, V+ = 5V and  $R_L = 100 k\Omega$  connected to 2.5V. Each amp excited in turn with 1kHz to produce  $V_Q = 3V_{PP}$ .

# **Typical Performance Characteristics** Unless otherwise specified, $V_S = +5V$ , single supply, $T_A = 25$ °C.

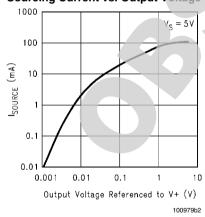
# Supply Current vs. Supply Voltage (LMV921)



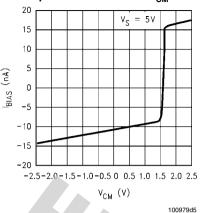
#### Sourcing Current vs. Output Voltage



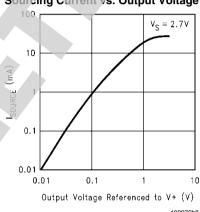
# Sourcing Current vs. Output Voltage



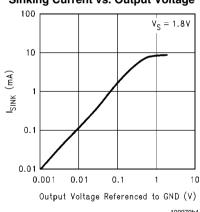
# Input Bias Current vs. V<sub>CM</sub>



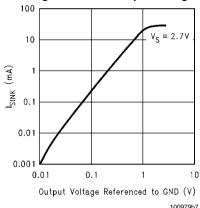
## Sourcing Current vs. Output Voltage



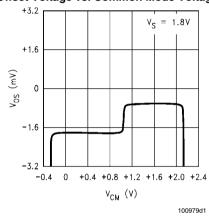
## Sinking Current vs. Output Voltage



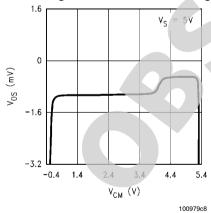
# Sinking Current vs. Output Voltage



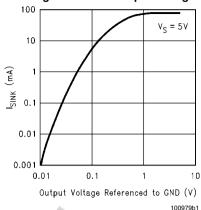
## Offset Voltage vs. Common Mode Voltage



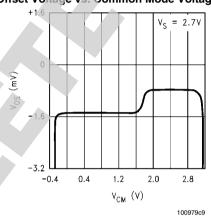
# Offset Voltage vs. Common Mode Voltage



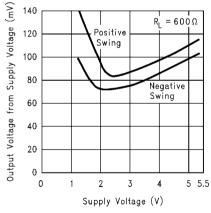
#### Sinking Current vs. Output Voltage



## Offset Voltage vs. Common Mode Voltage

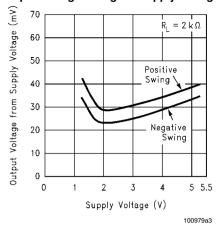


# Output Voltage Swing vs. Supply Voltage

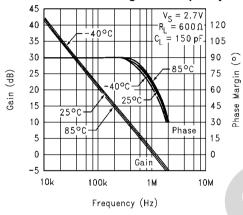


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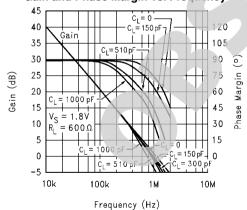
#### **Output Voltage Swing vs. Supply Voltage**



## Gain and Phase Margin vs. Frequency

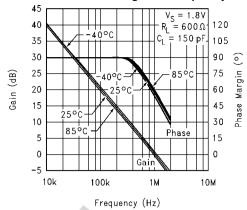


# Gain and Phase Margin vs. Frequency



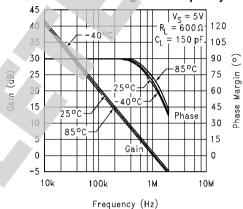
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## Gain and Phase Margin vs. Frequency



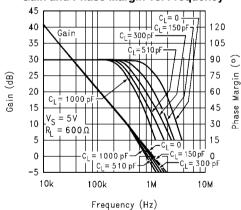
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#### Gain and Phase Margin vs. Frequency

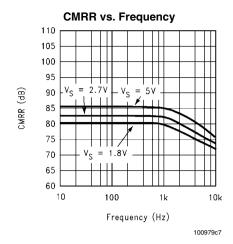


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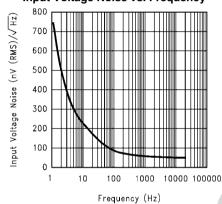
# Gain and Phase Margin vs. Frequency



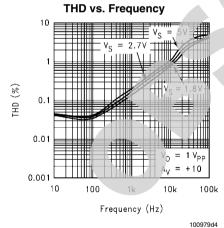
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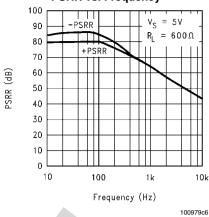




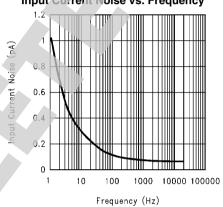
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#### PSRR vs. Frequency

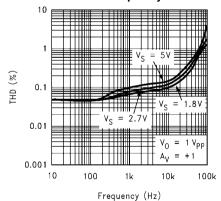


# Input Current Noise vs. Frequency



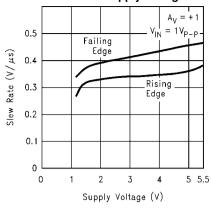
100979f5

#### THD vs. Frequency



100979d3

#### Slew Rate vs. Supply Voltage



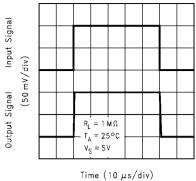
**Small Signal Non-Inverting Response** 

Input Signal

Output Signal

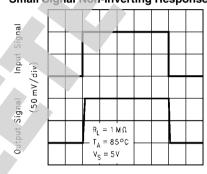
(50 mV/div)

#### **Small Signal Non-Inverting Response**



# 100979e3

# Small Signal Non-Inverting Response



#### Time (10 $\mu$ s/div)

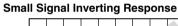
#### 100979e4

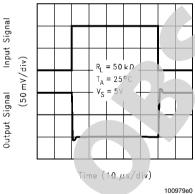
# Time (10 μs/div)

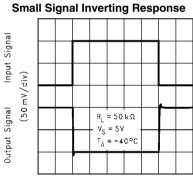
 $R_L = 1 M\Omega$ 

V<sub>S</sub> = 5V

= -40°C



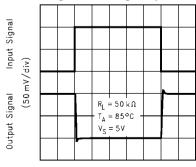




Time (10  $\mu$ s/div)

#### 100979d9

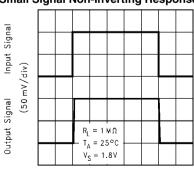
## **Small Signal Inverting Response**



Time (10  $\mu$ s/div)

100979d8

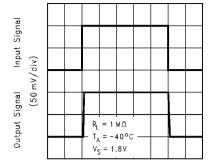
## **Small Signal Non-Inverting Response**



Time (10  $\mu s/div$ )

100979e6

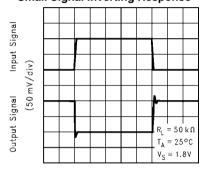
#### **Small Signal Non-Inverting Response**



Time (10  $\mu$ s/div)

100979e7

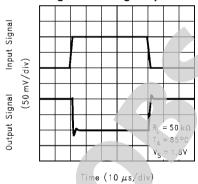
# **Small Signal Inverting Response**



Time (10  $\mu$ s/div)

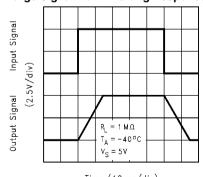
100979g3

## **Small Signal Inverting Response**



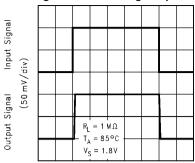
1009

\*Large Signal Non-inverting Response



Time (10  $\mu$ s/div)

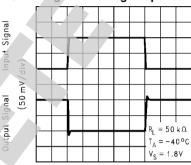
#### **Small Signal Non-Inverting Response**



Time (10  $\mu$ s/div)

100979e5

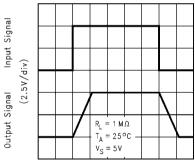
## **Small Signal Inverting Response**



Time (10  $\mu$ s/div)

100979g2

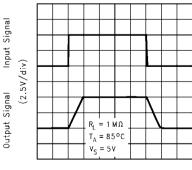
# \*Large Signal Non-Inverting Response



Time (10  $\mu s/div$ )

100979f0

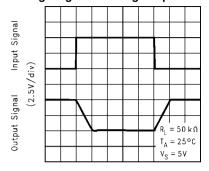
## \*Large Signal Non-Inverting Response



Time (10  $\mu \mathrm{s/div}$ )

100979g0

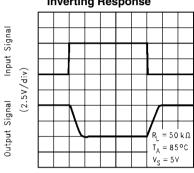
#### \*Large Signal Inverting Response



Time (10  $\mu$ s/div)

100979f9

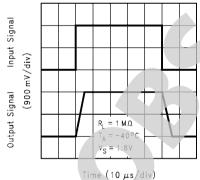
# \*Large Signal Inverting Response



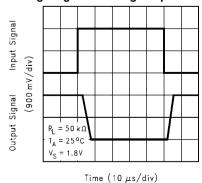
Time (10  $\mu$ s/div)

100979f7

# \*Large Signal Non-Inverting Response

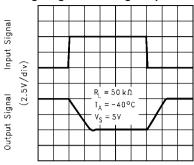


## \*Large Signal Inverting Response



100979d6

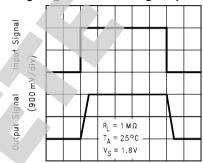
#### \*Large Signal Inverting Response



Time (10  $\mu$ s/div)

100979f8

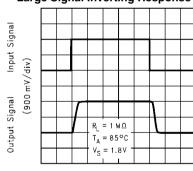
## \*Large Signal Non-Inverting Response



Time (10  $\mu$ s/div)

100979f1

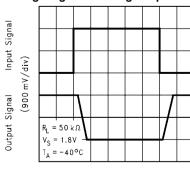
# \*Large Signal Inverting Response



Time (10  $\mu$ s/div)

100979f

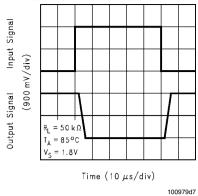
# \*Large Signal Inverting Response



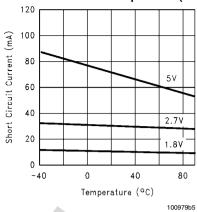
Time (10  $\mu$ s/div)

100979e1

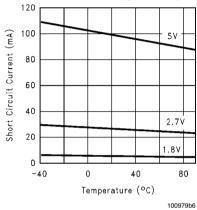
## \*Large Signal Inverting Response



#### **Short Circuit Current vs. Temperature (sinking)**



# **Short Circuit Current vs. Temperature (sourcing)**



\*For large signal pulse response in the unity gain follower configuration, the input is 5mV below the positive rail and 5mV above the negative rail at 25°C and 85°C. At –40°C, input is 10mV below the positive rail and 10mV above the negative rail.

# **Application Note**

#### 1.0 Unity Gain Pulse Response Considerations

The unity-gain follower is the most sensitive configuration to capacitive loading. The LMV921/LMV922/LMV924 family can directly drive 1nF in a unity-gain with minimal ringing. Direct capacitive loading reduces the phase margin of the amplifier. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. The pulse response can be improved by adding a pull up resistor as shown in *Figure 1* 

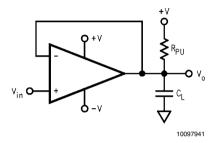


FIGURE 1. Using a Pull-Up Resistor at the Output for Stabilizing Capacitive Loads

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in *Figure 2*.

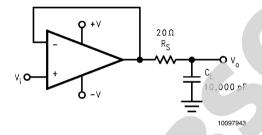


FIGURE 2. Using an Isolation Resistor to Drive Heavy Capacitive Loads

#### 2.0 Input Bias Current Consideration

The LMV921/LMV922/LMV924 family has a bipolar input stage. The typical input bias current ( $I_B$ ) is 12nA. The input bias current can develop a significant offset voltage. This offset is primarily due to  $I_B$  flowing through the negative feedback resistor,  $R_F$ . For example, if  $I_B$  is 50nA (max room) and  $R_F$  is 100k $\Omega$ , then an offset voltage of 5mV will develop ( $V_{OS} = I_B X R_F$ ). Using a compensation resistor ( $R_C$ ), as shown in *Figure 3*, cancels this affect. But the input offset current ( $I_{OS}$ ) will still contribute to an offset voltage in the same manner.

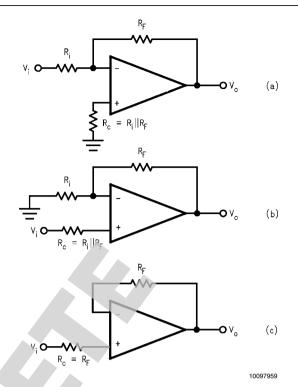


FIGURE 3. Canceling the Voltage Offset Effect of Input
Bias Current

#### 3.0 Operating Supply Voltage

The LMV921/LMV922/LMV924 family is guaranteed to operate from 1.8V to 5.0V. They will begin to function at power voltages as low as 1.2V at room temperature when unloaded. Start up voltage increases to 1.5V when the amplifier is fully loaded ( $600\Omega$  to mid-supply). Below 1.2V the output voltage is not guaranteed to follow the input. *Figure 4* below shows the output voltage vs. supply voltage with the LMV921/LMV922/LMV924 configured as a voltage follower at room temperature.

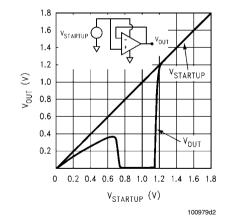


FIGURE 4.

#### 4.0 Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV921/LMV922/LMV924 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V- and the NPN stage senses common mode voltage near V+. The transition from the PNP stage to NPN stage occurs 1V below V+. Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below V+ as shown in the  $V_{\text{OS}}$  vs.  $V_{\text{CM}}$  curves.

This  $V_{OS}$  crossover point can create problems for both DC and AC coupled signals if proper care is not taken. For large input signals that include the  $V_{OS}$  crossover point in their dynamic range, this will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with  $V_S = 5V$ , a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of -1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the  $V_{OS}$  cross-over point.

For small signals, this transition in  $V_{OS}$  shows up as a  $V_{CM}$  dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the  $V_{OS}$  crossover point.

In addition to the rail-to-rail performance, the output stage can provide enough output current to drive  $600\Omega$  loads. Because of the high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

#### 5.0 Power-Supply Considerations

The LMV921/LMV922/LMV924 are ideally suited for use with most battery-powered systems. The LMV921/LMV922/LMV924 operate from a single +1.8V to +5.0V supply and consumes about 145µA of supply current per Amplifier. A high power supply rejection ratio of 78dB allows the amplifier to be powered directly off a decaying battery voltage extending battery life.

Table 1 lists a variety of typical battery types. Batteries have different voltage ratings; operating voltage is the battery voltage under nominal load. End-of-Life voltage is defined as the voltage at which 100% of the usable power of the battery is consumed. Table 1 also shows the typical operating time of the LMV921.

#### 6.0 Distortion

The two main contributors of distortion in LMV921/LMV922/LMV924 family is:

- 1. Output crossover distortion occurs as the output transitions from sourcing current to sinking current.
- 2. Input crossover distortion occurs as the input switches from NPN to PNP transistor at the input stage.

To decrease crossover distortion:

- 1. Increase the load resistance. This lowers the output crossover distortion but has no effect on the input crossover distortion.
- 2. Operate from a single supply with the output always sourcing current.
- 3. Limit the input voltage swing for large signals between ground and one volt below the positive supply.
- 4. Operate in inverting configuration to eliminate common mode induced distortion.
- 5. Avoid small input signal around the input crossover region. The discontinuity in the offset voltage will effect the gain, CM-RR and PSRR.

TABLE 1. LMV921 Characteristics with Typical Battery Systems.

Battery Type	Operating Voltage (V)	End-of-Life Voltage (V)	Capacity AA Size (mA - h)	LMV921 Operating time (Hours)
Alkaline	1.5	0.9	1000	6802
Lithium	2.7	2.0	1000	6802
Ni - Cad	1.2	0.9	375	2551
NMH	1.2	1.0	500	3401

# **Typical Applications**

# 1.0 Half-wave Rectifier with Rail-To-Ground Output Swing

Since the LMV921 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In *Figure 5* the circuit is referenced to ground, while in *Figure 6* the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV921 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R<sub>I</sub> should be large enough not to load the LMV921.

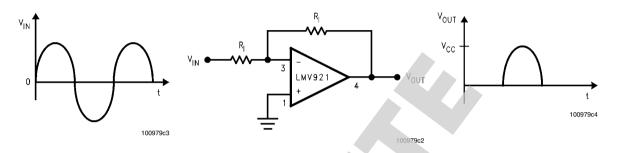


FIGURE 5. Half-Wave Rectifier with Rail-To-Ground Output Swing Referenced to Ground

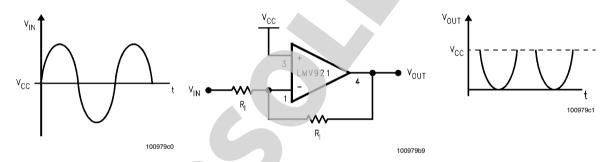


FIGURE 6. Half-Wave Rectifier with Negative-Going Output Referenced to V<sub>CC</sub>

# 2.0 Instrumentation Amplifier with Rail-To-Rail Input and Output

Using three of the LMV924 Amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common mode voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get unity gain, the amplifier must be run at high loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. Using the LMV924 eliminates all of these problems. In this example, amplifiers A and B act as buffers to the dif-

In this example, amplifiers A and B act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching  $R_1$ - $R_2$  with  $R_3$ - $R_4$ . The gain is set by the ratio of  $R_2$ / $R_4$  and  $R_2$  should equal  $R_4$ 

The gain is set by the ratio of  $\rm R_2/R_1$  and  $\rm R_3$  should equal  $\rm R_1$  and  $\rm R_4$  equal  $\rm R_2$ .

With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater that the supplies or limiting will occur. For additional applications, see National Semiconductor application notes AN–29, AN–31, AN–71, and AN–127.

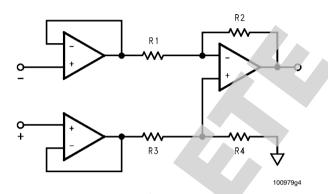
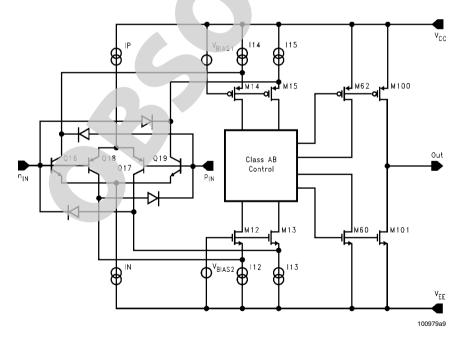
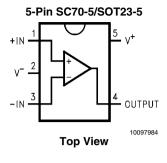


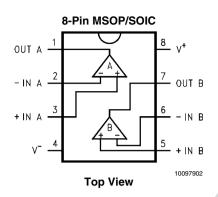
FIGURE 7. Rail-to-rail instrumentation amplifier

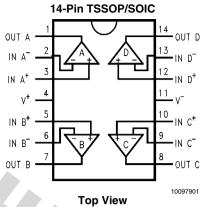
# **Simplified Schematic**



# **Connection Diagrams**



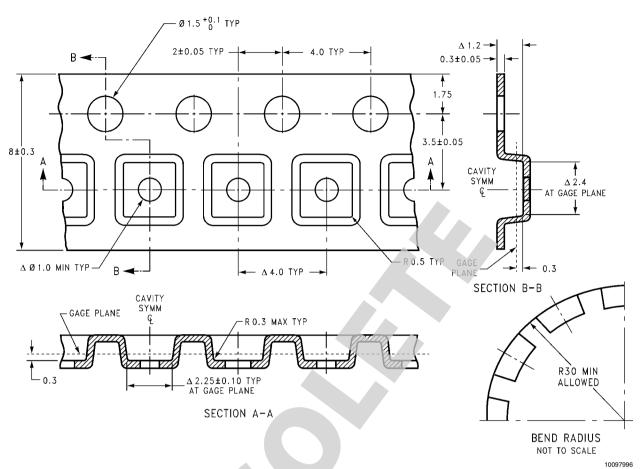




# **Ordering Information**

Package	Temperature Range Industrial -40°C to +85°C	Package Marking	Transport Media	NSC Drawing	
5-Pin SC70-5	LMV921M7	A21	1k Units Tape and Reel	MAA05A	
	LMV921M7X	A21	3k Units Tape and Reel		
5-Pin SOT-23	LMV921M5	<b>A</b> 29A	1k Units Tape and Reel	MEGEA	
	LMV921M5X	A29A	3k Units Tape and Reel	MF05A	
8-Pin MSOP	LMV922MM	LMV922	1k Units Tape and Reel	14114.004	
	LMV922MMX	LMV922	3.5k Units Tape and Reel	MUA08A	
14-Pin TSSOP	LMV924MT	LMV924	Rails	MTC14	
	LMV924MTX	LMV924	2.5k Units Tape and Reel	MTC14	
8-Pin SOIC	LMV922M	LMV922M	Rails	M08A	
	LMV922MX	LMV922M	2.5k Units Tape and Reel		
14-Pin SOIC	LMV924M	LMV924M	Rails	N444A	
	LMV924MX	LMV924M	2.5k Units Tape and Reel	M14A	

# **SC70-5 Tape Dimensions**

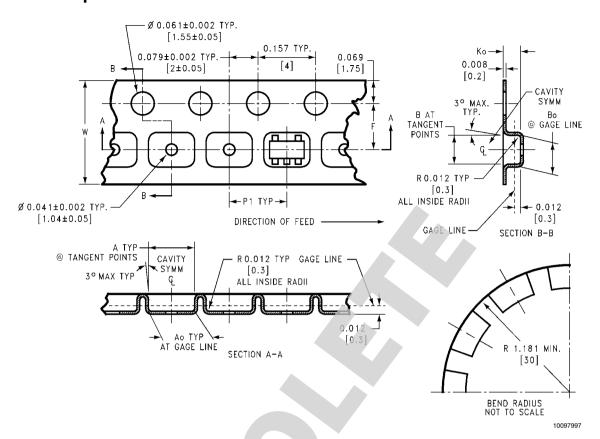


# SOT23-5 and SC70-5 Tape Format

# **Tape Format**

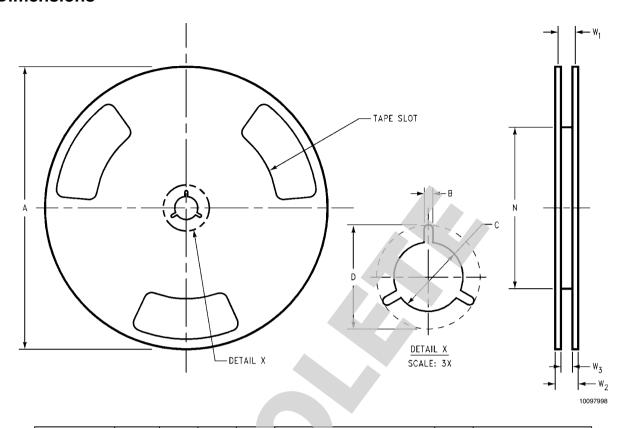
Tape Section	# Cavities	Cavity Status	Cover Tape Status	
Leader	0 (min)	Empty	Sealed	
(Start End)	75 (min)	Empty	Sealed	
Carrier	3000	Filled	Sealed	
	250	Filled	Sealed	
Trailer	125 (min)	Empty	Sealed	
(Hub End)	0 (min)	Empty	Sealed	

# **SOT23-5 Tape Dimensions**



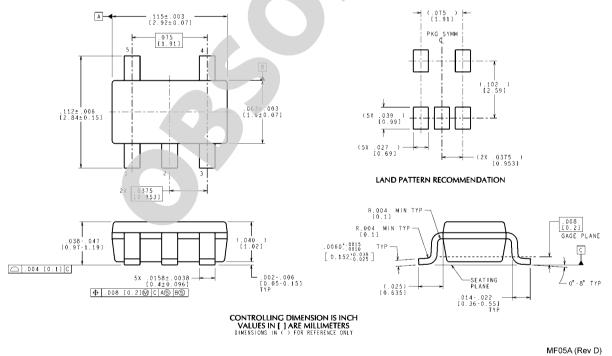
8 mm	0.130	0.124	0.130	0.126	0.138 ±0.002	0.055 ±0.004	0.157	0.315 ±0.012
	(3.3)	(3.15)	(3.3)	(3.2)	(3.5 ±0.05)	(1.4 ±0.11)	(4)	(8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

# SOT23-5 and SC70-5 Reel Dimensions

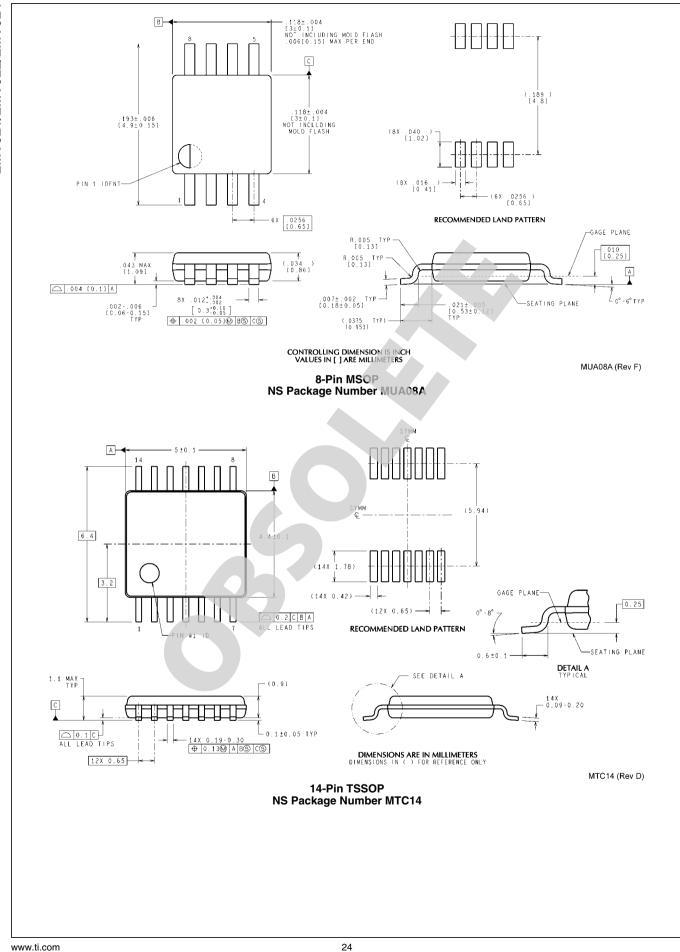


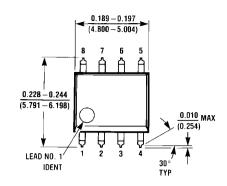
8 mm	7.00	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1+ 0.078/-0.039
	330.00	1.50	13.00	20.20	55.00	8.40 + 1.50/-0.00	14.40	W1 + 2.00/-1.00
Tape Size	Α	В	С	D	N	W1	W2	W3

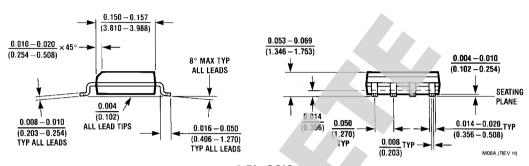
# Physical Dimensions inches (millimeters) unless otherwise noted 2+0.1 SYMM ¢ 0.65 -PIN 1 INDEX AREA 1.8-2.4 1.25±0.1 (5X 0.4) LAND PATTERN RECOMMENDATION R0.025 MIN GAGE PLANE RO.025 MIN TY 0.8-1.1 0.2 С 0.1 C SEATING PLANE-5X 0.4±0.05 (0.515 TYP) DIMENSIONS ARE IN MILLIMETERS DIMENSIONS IN ( ).FOR REFENEENCE ONLY MAA05A (Rev D) **NS Package Number MAA05A**



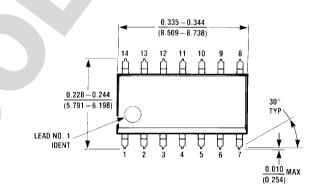
5-Pin SOT-23 NS Package Number MF05A

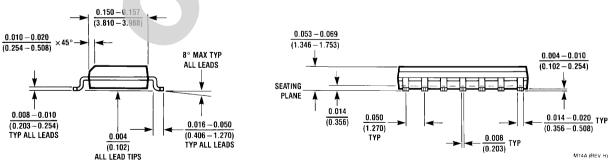






8-Pin SOIC NS Package Number M08A





14-Pin SOIC NS Package Number MA14

# **Notes**

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Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps		
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy		
DSP	dsp.ti.com	Industrial	www.ti.com/industrial		
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical		
Interface	interface.ti.com	Security	www.ti.com/security		
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics- defense		
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