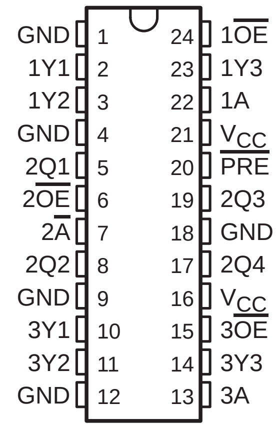
CDC330 CLOCK DRIVER WITH 3-STATE OUTPUTS

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Two Banks Distribute One Clock Input to Three Same-Frequency Clock Outputs**
- **One Bank Distributes One Clock Input to Four Half-Frequency Clock Outputs**
- **Internal Power-Up Circuit**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Symmetrical Output Drive (–32-mA I_{OH}, 32-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaged in Plastic Small-Outline Package**

**DW PACKAGE
(TOP VIEW)**



description

The CDC330 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring output signals at both the primary clock frequency and one-half the primary clock frequency.

This device contains two banks that fan out one input to three same-frequency outputs and one bank that fans out one input to four half-frequency outputs with minimum skew for clock distribution. Each bank of Y outputs switch in phase and at the same frequency as its clock (A) input. The four Q outputs switch at one-half the frequency of their clock (2$\overline{A}$) input.

When the output-enable (2$\overline{OE}$) input is low and the preset ($\overline{PRE}$) input is high, the Q outputs toggle on high-to-low transitions of 2$\overline{A}$. Taking $\overline{PRE}$ low asynchronously presets the Q outputs to the high level. When a bank's $\overline{OE}$ input is high, the outputs are in the high-impedance state.

The CDC330 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

INPUTS		OUTPUTS
n$\overline{OE}$	**nA**	**nY1 – nY3**
H	X	Z
L	L	L
L	H	H

n = 1, 3

INPUTS			OUTPUTS
2$\overline{OE}$	**$\overline{PRE}$**	**2$\overline{A}$**	**2Q1 – 2Q3**
H	X	X	Z
L	L	L	H
L	H	↓	Toggle

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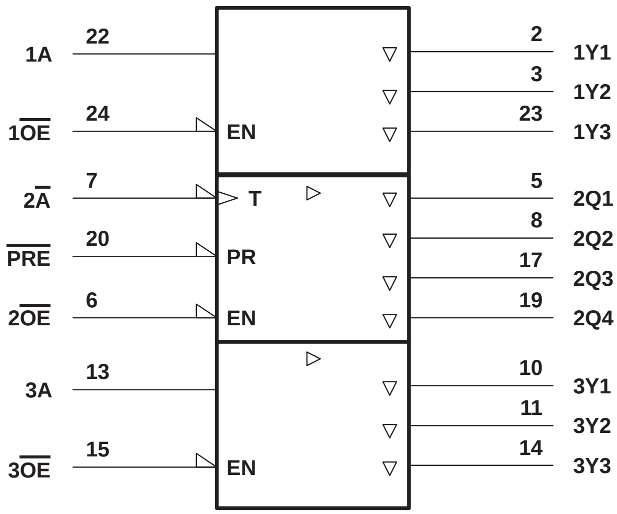
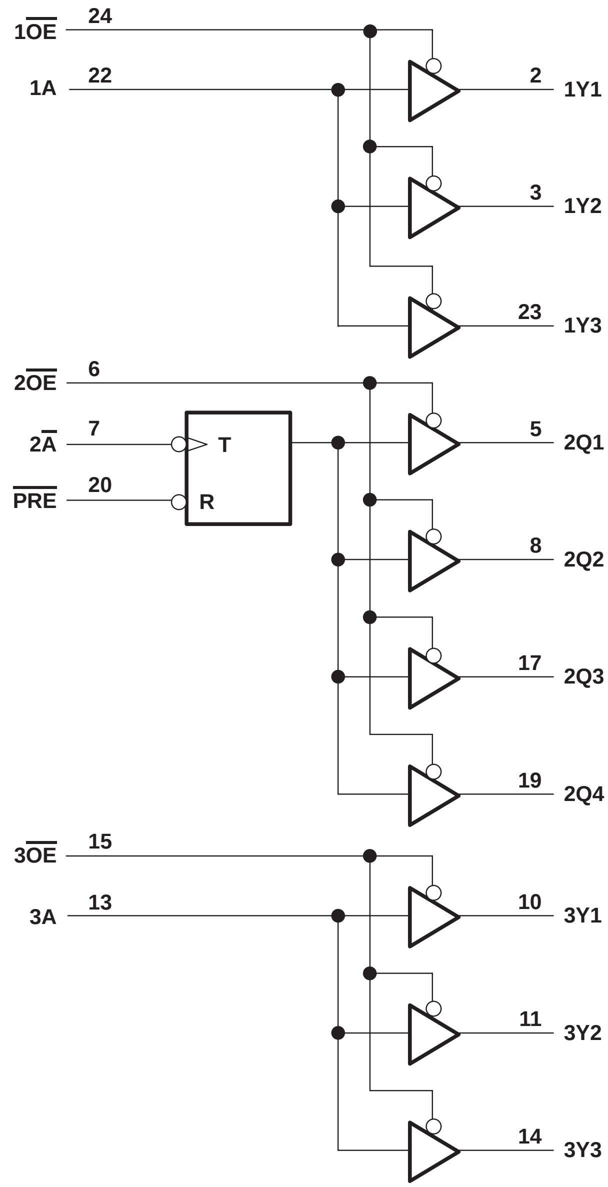
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . 96 mA
Input clamp current, I_{IK} (V_I < 0) . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . 1.6 W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 32 mA		2			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA				0.5	V
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				50	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.5 V				–50	µA
I_{OZ}	V_{CC} = 5.25 V,	V_O = V_{CC} or GND				±50	µA
I_O§	V_{CC} = 5.25 V,	V_O = 2.5 V		–30		–180	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		11	40	mA
			Outputs low		15	30	
			Outputs disabled		10	30	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = 2.5 V or 0.5 V				9		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	1A/3A (duty cycle 40 – 60%)		67	MHz
		$2\overline{A}$ (duty cycle 40 – 60%)		100	MHz
t_w	Pulse duration	1A/3A low	5.9		ns
		1A/3A high	5.9		
		$2\overline{A}$ low	2.8		
		$2\overline{A}$ high	4.5		
		$\overline{PRE}$ low	3		
t_{su}	Setup time	$\overline{PRE}$ inactive before $2\overline{A}\downarrow$	2		ns

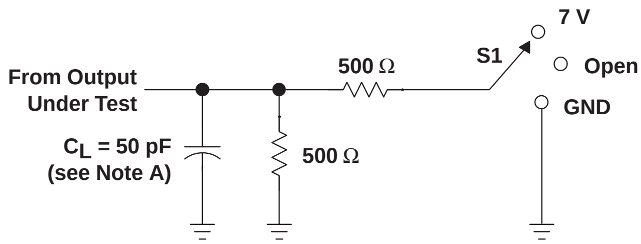
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}†	1A or 3A	Any 1Y or 3Y	67		MHz
	$2\overline{A}$	Any Q	100		
t_{PLH}	Any A or $\overline{A}$	Any Y or Q		11	ns
t_{PHL}				10.5	
t_{PHL}	$\overline{PRE}$	Any Q		12.5	ns
t_{PZH}	Any $\overline{OE}$	Any Y or Q		9	ns
t_{PZL}				8.5	
t_{PHZ}	Any $\overline{OE}$	Any Y or Q		8.5	ns
t_{PLZ}				9	
$t_{sk(o)}$	1A	Any 1Y		0.4	ns
	3A	Any 3Y		0.4	
	1A or 3A	Any 1Y or 3Y		0.5	
	$2\overline{A}$	Any Q		0.4	
$t_{sk(pr)}$	Any A or $\overline{A}$	Any Y or Q		1	ns

† Duty cycle 40 – 60%

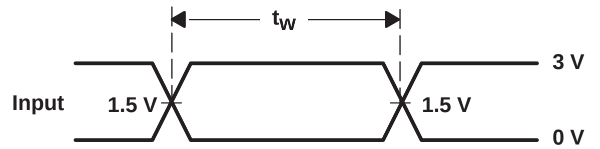
NOTE 4: All specifications are valid only for all outputs switching.

PARAMETER MEASUREMENT INFORMATION

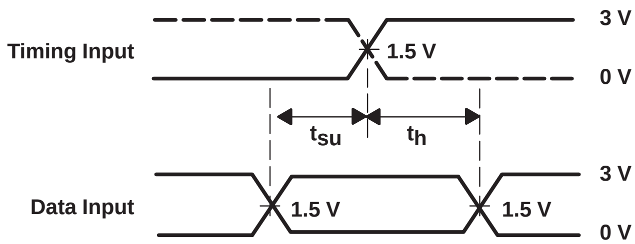


LOAD CIRCUIT

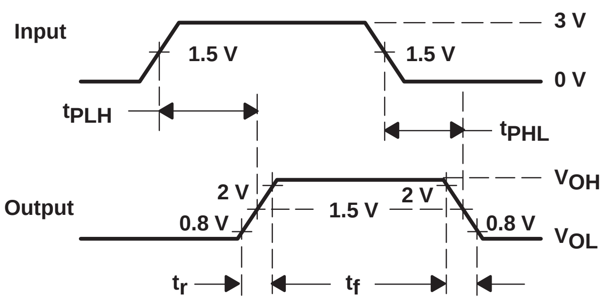
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



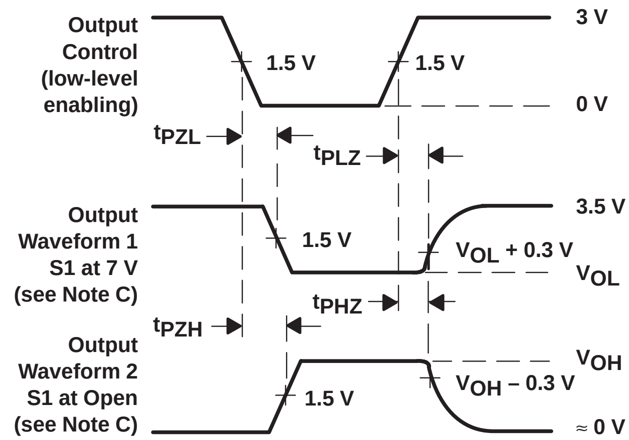
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

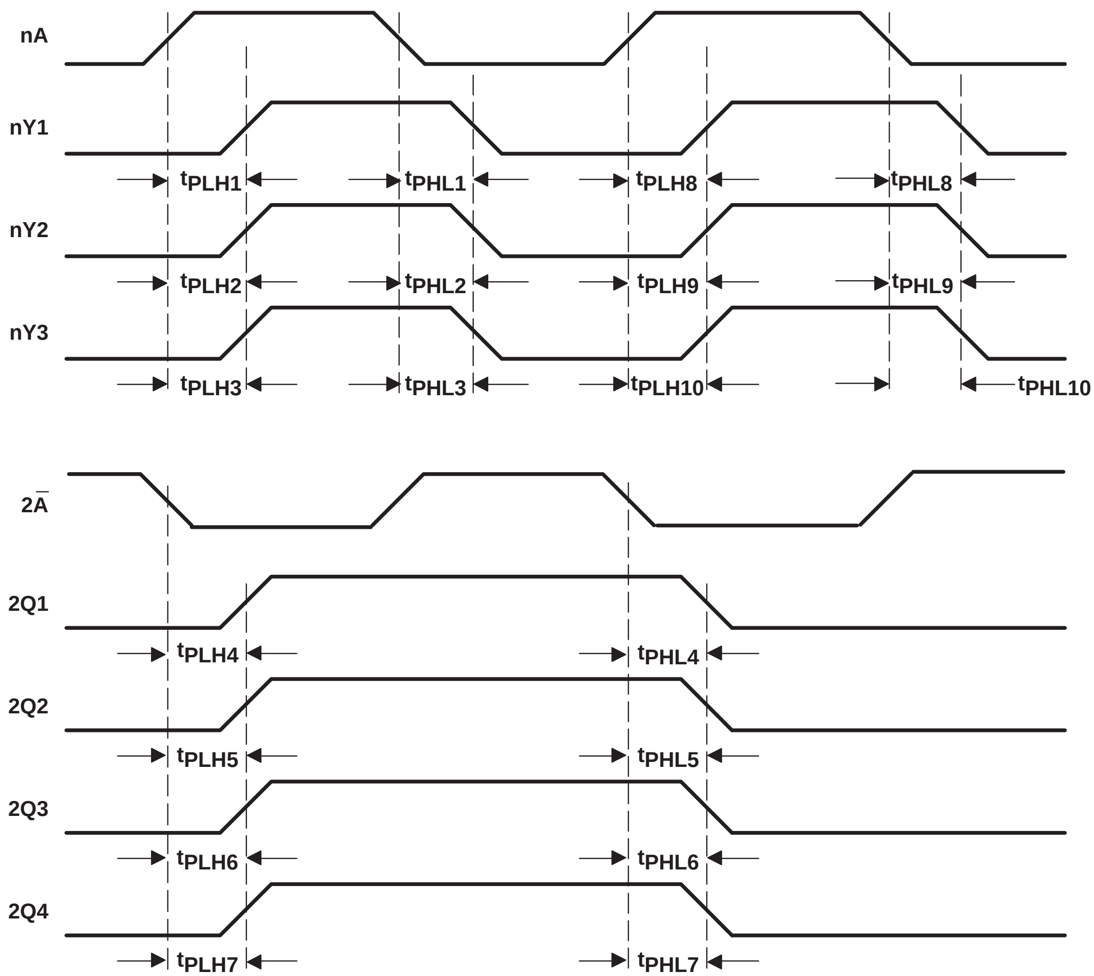
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- – The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3)
- – The difference between the fastest and slowest of t_{PLHn} (n = 4, 5, 6, 7)
- – The difference between the fastest and slowest of t_{PLHn} (n = 8, 9, 10)
- – The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3)
- – The difference between the fastest and slowest of t_{PHLn} (n = 4, 5, 6, 7)
- – The difference between the fastest and slowest of t_{PHLn} (n = 8, 9, 10)

B. Process skew, $t_{sk(pr)}$, is calculated the same as output skew, $t_{sk(o)}$, across multiple CDC330 devices under identical operating conditions.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CDC330DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
CDC330DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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