National Semiconductor

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November 1993

100115
Low-Skew Quad Clock Driver

General Description

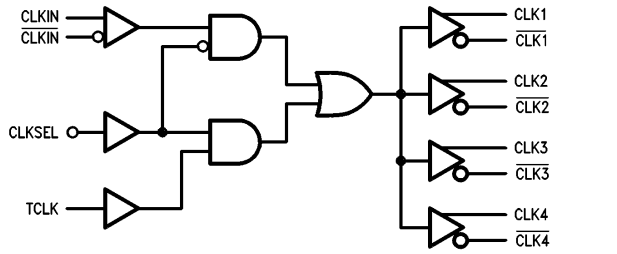
The 100115 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing.

*Replaced by 100315

Features

- Low output to output skew (≤75 ps)
- Differential inputs and outputs
- Small outline package
- Ideal for applications which require the low skew distribution of a clock signal to multiple outputs
- Secondary clock available for system level testing

Logic Diagram



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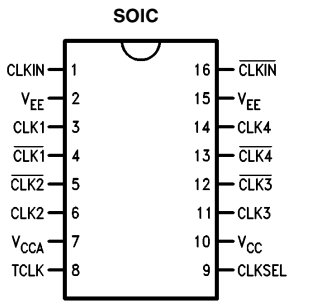
Connection Diagram



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Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input†
CLKSEL	Clock Input Select†

†TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{\text{CLKIN}}$	TCLK	CLK_N	$\overline{CLK_N}$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Single-Ended Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the ''worst case'' value for the parameter. Since these ''worst case'' values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under ''worst case'' conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

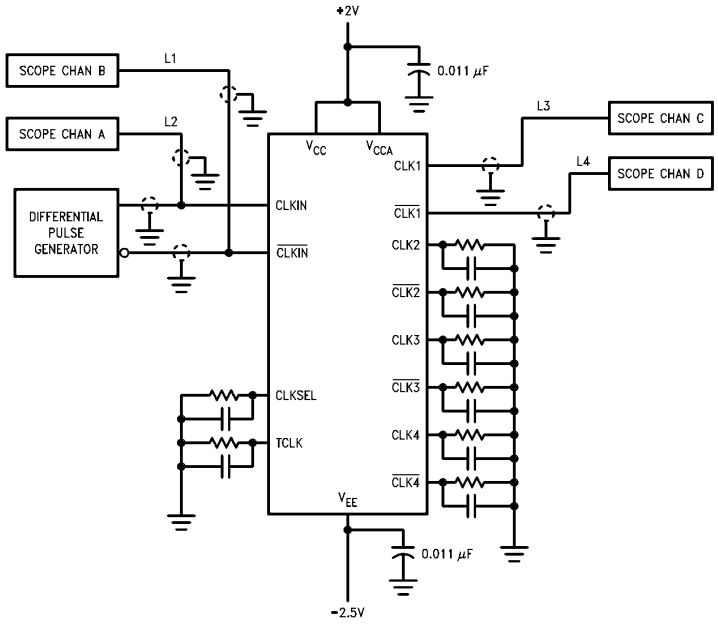
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V	V	
I_{IH}	Input High Current CLKIN, $\overline{CLKIN}$ TCLK CLKSEL			 107 300 260	 μA μA μA	V_{IN} = $V_{IH(Max)}$
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−70		−30	mA	

AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.63	0.83	0.65	0.85	0.70	0.93	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.60	1.40	0.60	1.40	0.60	1.40	ns	*Figures 1, 2*
$t_{S\ G-G}$	Skew Gate to Gate (Note 1)		75		75		75	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	0.80	0.30	0.75	0.25	0.75	ns	*Figures 1, 4*

Note 1: Maximum output skew for any one device.



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Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit

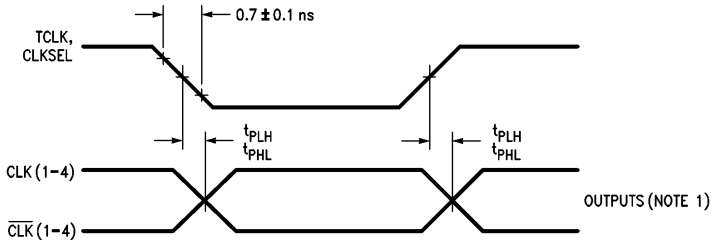

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FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs

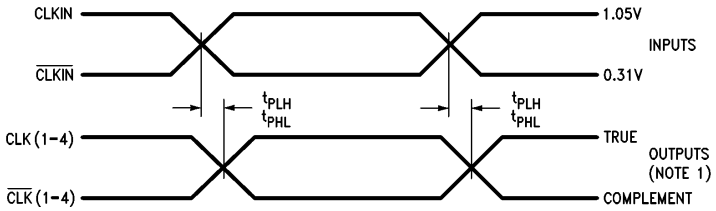

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FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs

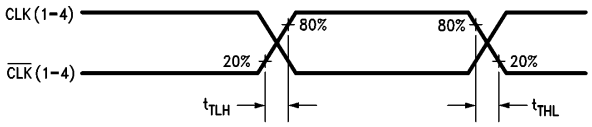

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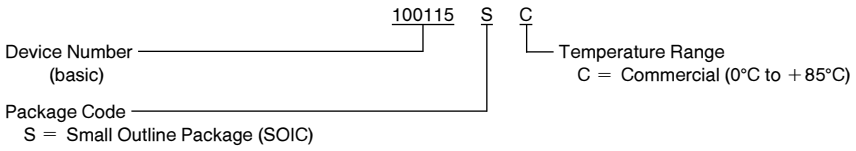
FIGURE 4. Transition Times

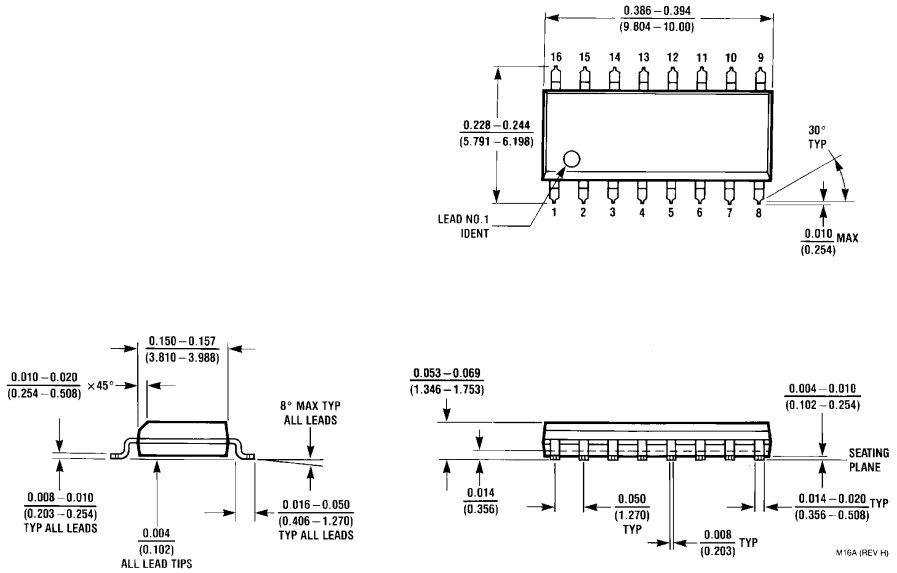
Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)



16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

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