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SSI 32P4782A
100 Mbit/s Read Channel Device

Advance Information

January 1995

DESCRIPTION

The 32P4782A device is a high performance BiCMOS single chip read channel IC that, together with the 32D4680 time base generator, contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, servo functions, data synchronizer, window shift, write precomp and 1,7 RLL ENDEC. Data rates from 33 to 100 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor.

The programmable functions of the 32P4782A device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The 32P4782A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL

- **Programmable data rate, internal DAC controlled: 33 to 100 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation (550 mW typical @ 80 Mbit/s, 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode < 8 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

AGC

- **LowZ and fast decay timings independently set by two external resistors**
- **fast decay current set by an external resistor**
- **Low Drift AGC Hold circuitry**

(continued)

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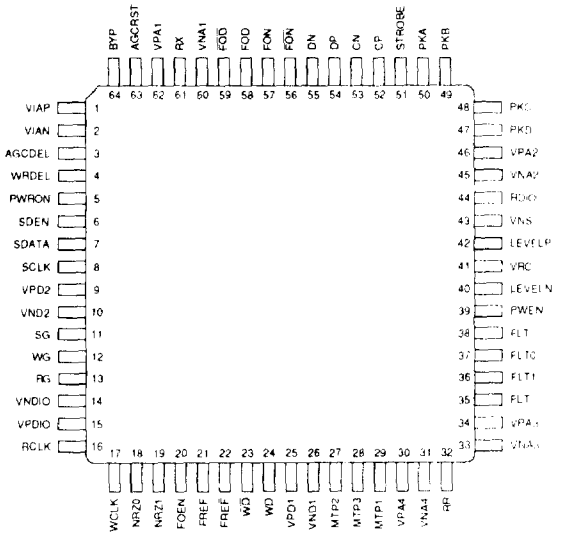
PIN DIAGRAM



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32P4782A
100 Mbit/s Read Channel Device

FEATURES (continued)

AGC (continued)

- Separate read and servo AGC levels (4-bit DAC)
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Wide bandwidth, high precision multirate charge pump

PULSE DETECTOR

- DP, DN and CP, CN LowZ pin for rapid transient recovery
- Pulse qualification circuitry can be configured via serial port to support one of three modes of operation:
  - bit by bit qualification with polarity check
  - bit by bit qualification without polarity check
  - analog Viterbi detector
- Independent control of positive and negative thresholds levels in the data comparators
- CMOS RDIO signal output for servo timing support
- 0.3 ns max. pulse pairing with sine wave input
- Programmable fixed positive and negative threshold

SERVO CAPTURE

- 4-burst servo capture with A, B, C and D outputs.
- Separate full wave rectifier connected to filter differentiated output.
- Separate registers for filter cutoff, AGC level and qualification threshold during servo mode

PROGRAMMABLE FILTER

- External hold capacitors and reset line required
- Cutoff frequency programmable via serial port:
  - 9 to 27 MHz (4 - 9 MHz at degraded specs for filtering in servo mode)
- Advanced architecture minimizes filter settling characteristics when switching between servo mode and data mode
- Programmable boost/equalization range of 0 to 12 dB
- Separate boost for servo and read mode
- Programmable group delay equalization with asymmetric zeroes control
- Matched normal and differentiated outputs
- ±15% fc accuracy over operating temperature and supply ranges
- ±2% maximum group delay variation (≤500 ps @ fc = 27 MHz)
- Less than 1% total harmonic distortion
- No external filter components required

DATA SEPARATOR

- High performance dual-bit NRZ interface
- Integrated 1,7 RLL encoder decoder
- Fast acquisition phase lock loop with zero phase restart technique
- Fully integrated data separator
  - no external delay lines or active components are required
  - no external active PLL components are required
- Programmable decode window symmetry control via serial port
  - window shift control ±50% (4-bit)
  - delayed read data and VCO clock monitor points
- Programmable write precompensation (3-bit)
  - independent control of two precompensation levels

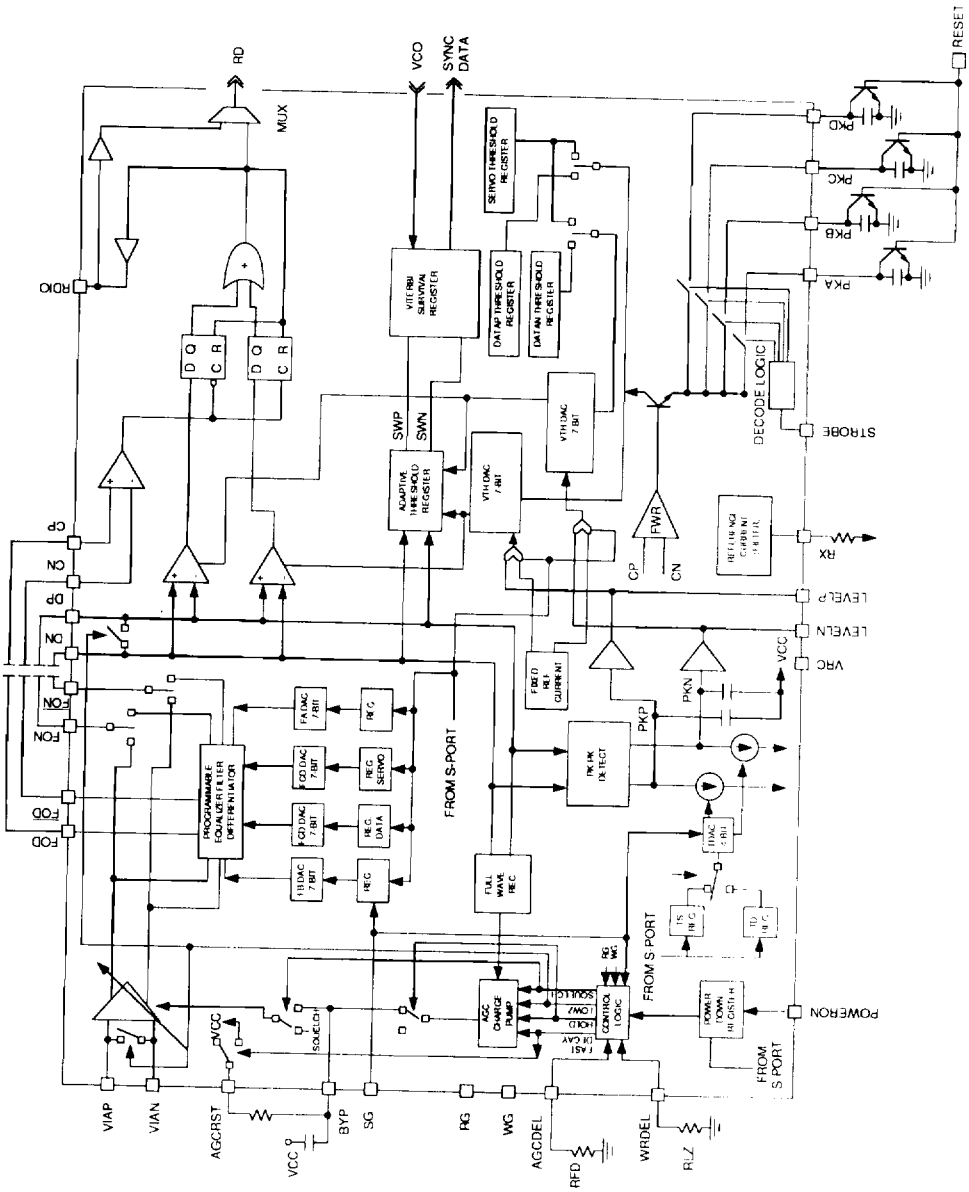


FIGURE 1: Block Diagram – Fron End

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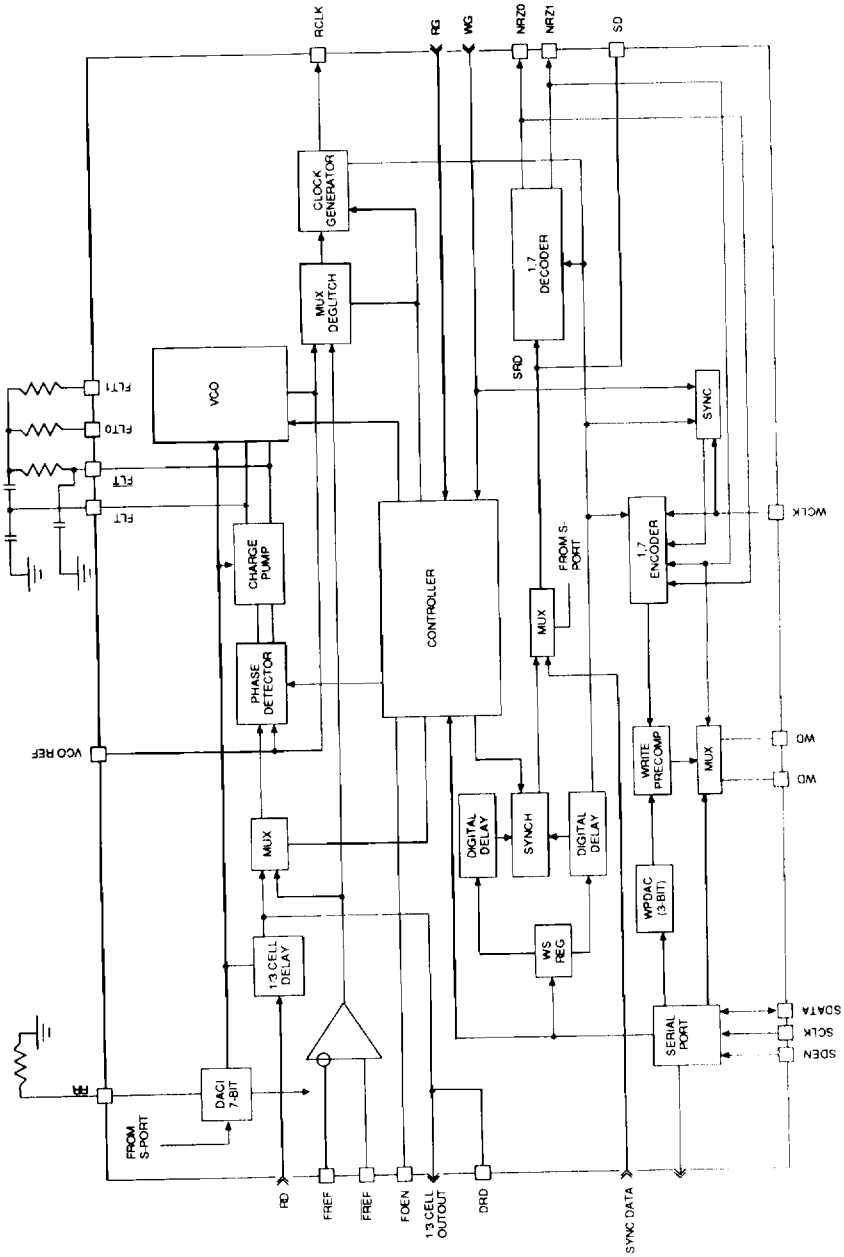

FIGURE 2: Block Diagram– Back End

FUNCTIONAL DESCRIPTION

The SSI 32P4782A implements a high performance complete read channel, including pulse detector, servo functions, programmable active filter, data synchronizer and 1,7 ENDEC, at data rates up to 100 Mbit/s. A circuit block diagram is shown in Figures 1 and 2.

Most critical system parameters are user-controlled by writing to a bank of sixteen 8-bit registers. These registers can be written to or read back via a 3 line bi-directional serial interface. Upon application of power to the device, these registers must be written to appropriate state as they may come up at random.

AGC & PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier (AGC), a precision wide bandwidth fullwave rectifier, and a multirate charge pump. The entire signal path is fully differential to minimize external noise pick up.

AGC Circuit

The gain of the AGC amplifier is controlled by the voltage VBYP stored on the hold capacitor at the BYP pin. A multirate charge pump drives the hold capacitor with currents that depend on the instantaneous differential voltage at the DP,DN pins as compared to an internal reference voltage. When the signal at DP, DN is greater than 100% of the programmed AGC level, the nominal attack current of approximatlely 0.19 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. A constant decay current of approximately 4.2 µA acts to increase the amplifier gain when the signal at DP,DN is less than the programmed AGC level. The large ratio (0.18 mA / 4.2 µA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is controlled by the user through a resistor connected between the AGCRST and the BYP pins. This current will remain turned 'on' until the signal at DP, DN exceeds 125% of the programmed AGC level.

The AGC loop has built in a power supply tracking feature which makes the voltage at DP, DN linear function of the power supply as outlined by the equation below:

$$V_{Dp,Dn} = (0.206 \cdot Vcc) + 0.049\ Vp\text{-}pd$$

In read mode and write mode, the reference voltage for the AGC charge pump is a nominal 1.1 Vp-pd at DP, DN. When SG is set high (servo mode), the reference voltage for the AGC charge pump is adjusted by a 4-bit DAC (DACA) controlled through the serial port register AGC1. The DAC output voltage is offset so that 1111 results in a 0.88 Vp-pd output, and 0000 results in a 1.1 Vp-pd output:

$$VAGC = 1.10 - (DACA \times 0.01667)\ Vp\text{-}pd$$

where DACA is the decimal value of the DACA register.

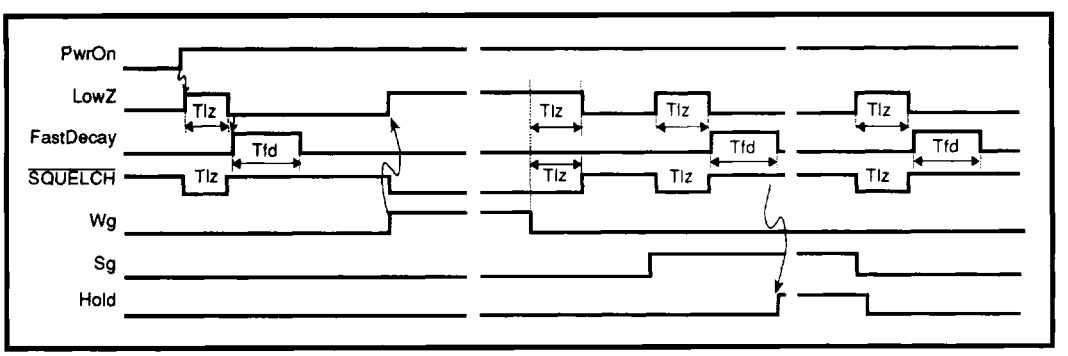

FIGURE 3: AGC Timing

AGC & PULSE DETECTOR CIRCUIT DESCRIPTION (continued)

AGC Mode Control

The timing diagram in Figure 3 summarizes the sequence of states the AGC undergoes during a transition from one mode to another.

The AGC enters the LowZ mode when the chip is powered up, when the channels enters write mode (Bits 6 and 7 of the AGC1 register allows disabling of Low Z acuracy write mode) and upon entering and exiting servo mode (Bit 5 of register AGC1 allows the disabling of LowZ upon entering or exiting servo mode). The duration of the LowZ mode is determined by a resistor (RLZ), connected from the WRDEL pin to ground and is defined to be:

$$Tlz = RLZ \times 0.1\ \mu s/k\Omega$$

During LowZ mode, the AGC gain is squelched, without disturbing the voltage at the bypass capacitor, to reduce the effect of transients associated with the AGC mode transition.

The fast decay mode is triggered by the falling edge of the (internal) LowZ signal except when exiting write mode in which case the fast decay mode is skipped. The value of the fast decay current is controlled by the user through a resistor set between the AGCRST and BYP pins. Bit 4 of register AGC1 allows the user to disable the fast decay when exiting servo mode. The duration of the fast decay mode is dependent on the voltage at the DP,DN terminals: upon entering the fast decay mode, the AGC gain is rapidly increased until the voltage at DP,DN reaches 125% of the nominal value at which point the fast decay current is shut off. While in fast decay mode, the normal attack and decay currents are increased by a factor of 3 to speed the recovery back to 100%. The value of Tfd is defined by:

$$Tfd = RFD \times 0.1\ \mu s/k\Omega$$

where RFD is the value of an external resistor between the AGCDEL pin and ground.

The hold mode, triggered by the falling edge of the (internal) fast decay signal, is entered Tfd µs after the rising edge of SG. In this mode the AGC charge pump is disabled and the BYP voltage is held constant (except for leakage currents).

Qualifier Selection

The pulse qualifier transforms each valid analog read data pulse into a digital pulse, while preserving the relative time position of each valid pulse peak. Each pulse is validated by a combination of level qualification and time qualification. The SSI 32P4782A supports three forms of level qualification; in time qualification, the differentiated filter output is used to locate the signal peaks in time.

For read mode operation, the pulse qualification method is selected by setting bits D1...D0 in the PulseDetector1 control register to be one of the following:

Hysteresis Comparator Qualification: When the hysteresis qualification mode is selected, a comparator pair is used to perform level qualification while enforcing the following polarity check rule: the qualification of a peak of a given polarity must be followed by the qualification of a peak with opposite polarity.

Dual Comparator Qualification: When in Dual Comparator mode, independent positive and negative threshold comparators are used to suppress the error propagation characteristic of the hysteresis comparator mode.

Viterbi Qualifier: The Viterbi qualifier performs amplitude qualification using a floating threshold level architecture. The absolute threshold level is continuously calculated based upon the amplitude of the previous significant pulse. The previous significant pulse is defined to be either the opposite polarity pulse or the most recent same polarity pulse which exceeded the absolute threshold set earlier.

The floating threshold architecture offers two main advantages: it makes an excellent qualifier to use with asymmetrical signals because it does not assume that the qualification window must be centered around zero and it is able to adapt its qualification window around the mean of the peak to peak signal levels. As a second advantage, it allows consecutive same polarity peaks to be detected. Yet, it differs from the dual comparator qualification mode in that only the highest amplitude peak will find its way to the data separator.

The lower 7 bits of the PQ2 and PQ3 control registers are used to independently set the threshold levels of the positive and negative comparators used for amplitude qualification in read mode while the lower 7 bits of PQ5 and PQ6 controls the

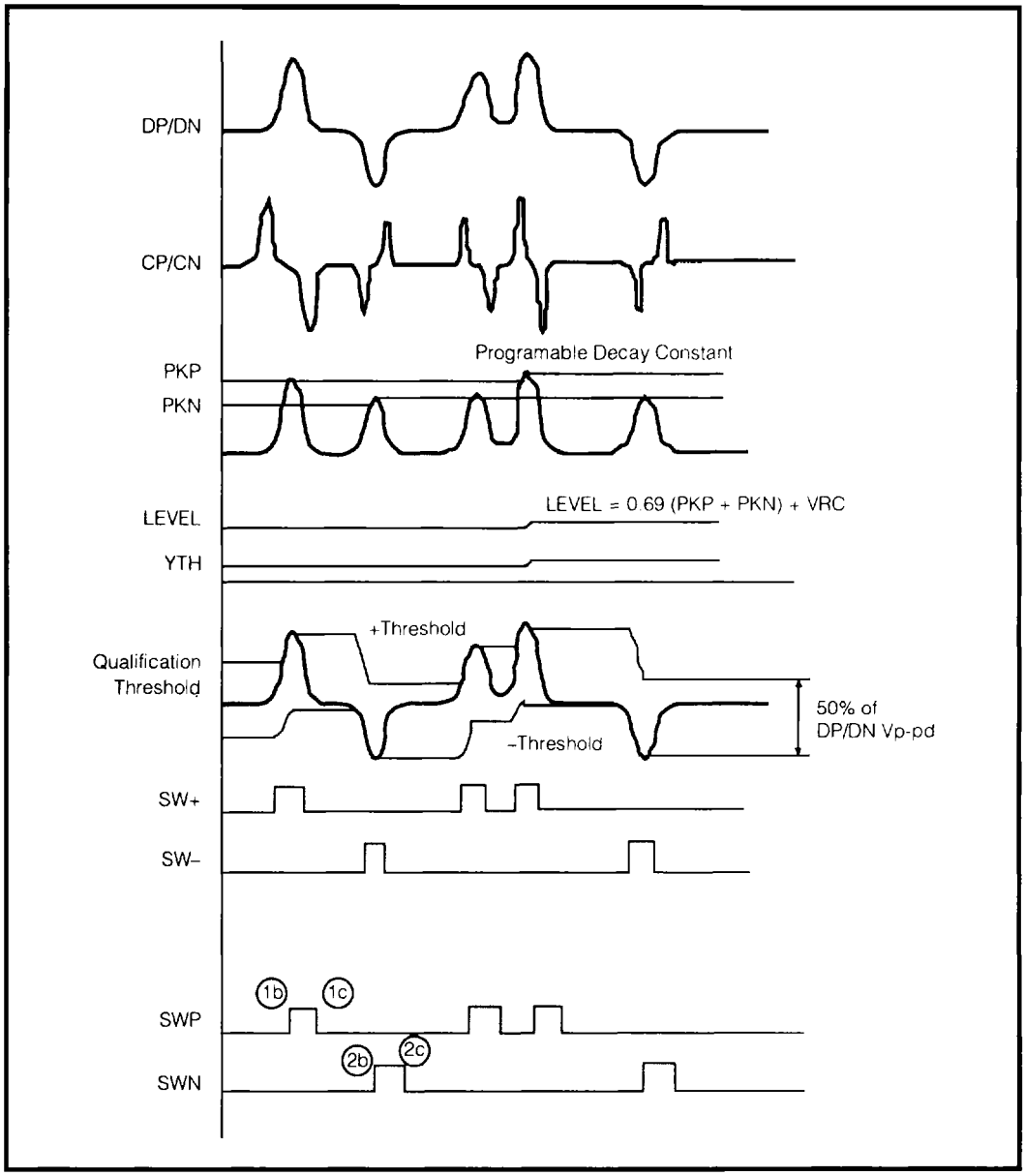

FIGURE 4: Viterbi Threshold Qualifier Timing

Qualifier Selection (continued)

threshold levels in servo mode (note: these registers do not affect the threshold of the Viterbi qualifier which, in effect, may be thought as the average of the threshold voltages VTHP and VTHN defined below, with PQ3 and PQ4 set to obtain 50% qualification threshold). As a design feature, a slight amount of hysteresis is introduced to improve the comparator response time when a signal that just exsceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator.

The positive and negative peaks (referenced to VRC) are captured and stored on internal hold capacitors (connected to PKP and PKN, respectively). Programmable pull down currents are provided on the PKP and PKN pins to set the decay time constants of these capacitor voltages. These pull down currents are controlled by a 4-bit DAC controlled by bits D5 ... D2 (DKDAC) of PQ1 control register, and are proportional to the data rate, bits D6 .... D0 of register DSI (IDAC), according to the following equation:

$$\frac{0.0039}{RR} \text{ IDAC } \frac{DKDAC}{80}$$

Note that during acquisition of servo mode preamble the decay current is reduced by a factor of 3 to:

$$\frac{0.0039}{RR} \text{ IDAC } \frac{DKDAC}{240}$$

and it is removed upon assertion of the internal HOLD signal. The voltages on PKP and PKN are buffered and brought out to the LEVELP and LEVELN pins where the user can further process them. The final thresholds, VTHP and VTHM, are established by multiplying DACs driven by the voltages at LEVELP and LEVELN, respectively, and may be adjusted from 10% to 80% with a resolution of 1%.

Mathematically, the above can be summarized as follows:

V@PKP = Positive Peak of (DP - DN) + VRC

V@PKN = Negative Peak of (DP - DN) + VRC

V@LEVELP = (V@PKP - VRC) + VRC =
Positive Peak of (DP - DN) + VRC

V@LEVELN = (V@PKM - VRC) + VRC =
Negative Peak of (DP - DN) + VRC

VTHP α • (V@LEVELP - VRC) •
DacCodeP/127 [Vpd] 32 < DacCode P < 127

VTHN α • (V@LEVELN - VRC) •
DacCodeN/127 [Vpd] 32 < DacCode N < 127

PQual% = -2.15 + 0.692 DacCodeP

NQual% = -2.15 + 0.692 DacCodeN

Viterbi Qual% = 50% • (LEVELP + LEVELN)

where :

VRC = Internal band gap based reference ~ VCC - 2.3 V

DacCodeP is set through bits D6.. D0 of PQ2 control register.

DacCodeN is set through bits D6...D0 of PQ3 control register.

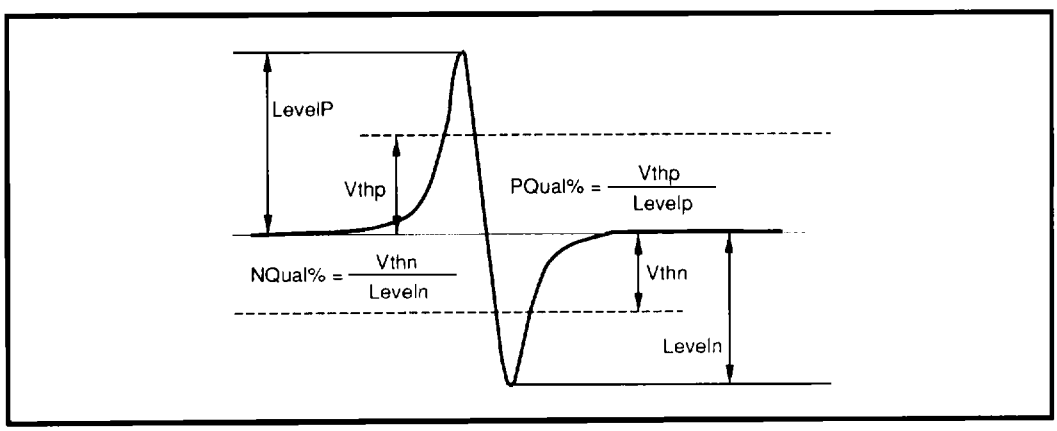

FIGURE 5: Qualification Percentage Definition

The threshold in servo mode is controlled by bits D6 ... D0 of PQ5 and PQ6 control registers as well as by the threshold selected in read mode as it is described by the following two expressions:

PQUAL % = -2.15 + 0.692 DacCode P (servo)

NQUAL % = -2.15 + 0.692 DacCode N (servo)

32 < DacCodeP (servo) < 127 (PQ5 Bits 6-0)

32 < DacCodeN (servo) < 127 (PQ6 Bits 6-0)

The Viterbi qualifier metric, VTH, may be thought as the average of the threshold voltages VTHP and VTHN previously defined. Because the AGC loop works off the full wave rectified DP,DN signal, it will force the DP,DN signal to 1.1 Vp-pd. With an asymmetrical read signal, the peak-to-peak differential signal at DP,DN will be less than 1.1 Vp-pd.

For servo mode operation the pulse qualifier is automatically set to operate in dual comparator mode.

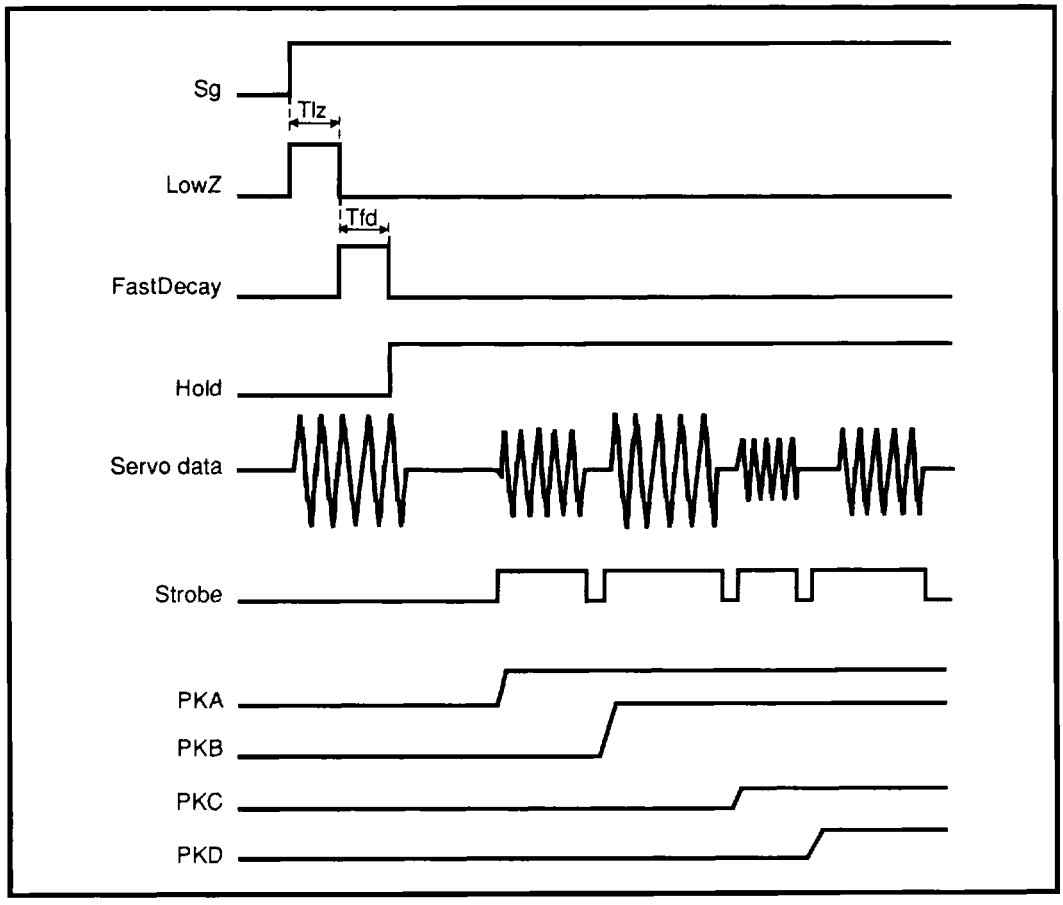

FIGURE 6: Servo Timing Diagram (sample)

FUNCTIONAL DESCRIPTION (continued)

SERVO DEMODULATOR CIRCUIT DESCRIPTION

The 32P4782A servo section captures four separate servo bursts and provides A,B,C,D burst outputs via open emitter outputs connected to pins PKA, PKB, PKC, and PKD. External capacitors are required to hold the burst outputs, and an external reset line is required to discharge the capacitors via external transistors (see Figure 1). To support embedded servo applications it provides additional programming registers that set the filter cutoff frequency, the qualifier threshold and the AGC level for servo mode. Servo mode is enterd when SG is set high, regardless of the state of RG and WG.

When SG is set high (servo mode), the reference voltage for the AGC charge pump is adjusted by a 4-bit DAC (DACA) controlled through the serial port register AGC1 bits 3-0. The DACA output voltage is offset so that 1111 results in a 0.88 Vp-pd output, and 0000 results in a 1.10 Vp-pd output:

$$VAGC = 1.10 - (DACA \times 0.01467)\ Vp\text{-}pd$$

where DACA is the decimal value of the DACA register. Also, the charge pump now drives the BYPS capacitor, which will be held constant (subject to leakage currents) as soon as SG is set low.

Servo Mode Operation

When the servo gate SG is set high, the DAC controlled current defining FC and VTH is switched from the read mode DAC to the servo mode DAC thus enabling fast switchover characteristics. In addition, the RDIO CMOS output is activated (provided that the MSB of register servo1 is set low), filter boost is disabled (provided that the MSB of register filter3 is set low), group delay equalization is disabled (provided that the MSB of register filter2 is set low). By disabling the boost and group delay equalization, as well as providing the servo control register for FC, the servo signal to noise ratio can be optimized by the user. During servo mode, the AGC circuit remains active through fast decay. Typically, a servo preamble is used to achieve the desired AGC level then the hold mode is entered to hold the AGC gain constant.

RDIO OUTPUT PIN

To support servo timing recovery, the pulse detector section provides a CMOS output of the servo information via the RDIO pin. A negative going transition is generated for each servo peak that is qualified through the pulse detector circuitry. This pin will be held high in idle and write modes, in read mode (unless Servo 1 bit 6 is set high), and in servo mode (unless Servo 1 bit 7 in set low) to reduce noise and accompanying jitter during read or write modes. There is no independent control of positive and negative threshold while in servo mode. Note that the nominal output pulse width is 30 ns.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

Ideal for constant density application, the SSI 32P4782A includes a programmable low pass filter with the following four key features:

- programmable cutoff frequency from 4 to 27 MHz,
- programmable boost from 0 to 12 dB at the cutoff frequency

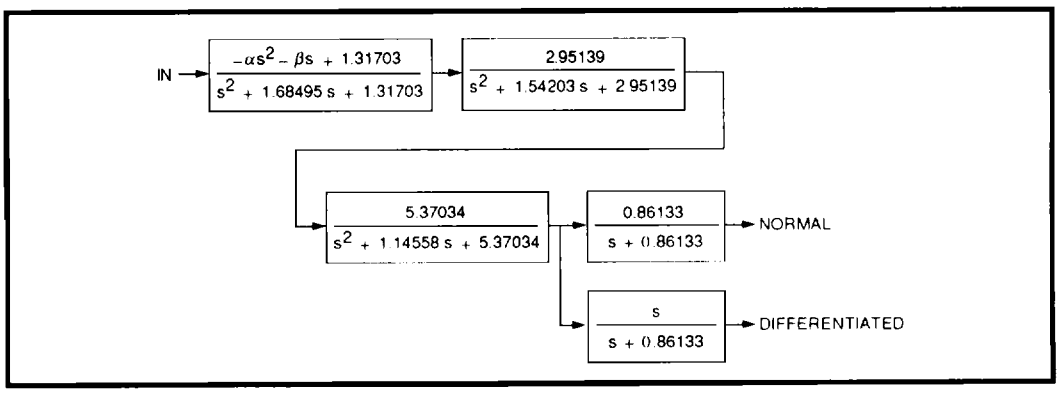

FIGURE 7: Filter Normalized Transfer Function

- programmable phase equalization
- normal low pass output and time-differentiated output

The normal low pass filter is a seven-pole two-real-zero type. Figure 4 illustrates the normalized transfer function. The cutoff frequency is scaled by replacing s with $s/2\pi Fc$, and the alpha boost & group delay equalization are controlled by varying the α and β parameters, repectively.

With a zero at the origin, the filter provides a time-differentiated filter output. The normal low pass output feeds the data qualifier (DP,DN), and the differentiated output feeds the clock comparator (CP,CN).

Five definitions are introduced for the programmable filter control discussion:

Cutoff Frequency: The cutoff frequency is the -3 dB low pass bandwidth with no alpha boost & group delay equalization, i.e., $\alpha = 0$ and $\beta = 0$.

Actual Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha \neq 0$ and/or $\beta \neq 0$.

Alpha Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha \neq 0$ and without group delay equalization ($\beta = 0$).

Group delay Δ%: The group delay Δ% is defined to be the percentage change in the value of absolute group delay measured at DC with group delay applied ($\beta \neq 0$), to that value of absolute group delay without group delay equalization being applied ($\beta = 0$).

Group delay Variation: The group delay variation is the change in group delay over a specified frequency interval. This can be expressed as a percentage defined as:

$$G.D.(\%) = 100 \frac{GDmax - GDmin}{GDmax + GDmin}$$

Direct coupled differential signals from the AGC amplifier output are applied to the filter. The programmable bandwidth and equalization characteristics of the filter are controlled by 5 internal DACs. The registers for these DACs (FCR, FCS, FBR, FBS, and FG) are programmed through the serial port. The current reference for the DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. This establishes the excellent temperature stability for the filter characteristics.

The boost and cutoff frequency can be set independently in the servo mode and the data mode. In the data mode, the cutoff frequency is controlled by the Filter 3 Register and the boost is controlled by the Filter 5 Register, and the boost is controlled by the Filter 6 Register. Furthermore, the Group Delay Equalization function can be enabled by setting the MSB bit in the Filter 3 Register, and boost is controlled by the Filter 5 Register.

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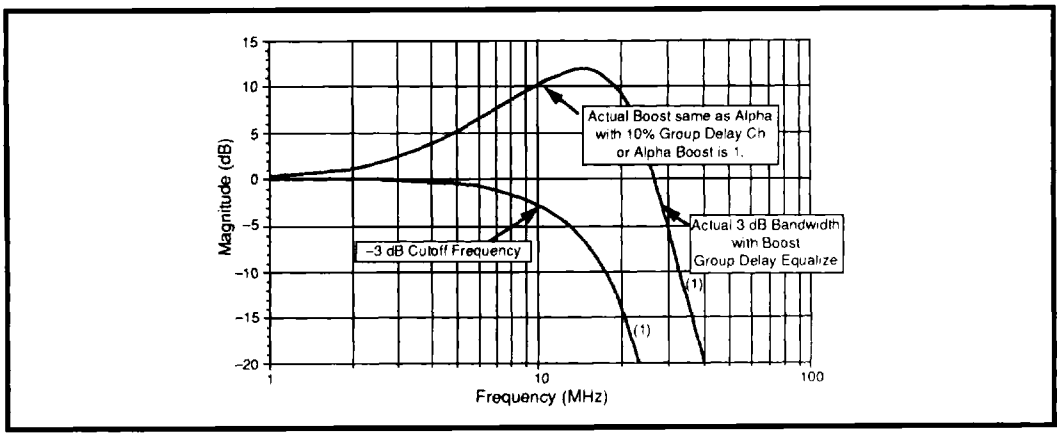

FIGURE 8: Filter Magnitude Response

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION (continued)

Filter Cutoff Control

The programmable filter cutoff frequency, fc, is set by the read mode cutoff register (FCD) while in read mode, and by the servo mode cutoff register (FCS) in servo mode. The DACs have 7-bit registers that program the DAC values to set the filter 3 dB cutoff frequency as follows:

fc (MHz) = 0.2141 x FCR - 0.5872
21 < FCR < 127
in read mode and

fc (MHz) = 0.2141 x FCS - 0.5872
21 < FCS < 127
in servo mode

The filter cutoff frequency will move out in frequency when boost is applied. The ratio of the actual -3 dB bandwidth to the programmed fc is tabulated in Table 1 as a function of applied boost and group delay equalization.

Filter Boost Control

The amount of boost is controlled by two parameters, alpha boost (α) and group delay equalization (β). The value of alpha boost is programmed from 0 to 12 dB by programming a linear 7-bit FBR DAC. The FBR for read mode and FBS register for servo mode register stores the 7-bit FB DAC control value. The alpha boost is set as follows:

Alpha boost (dB) = 20 log [1.00098 + 0.2496 • FBR/S + 0.00002 • FBR/S^2

0 < FBR/S < 127, 4 MHz < fc < 27 MHz

The programmed value of alpha boost is the expected magnitude of (Normal output) gain measured at the filter cutoff frequency when no group delay equalization is applied (β =0). When alpha boost values between 0 and 3 dB are programmed, the actual boost is higher than the programmed alpha boost. For alpha boost values greater than 3 dB, however, the difference becomes negligible.

Table 2 tabulates the actual boost as a function of the programmed alpha boost and group delay equalization.

Group delay equalization

The group delay Δ% can be programmed between -30% to +30% by the 8-bit linear FG DAC. The filter 2 register holds the 8-bit DAC control value. The group delay Δ% is set as:

Group delay D% = 0.2362 x (FG) x 100%
0 < FG < 127

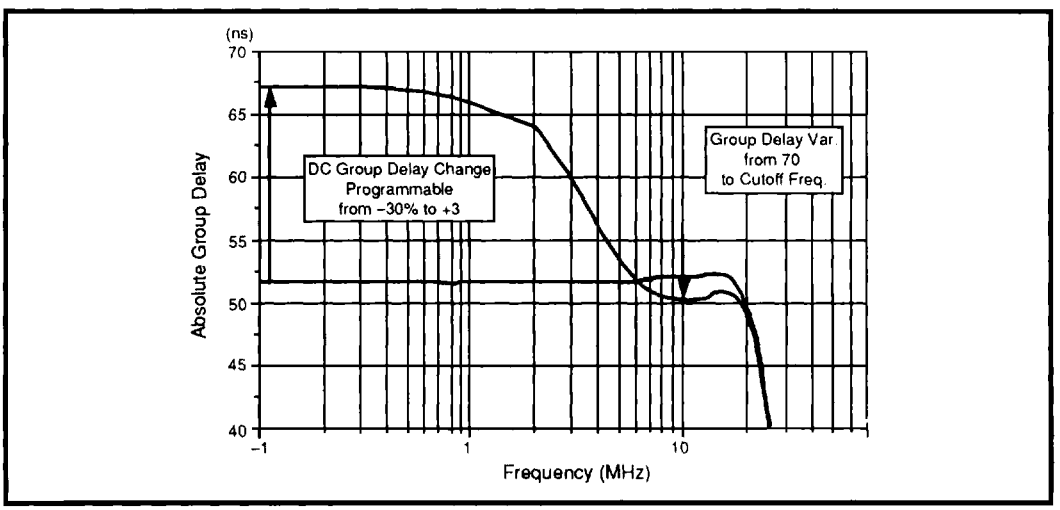

FIGURE 9: Filter Group delay Response

TABLE 1: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency

Alpha Boost	Group delay Δ%						
	±30%	±25%	±20%	±15%	±10%	±5%	0%
0 dB	1.58	1.45	1.30	1.17	1.07	1.02	1.00
1	1.67	1.57	1.47	1.36	1.27	1.21	1.19
2	1.78	1.71	1.64	1.56	1.50	1.46	1.44
3	1.90	1.85	1.80	1.76	1.72	1.70	1.69
4	2.01	1.98	1.96	1.93	1.91	1.90	1.90
5	2.13	2.11	2.09	2.08	2.07	2.06	2.06
6	2.23	2.22	2.21	2.20	2.20	2.20	2.20
7	2.33	2.32	2.32	2.31	2.31	2.31	2.31
8	2.42	2.41	2.41	2.41	2.41	2.40	2.40
9	2.50	2.50	2.50	2.49	2.49	2.49	2.49
10	2.58	2.58	2.58	2.57	2.58	2.57	2.57
11	2.66	2.65	2.65	2.65	2.65	2.65	2.65
12	2.73	2.73	2.73	2.73	2.73	2.73	2.73
13	2.80	2.80	2.80	2.80	2.80	2.80	2.80

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TABLE 2: Actual Boost vs. Alpha Boost & Group Delay Change

Alpha Boost	Group Delay Δ%						
	±30%	±25%	±20%	±15%	±10%	±5%	0%
0 dB	2.92	2.21	1.54	0.93	0.44	0.12	0.00
1	3.46	2.84	2.27	1.76	1.35	1.09	1.00
2	4.05	3.52	3.03	2.61	2.28	2.07	2.00
3	4.26	4.25	3.84	3.49	3.23	3.06	3.00
4	5.40	5.02	4.68	4.40	4.18	4.05	4.00
5	6.15	5.83	5.55	5.32	5.15	5.04	5.00
6	6.94	6.67	6.44	6.25	6.12	6.03	6.00
7	7.76	7.54	7.36	7.20	7.09	7.02	7.00
8	8.61	8.44	8.28	8.16	8.07	8.02	8.00
9	9.50	9.35	9.22	9.13	9.06	9.02	9.00
10	10.4	10.3	10.2	10.1	10.1	10.0	10.0
11	11.3	11.2	11.1	11.0	11.0	11.0	11.0
12	12.3	12.2	12.1	12.1	12.0	12.0	12.0
13	13.2	13.1	13.1	13.1	13.0	13.0	13.0

FUNCTIONAL DESCRIPTION (continued)

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the read mode, the data synchronizer performs sync field search and data synchronization. Data rates from 33 to 100 Mbit/s can be programmed using an internal DAC (DACI) whose reference current, set by a single external resistor RR, determines the VCO center frequency, the phase detector gain, and the 1/2 symbol delay. Data synchronization is performed by a fully integrated PLL with an advanced zero-phase restart technique that minimizes PLL acquisition time. The PLL is fully differential for maximum performance and noise rejection and includes inputs for three loop filter damping resistors. These resistors can be switched (using the serial port interface) to change the loop filter characteristics in a zoned recording application.

In the write mode, the circuit provides data encoding and independent late, early write precompensation for NRZ data applied to the NRZ0/1 pins. Data rate is established by the external reference frequency applied to FREF/$\overline{\text{FREF}}$ and the internal DACI.

Phase Locked Loop

The circuit employs a Dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a DRD pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise.

Mode Control

The read gate RG and write gate WG inputs control the Device Operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. It should be noted that RG should be held high until lock is achieved to data, then it may be brought low. If this condition is violated, RRC may disappear, and either RG or PWRON will have to be toggled to restart RRC. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

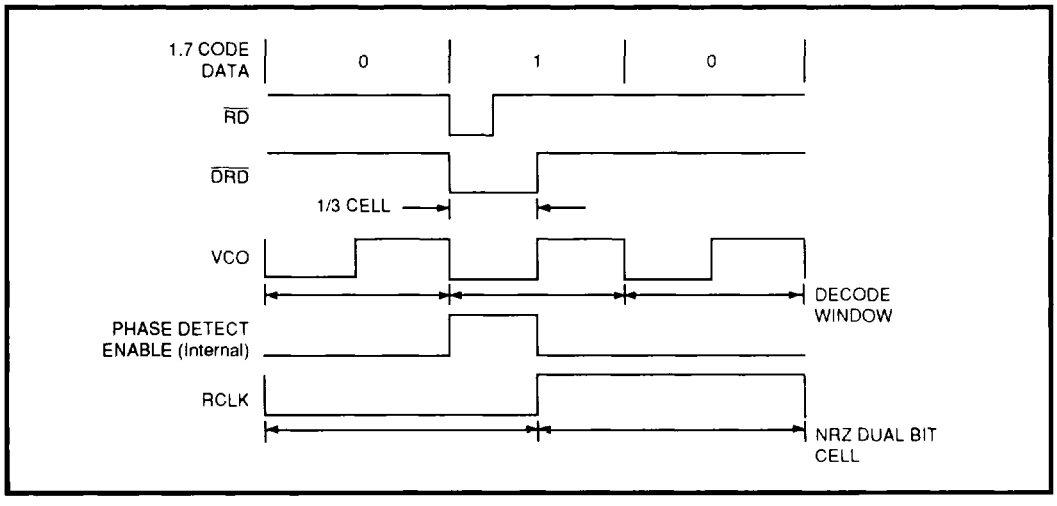

FIGURE 10

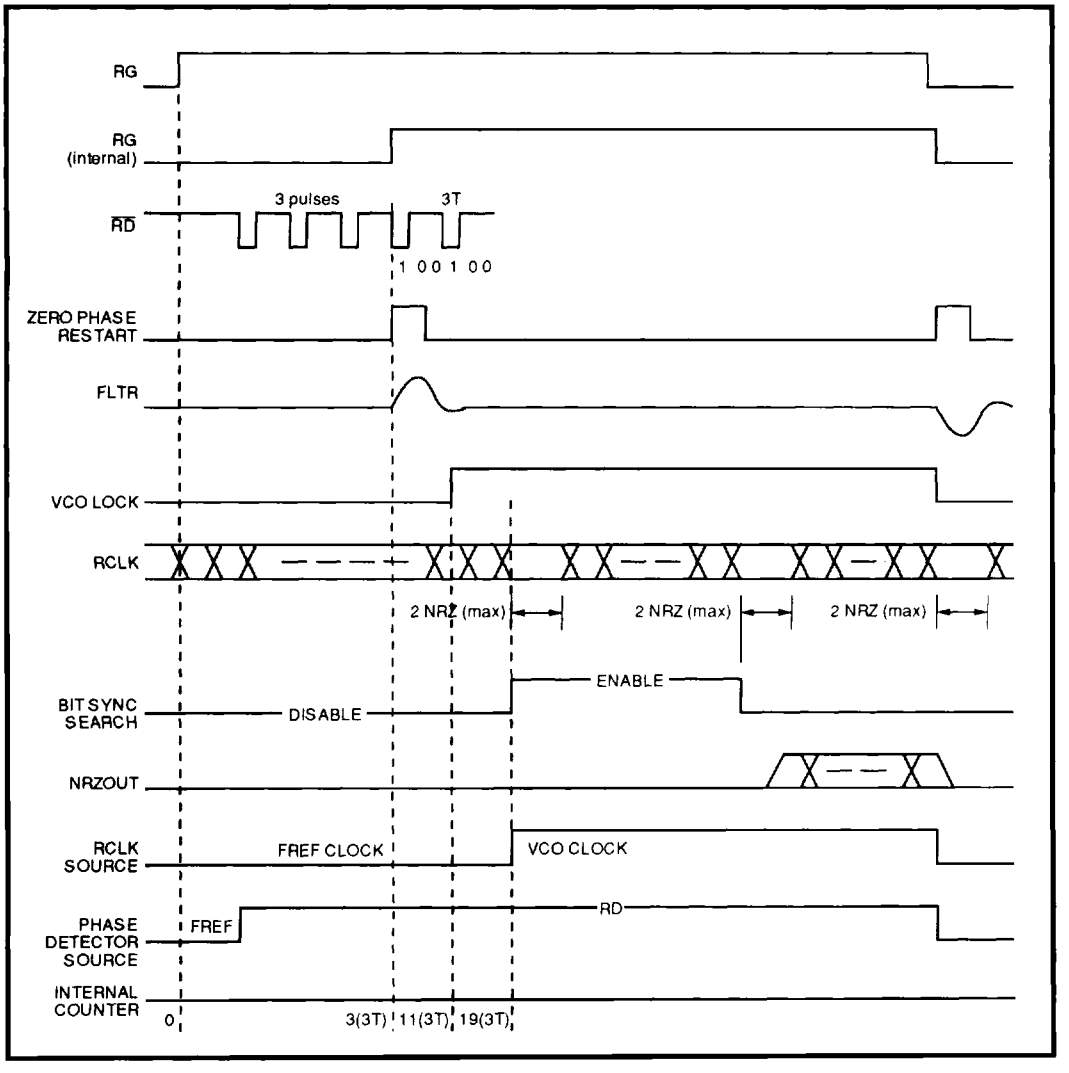

FIGURE 11: Read Mode Locking Sequence

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DATA SYNCHRONIZER CIRCUIT DESCRIPTION
(continued)

Read Mode

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate RG initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of DRD enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). DRD is a 1/2 symbol wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

Preamble Search

RG is asserted to initiate the preamble search. When RG is asserted, an internal counter is triggered to count positive transitions of the read data (RD). Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the FREF/$\overline{\text{FREF}}$ input to the delayed read data (DRD) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the DRD. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO Lock and Bit Sync Enable

Once ther internal RG is enabled the data synchronizer looks for 16 consecutive 3T patterns; the VCO lock signal is asserted after the first 8x3T while NRZ data will not appear until a total of 16x3T. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. The next 2 X 3T patterns are used to get the proper decode window so that the VCO is in sync with RCLK and RCLK is in sync with the data. Following this, the NRZ0/1 outputs are enabled and the data is toggled through the decoder for the duration of RG.

When the VCO lock signal is asserted, the internal RCLK source is also switched from the FREF/$\overline{\text{FREF}}$ input to the VCO clock signal that is phase locked to $\overline{\text{DRD}}$. During the internal RCLK switching period, the external RCLK signal may be held for a maximum of 2 NRZ clock periods, however no short duration glitches will occur.

Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS control bits of the window shift control register (DS3). The WS register bits are as follows:

BIT	NAME	FUNCTION
0	WS0	magnitude (SB)
1	WS1	magnitude
2	WS2	magnitude
3	WS3	magnitude (MSB)

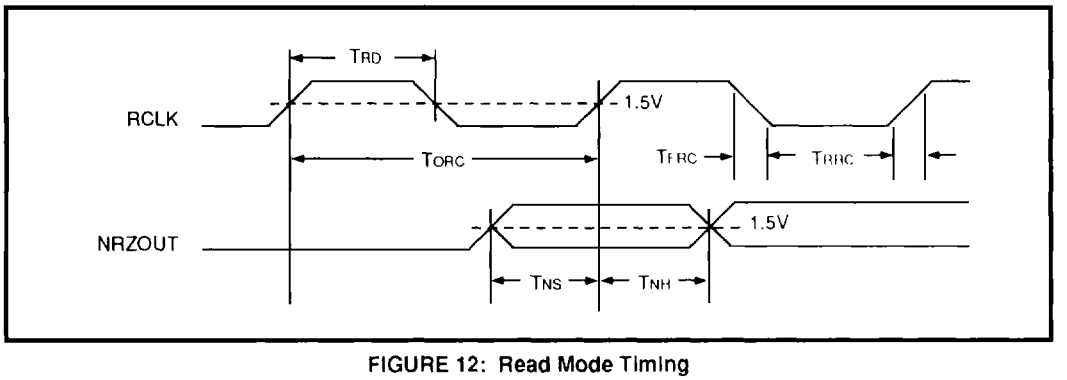

FIGURE 12: Read Mode Timing

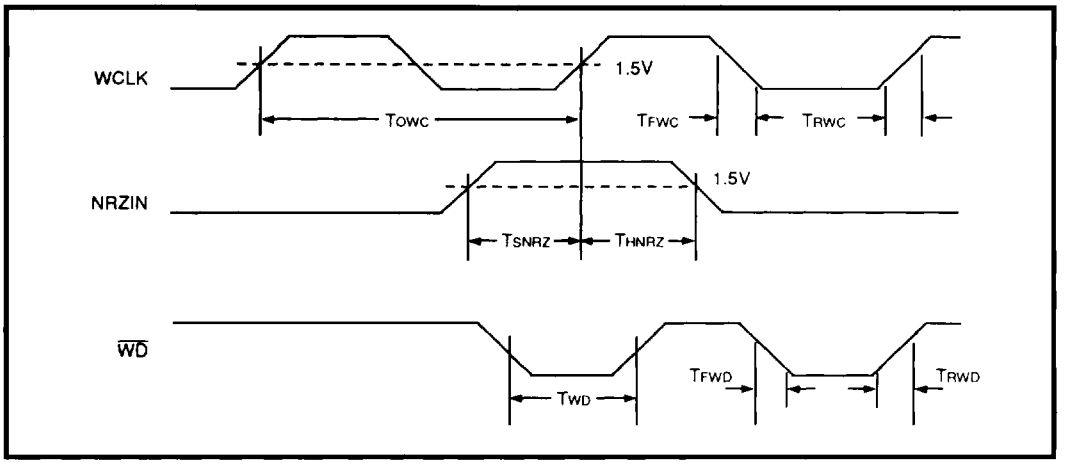

FIGURE 13: Timing Diagram

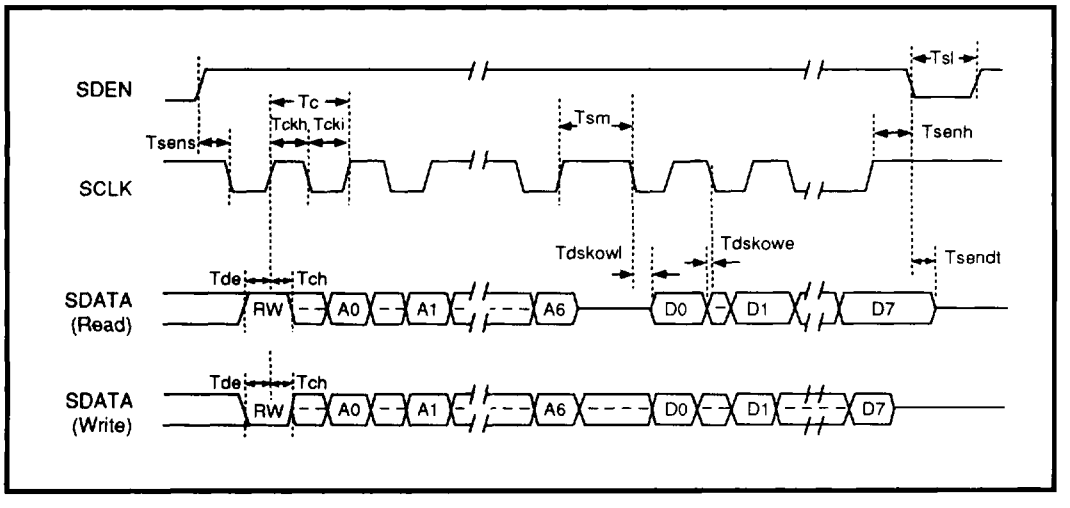

FIGURE 14: Serial Interface Timing

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DATA SYNCHRONIZER CIRCUIT DESCRIPTION (continued)

The window shift magnitude is set as a percentage of the decode window, in 5% steps. The window shift direction is set by bit 3 (WSD) in the WS register; a 1 sets positive shift, whereas 0 sets negative shift. Window shift should be set during idle mode or write mode.

WS3	WS2	WS1	WS0	Shift Magnitude
0	0	0	0	No shift
0	0	0	1	5% (minimum shift)
0	0	1	0	10%
0	0	1	1	15%
0	1	0	0	20%
0	1	0	1	25%
0	1	1	0	30%
0	1	1	1	35%
1	0	0	0	40%
1	0	0	1	45%
1	0	1	0	50% (maximum shift)

Non-Read Mode

In the non-read modes, the PLL is locked to the reference clock therefore forcing the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

Write Mode

Write mode is entered by asserting the write gate WG while the RG is held low. During write mode the VCO and the RRC are referenced to the internal time base generator signal.

When WG is asserted, the NRZ0/1 pins should be held low while the encoder generates the 3T preamble pattern. 3T patterns will be generated as long as the NRZ0/1 pins are both held low. While the preamble is being written the encoder is active. Therefore, WCLK must be toggling and NRZ0/1 must be held low ("0"). The first non-zero NRZ0/1 input bit indicates the end of the preamble pattern. After a delay of 5-6 WCLK time periods, non-preamble data begins to toggle out WD/$\overline{WD}$. At the end of the write cycle, 3 WCLK periods of blank NRZ data are required to insure the encoder is flushed of data before the WG can be transitioned low. WD/$\overline{WD}$ stop toggling a maximum of 1 WCLK time period after WG goes low.

Independent Early and Late Precomp Levels

The 32P4782A offers two independent levels of write precomp. Write precomp magnitude is set by the value in the Write Precomp register (DS2). The WP register bits are as follows:

BIT	NAME	FUNCTION
0	EW0	early magnitude (LSB)
1	EW1	early magnitude
2	EW2	early magnitude (MSB)
3	LW0	late magnitude (LSB)
4	LW1	late magnitude
5	LW2	late magnitude (MSB)

The EWn bits set the early magnitude, while the LWn set the late magnitude. The precomp magnitudes are calculated as follows:

$$TPC_{level\ 1} = EWn \times 0.05 \times T_{vco}$$

$$TPC_{level\ 2} = LWn \times 0.05 \times T_{vco}$$

where n = precomp magnitude scaling factor as shown below and T_{vco} is the preriod of VCO (which, of course, is assumed locked to the reference frequency FREF/$\overline{FREF}$).

W2	W1	W0	Scaling factor
0	0	0	No precomp
0	0	1	1X
0	1	0	2X
0	1	1	3X
1	0	1	4X
1	0	1	5X
1	1	0	6X
1	1	1	7X (maximum)

The following table defines the patterns decoded by the precomp logic:

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	compensation
0	0	1	0	0	None
1	0	1	0	1	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude. Late = Bit N is time shifted toward the N+1 bit by the programmed nagnitude.

For normal opeartion, bit 0 in the serial port register DS4 should be set to 0. This bypasses the precomp circuitry, and should result in better jitter performance. When this bit is set to 1, the precomp circuit is always active and will search for one of the listed conditions.

Direct Write Function

The 32P4782A includes a Direct write (DW) function that allows the NRZ1 data to bypass the write precomp circuitry. When the bit 7 is set in the DS3 register, the data applied to NRZ1 will bypass the write precomp circuitry and directly control the WD/$\overline{WD}$ output buffer. This allows the user to perform DC erase and media tests.

OPERATING MODES AND CONTROL

The 32P4782A has several operating modes that support read, write, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG), and PWRON pins. Additional modes are also controlled by programming the MSB of registers AGC1, PQ1 and DS1 via the serial port.

When PWRON is low, the device is in sleep mode.

External Mode Control

All operating modes of the device are controlled by driving the read gate (RG), write gate (WG), servo gate (SG), and PWRON pins with CMOS compatible signals. For normal operation the PWRON pin is set high. During normal operation the 32P4782A is controlled by the read gate (RG), write gate (WG), and servo gate (SG) pins.

When RG is high and WG is low the device is in read mode.

When WG is high and RG is low the device is in write mode.

If the RG is low and WG is low the device will be in idle mode.

Servo mode is entered by setting SG high regardless of the state of RG and WG.

Power Down Control

When the PWRON pin is brought low (0) the device is placed into sleep mode (<8 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the PWRON pin is driven high (1), the contents of the MSB of registers AGC1, PQ1, and DS1 determine which blocks will be active.

MULTIPLEXED TEST POINT SELECTION

The selection of the three multiplexed test points MTP1, MTP2, MTP3 is controlled by the two serial port bits PQ5_7 (MTPS0) and PQ6_7 (MTPS1) as shown in the following table.

MTPS0	MTPS1	MTP1	MTP2	MTP3
0	0	CPwin	CNwin	RRD2
1	0	VPwin	VNwin	QCK
0	1	VSWP	VSWN	SD2
1	1	SD2	DRD2	VCOR2

The function of these test points are outlined below:

CPwin Output of Classic Qualifier's positive pulse comparator.

CNwin Output of Classic Qualifier's negative pulse comparator.

RRD2 Read data pulse from Classic Qualifier.

VPwin Output of Viterbi Qualifier's positive pulse comparator.

VNwin Output of Viterbi Qualifier's negative pulse comparator.

QCK Qualifier clock.

VSWP Survivor register's synchronized positive pulse.

VSWN Survivor register's synchronized negative pulse.

SD2 Synchronized data as before.

DRD2 Window centering test points as before.

VCOR2 Window centering test points as before.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32P4782A. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits determine the internal register to be accessed. The second byte contains the programming data. In read mode (R/W = 1) the 32P4782A will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in the Electrical Specifications section.

REGISTER DESCRIPTION

SERIAL PORT REGISTER

In the following pages the legend '(normal operation)' identifies the preferred setting for the specified register bit. Performance degradation will result if this setting is not observed.

AGC GROUP

BIT	DESCRIPTION
Register AGC1	Address 0000011 = 0 x 03
7	1: WG-LowZ
6	0: WG-LowZ
	WGS-LowZ / WG-LowZ / Result 1 / 1 / no LowZ in write WG 0 / 1 / no LowZ in write WG 1 / 0 / LowZ same as WG 0 / 0 / LowZ during WG plus 1 µs after WG goes low.
5	Servo mode LowZ enable 1: No LowZ mode on rising or falling edge of SG fast decay is initated by the rising and falling edges of SG 0: LowZ entered upon rising and falling edge of SG. Fast decay is initiated by the falling edge of LowZ
4	Servo mode fast decay enable 1: Disables fast decay after falling edge of LowZ on exit from servo mode. 0: Enables fast decay after falling edge of LowZ on exit from servo mode (normal operation).
3...0	AGC Reference Voltage in servo mode 1111: 0.75 Vp-pd at DP/DN 0000: 1.10 Vp-pd at DP/DN

AGC (continued)

BIT	DESCRIPTION
Register AGC2	Address 0001011 = 0 x 0B
7	AGC/Filter enable 1: power down 0: power up (normal operation)
6	Filter bypass mode enable 1: enable (filter bypass) 0: disable (normal operation)
5	AGC offset trim enable 1: trim enabled 0: trim disabled (normal operation)
4	AGC offset trim polarity
3-0	AGC offset trim magnitude

FILTER GROUP

Register Filter 1	Address 0010011 = 0 x 13
7	Filter Fc trim enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
6	Fc DAC test enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
5	Boost DAC test enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
4	Group delay DAC test enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
3-0	Filter Fc trim magnitude (reserved to SSI)

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FILTER GROUP (continued)

Register Filter 2 Address 000111 = 0 x 1B

BIT	DESCRIPTION
Register Filter 2	Address 0011011 = 0 x 1B
7	Group delay equalization polarity 1: positive group delay 0: negative group delay
6-0	Group delay equalization magnitude
Register Filter 3	Address 0100011 = 0 x 23
7	Servo mode group delay equalization enable 1: enables group delay qualization in servo mode 0: disable group delay equalization in servo mode
6-0	Filter cutoff frequency (servo mode only)
Register Filter 4	Address 0101011 = 0 x 2B
7	Internal reference oscillator enable (reserved to SSI) 1: enables oscillator (wafer probe only) 0: disables oscillator (normal operation)
6-0	Filter cutoff frequency (read mode only)
Register Filter 5	Address 0110011 = 0 x 33
7	Reserved to SSI
6-0	Alpha boost magnitude (for read mode only)
Register Filter 6	Address 0111011 = 0 x 3B
7	Reserved to SSI
6-0	Alpha boost magnitude (for servo only)

SERIAL PORT REGISTER (continued)

PULSE QUALIFIER GROUP

BIT	DESCRIPTION
Register PQ1	Address 0000010 = 0 x 02
7	Qualifier/Servo enable 1: power down 0: power up (normal operation)
6	Qualifier mode (in servo) 0: polarity check 1: no polarity check
5-2	Qualifier internal decay current (bit 2 is the MSB, bit 5 is the LSB)
1-0	Qualifier mode (read mode) Bit 1 Bit 0 1 1 classic, polarity check 0 1 classic, no polarity check 1 0 viterbi, polarity check
Register PQ2	Address 0001010 = 0 x 0A
7	Negative data threshold test point enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
6-0	Negative threshold value (read mode only)
Register PQ3	Address 0010010 = 0 x 12
7	Positive data threshold test point enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
6-0	Positive threshold value (read mode only)
Register PQ4	Address 0011010 = 0 x 1A
7	Reserved to SSI
6-0	Adaptive threshold value
Register PQ5	Address 0100010 = 0 x 22
7	Test point selection MTP0
6-0	Negative threshold value (servo mode only)
Register PQ6	Address 0101010 = 0 x 2A
7	Test point selection MTP1
6-0	Positive threshold value (servo mode only)

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SERIAL PORT REGISTER (continued)

DATA SEPARATOR GROUP

BIT	DESCRIPTION
Register DS1	Address 0000100 = 0 x 04
7	Data separator enable 1: power down 0: power up (normal operation)
6-0	VCO center frequency control
Register DS2	Address 0001100 = 0 x 0C
7	Write flip flop control 1: bypass 0: enable
6	Charge pump common mode control 1: disabled (VCO DAC test point enabled) 0: enabled (VCO DAC test point disabled)
5-3	Late precomp magnitude
2-0	Early precomp magnitude
Register DS3	Address 0010100 = 0 x 14
7	Direct write enable 1: enabled 0: disabled (normal operation)
6	Filter switches selection, F1 1: on 0: off
5	Filter switches selection, F0 1: on 0: off
4	Window shift sign
3-0	Windo shift magnitude

DATA SEPARATOR GROUP

BIT	DESCRIPTION
Register DS4	Address 0011100 = 0 x 1C
7	Center frequency DAC trim enable (reserved to SSI) 1: enabled (wafer probe only) 0: disabled (normal operation)
6	Center frequency DAC trim polarity (reserved to SSI)
5-3	Center frequency DAC trim magnitude (reserved to SSI)
2	Phase detector windo centering test mode 1: test enabled 0: test disabled (normal operation)
1	Phase detector control 1: disabled (test mode) 0: enabled (normal operation)
0	Precomp automatic bypass control 1: disabled 0: enabled (normal operation)

SERVO GROUP

Register servo 1	Address 0000111 = 0 x 07
7	RDIO Servo mode enable 1: disables RDIO in servo mode 0: enables RDIO in servo mode (normal operation)
6	RDIO Read mode enable 1: enables RDIO output in read mode 0: disables RDIO in read mode (normal operation
5	Reserved to SSI (set to zero for normal operation)
4	Default 50 µA Iref for threshold in servo mode 1: enable 0: disable (normal operation)
3	Default 50 µA Iref for threshold in read mode 1: enable 0: disable (normal operation)
2-1	Reserved, set to Q for normal operation
0	Data synchronizer disabled by write gate 1: disable (data sync. always on) 0: enable (data sync. disable by WG)

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PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA1, VNA1	–	+5V analog SUPPLY and GND (AGC, filter)
VPA2, VNA2	–	+5V analog SUPPLY and GND (Servo, Qualifier)
VPA3, VNA3	–	+5V analog SUPPLY and GND (data Separator PLL)
VPA4, VNA4	–	+5V analog SUPPLY and GND (data Separator PLL)
VPD1, VND1	–	+5V digital SUPPLY and GND (data Separator PLL)
VPD2, VND2	–	+5V digital SUPPLY and GND (ENDEC, Serial Port)
VPDIO, VNDIO	–	+5V digital SUPPLY and GND (IO interface)
VNS	–	Substrate GND

INPUT PINS

VIAP, VIAN	I	AGC AMPLIFIER INPUTS.
WRDEL	I	AGC delay: A resistor RLZ connected from this pin to GND sets the LowZ time period.
PWRON	I	POWER ENABLE: A high level CMOS input enables power to the chip.
AGCDEL	I	AGC delay: A resistor connected from this pin to GND sets the fast decay time period (see AGC timing diagram on Figure 3).
RX	I	FILTER REFERENCE RESISTOR: The current reference for the filter DACs is set using a single external resistor connected from pin RX to ground. RX = 6.49 kΩ
BYP	I	AGC bypass capacitor.
AGCRST	I	Fast decay control: A resistor connected between this pin and the BYP pin sets the value of the fast decay current.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
RR	I	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to AGND to establish a precise internal reference current for the IDAC. The value of this external resistor should be 4.75K.The voltage at this pin should be both temperature and supply compensated and nominally is equal to 1.5V.
FREF, $\overline{\text{FREF}}$	I	REFERENCE FREQUENCY: Pseudo ECL. A differential reference frequency of 1.5x the data rate must be dc-coupled into these pins.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
WCLK	I	WRITE REFERENCE CLOCK: CMOS compatible. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to RCLK. For long cable delays, WCLK must be connected to an RCLK return line matched to the NRZ bus line delay.
RG	I	READ GATE: CMOS compatible read gate input. A high level CMOS input selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
SG	I	SERVO GATE: CMOS compatible servo gate input. A high level CMOS input activates the servo mode by selecting the servo control registers, the RDIO pin, the RTS resistor, and the BYPS capacitor.
STROBE	I	BURST STROBE: CMOS compatible burst strobe input. A high level will enable the servo peak detector to charge one of the burst capacitors, The falling edge of strobe increments an internal counter that determines which burst capacitor will charge on the next strobe pulse
WG	I	WRITE GATE: CMOS compatible write gate input. A low level CMOS input disables the write mode.
$\overline{\text{PWEN}}$	I	PHASE DETECTOR WINDOW TEST POINT: It must be held high during normal operation.

OUTPUT PINS

RCLK	O	READ REFERENCE CLOCK: PSEUDO TTL. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RCLK remains synchronized to FREF/3. When the SYNC bits are detected, RCLK is synchronized to the read data. When RG goes low, RCLK is synchronized back to FREF/3.
FON, $\overline{\text{FON}}$	O	FILTER NORMAL OUTPUTS: Filter normal outputs (AC coupled into the DP/ DN inputs).
FOD, $\overline{\text{FOD}}$	O	FILTER DIFFERENTIATED OUTPUTS: Filter differentiated outputs (AC coupled into the CP/CN inputs).
PKA,B,C,D	O	SERVO OUTPUTS: These outputs are raw outputs of the servo peak detectors. They are referenced to a baseline of 0.2V.
LEVELP, LEVELN	O	DATA QUALIFIER THRESHOLD MONITORS: An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACA).
VRC	O	THRESHOLD REFERENCE: An internally Vcc - 2.3V reference at this pin establishes the DC baseline for the LEVELP, LEVELN outputs.

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OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
MTP 1-3	O	MULTIPLEXED TEST POINT: Open emitter (pseudo ECL) test point. One external pulldown (562Ω) resistor is required to use this pin. It should be removed during normal operation to reduce power dissipation and jitter.
SD	O	SYNCHRONIZED DATA TEST POINT: Open emitter (pseudo ECL) test point. The positive edges of this signal represent the data out of the synchronizer. One external pulldown (562Ω) resistor is required to use this pin. It should be removed during normal operation to reduce power dissipation and jitter.
FOEN	O	FREQUENCY REFERENCE ENABLE: Pseudo TTL compatible. When this pin goes high the FREF, $\overline{\text{FREF}}$ clock is internally enabled. This pin goes low, internally disabling the FREF, $\overline{\text{FREF}}$ clock when RG is active, 19 3T patterns have been detected, and the VCO output is switched over as the source for RCLK. This signal can be used to disable the external timebase generator for improved jitter performance.
WD,$\overline{\text{WD}}$	O	WRITE DATA: Differential pseudo ECL. Output of the write data flip flop that is synchronized to the FREF, $\overline{\text{FREF}}$ reference clock. When a direct write is active, the outputs are directly controlled by the data on NRZ0. These pins will output differential synchronized data when RG = 1, bit 0 of DS 4 = 0, and bit 7 of DS 2 = 1.

SERIAL PORT PINS

SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level TTL input enables the serial port.
SDATA	I	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

PIN DESCRIPTION (continued)

BIDIRECTIONAL PINS

NAME	TYPE	DESCRIPTION
RDIO	I/O	READ DATA I/O: Bi-directional TTL pin. RDIO is an output when the SG is active or the RDIO bit is enabled in the pulse detector register. RDIO is an input when the RDIO bit is enabled in register servo 1. The SG and pulse detector functions override the bit in the servo 1.
FLT, $\overline{FLT}$	–	PLL LOOP FILTER: These pins are the connection points for the loop filter. FLT is the positive output of the phase detector, $\overline{FLT}$ is the negative output of the phase detector. The effective VCO voltage is FLT - $\overline{FLT}$.
FLT0, FLT1	–	PLL LOOP FILTER RESISTORS: Loop filter damping resistors are connected to these pins to establish the loop characteristics. Internal FETs can be enabled to connect the resistors to the $\overline{FLT}$ side of the VCO. The serial port register DS3 (bits D6...D4) is used to control the resistor selection.
NRZ0, NRZ1	I/O	NRZ DATA PORT: Bi-directional pin. (CMOS IN, PSEUD TTL OUT) read data output when RG is high, write data inputs when WG is high. (NRZ1 is the MSB).

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
Storage temperature	-65 to 150°C
Junction operating temperature	+130°C
Positive supply voltage (Vp)	-0.5 to 7V
Voltage applied to logic inputs	-0.5V to Vp+0.5V
All other pins	-0.5V to Vp+0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ICC	Outputs and test point pins open Ta = 27°C Vcc = 5V, 80 Mbit/s		100	155	mA
PWR Power dissipation	Outputs and test point pins open, Ta = 27°C Vcc = 5V, 80 Mbit/s		550	850	mW
Sleep mode current	PWRON = 0			1.5	mA
Stand by current	PWRON = 1 All functions disabled			20	mA

DIGITAL INPUTS AND OUTPUTS

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD + 0.3	V
Input low current	IIL	VIL = 0.4V			-0.4	mA
Input high current	IIH	VIH = 2.4V			100	µA

TTL COMPATIBLE OUTPUTS

Output low voltage	VOL	IOL = 4 mA			0.5	V
Output high voltage	VOH	IOH = -400 µA	2.4			V

DIGITAL INPUTS AND OUTPUTS (continued)

PSEUDO TTL OUTPUTS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Output low voltage	VOL	IOL = 0.0 mA			0.3	V
Output high voltage	VOH	IOH = 0.0 mA	2.2			V

CMOS COMPATIBLE INPUTS

Input low voltage	5V, 25°C			0.5	V
Input high voltage	5V, 25°C	4.5			V
Rise time	4.3V, 70°C, C = 1.5 pF			5	ns
Fall time	4.3V, 70°C, C = 1.5 pF			4.5	ns

CMOS COMPATIBLE OUTPUTS

Output low voltage	5V, 25°C IOL = 4.07 mA			0.5	V
Output high voltage	5V, 25°C IOH = -4.83 mA	4.5			V
Rise time	4.3V, 70°C, C = 16 pF			5.5	ns
Fall time	4.3V, 70°C, C = 16 pF			5	ns

PSEUDO ECL OUTPUT LEVELS

DRD, SD, VCOREF. For all tests, 261Ω to VPA and 402Ω to GND with VCC = 5V.

Output high level	Vcc = 5V		VCC - 1.2		V
Output swing		300			mVp

SERIAL PORT

SCLK period			100			ns
SCLK low time	TCKL		40			ns
SCLK high time	TCKH		40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		35			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

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PULSE DETECTOR CHARACTERISTICS

AGC AMPLIFIER

Input signals are AC coupled to VIAP/AIN, and FNP/FNN are AC coupled to DP/DN. 1000 pF capacitor is connected from BYPD to VPG (CBYP). Unless otherwise specified, outputs are measured differentially at DP/DN, FIN = 22 MHz, and filter boost = 0 dB.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input range	Filter boost = 0 dB	20		250	mVp-pd
	Filter boost = 12 dB	20		250	mVp-pd
DP-DN voltage	VIAP - VIAN = 0.1 Vp-pd Fin = 8 MHz Vcc = 5V	0.93	1.10	1.27	Vp-pd
	SG = high, AGC DAC = 0	0.93	1.10	1.27	Vp-pd
	SG = high, AGC DAC = 15	0.74	0.88	1.02	Vp-pd
DP-DN voltage variation	20 mVp-pd < VIAP - VIAN < 250 mVp-pd Fin = 8 MHz, Vcc = 5.0			5	%
	20 mVp-pd < VIAP - VIAN < 250 mVp-pd Fin = 10 MHz, Vcc = 5.0			5	%
	20 mVp-pd < VIAP - VIAN < 250 mVp-pd Fin = 30 MHz, Vcc = 5.0			10	%
Gain range	Including filter gain	0.45		50	V/V
Gain sensitivity	BYP voltage change	20	25	30	dB/V
Differential input impedance	WG = low	1.5	2.5	3.5	kΩ
	WG = high	300	500	700	Ω
Single-ended input impedance	WG = high	0.75	1.25	1.75	kΩ
	WG = high	150	250	350	Ω
Output offset voltage		-100		100	mV
Input noise voltage	Max gain		14	20	nV/√Hz
Bandwidth		100	140		MHz
CMRR	Gain = 22, fc = 33 MHz	40			dB
PSRR	Gain = 22, fc = 33 MHz	45			dB
Gain decay time	VIAP - VIAN = 200 to 100 mVp-pd VDP - VDN < 0.9 Final Value (reference only)		50		µs
Gain attack time	VIAP - VIAN = 100 to 200 mVp-pd VDP - VDN < .10 Final Value (reference only)		1		µs

PULSE DETECTOR CHARACTERISTICS (continued)

AGC CONTROL

The input signals are AC coupled from the filter normal output into DN,DP, CBYPD = 1000 pF to VCC, SG = low unless otherwise specified.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
DP-DN input range		For reference only			1.5	Vp-p
Decay current Normal decay	ID		-3	-4.2	-7	µA
Fast decay mode	IDF	For reference only		3 x ID		µA
Attack current						
Normal attack	ICH		0.12	0.18	0.29	mA
Fast/normal attack Mode ratio	ICHF		7	8.5	11	mA/mA
BYPD leakage current		WG = high	-10		10	nA
Fast decay duration		For reference only		1		µs
LowZ duration		After Pwron		1.2	1.5	µs
		After servo or write		1	1.2	µs
WRDEL voltage		Rlz = 10 kΩ	0.3	0.4	0.5	V
AGCDEL voltage		Rfd = 10 kΩ	0.3	0.4	0.5	V
LEVEL output gain		DP-DN = 0.25 to 0.75 VDC	0.4	0.45	0.5	V/Vp-p
LEVEL offset voltage		Output - VRC, IL = 50 µA	-150		150	mV
VRC voltage		Vcc - VRC -1 mA < Ivrc < 0 mA	2.1	2.3	2.5	V

DATA COMPARATOR

The input signals are AC coupled into DP,DN.

DP-DN input range	For reference only			1.5	Vp-pd
Differential input resistance		3	4	5	kΩ
Differential input resistance	WG = high	750	1000	1400	Ω
Differential input capacitance				5	pF
Positive threshold accuracy (DR = 32 - 100 Mbit/s)	Qual% = -2.15 + 0.692 DacCode 32 < DacCode < 127 VIAP, VIAN = 0.1 Vp-pd, SG = 0 3T test pattern, Vcc = 5V	-20		20	%
Negative qual threshold (DR = 32 - 100 Mbit/s)	Qual% = -2.15 + 0.692 DacCode 32 < DacCode < 127 VIAP, VIAN = 0.1Vp-pd, SG = 0 3T test pattern, Vcc = 5V	-20		20	%

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CLOCK SECTION

The input signals are AC coupled into CP/CN.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
CP-CN input range	For reference only			1.5	Vp-p
Comparator offset voltage	For reference only	-4.0		4	mV
Differential input resistance		3	4	5	kΩ
Differential input capacitance				5	pF
Pulse pairing DR = 32 -100 Mbit/s	VIAP, VIAN = = 1 Vp-pd, SG = 0 3T test pattern			0.25	ns

SERVO CAPTURE CHARACTERISTICS

A, B, C, D output Low voltage offset	CP-CN = 0 Strobe = Hi ATE			0.1 0.2	V V
A, B, C, D output Clip level	CP-CN = 1.5 Vp-pd, F = 8 MHz	1.7		2.3	V
A, B, C, D gain	CP-CN = 1.0 Vp-pd, F = 8 MHz	1.45	1.6	1.75	V/Vp-pd
Channel to channel amplitude mismatch	CP-CN = 1Vp-pd Sinewave at 8 MHz	-10		10	mV
RDIO fall time	CL = 15 pF Cl = 40 pF (ATE)			5 8	ns ns
RDIO rise time	CL = 15 pF CL = 40 pF (ATE)			5 8	ns ns
RDIO pulsewidth	CL = 15 pF CL = 40 pF (ATE)	20 20	30 30	40 40	ns ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range	*fc* @ -3 dB point -read mode -servo mode	9 4		27 9	MHz MHz
Filter cutoff accuracy	DACF = 127	-15		15	%
FNP, FNN differential gain AN	F = 0.67 x *fc*, boost = 0 dB		1		V/V
FDP, FDN differential gain AD	F = 0.67 x *fc*, boost = 0 dB	0.8 AN		1.2 AN	V/V
Frequency boost accuracy	@ 6 dB, DACS = 37	-1		+1	dB
	@ 9 dB, DACS = 67	-1.25		1.25	dB
	@ 13 dB, DACS = 127	-1.5		1.5	dB

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
group delay equalization Accuracy	*fc* = 4 - 27 MHz Boost = 0 dB	-5		5	%
group delay variation	F = 0.2 *fc* to 1 *fc* *fc* = 4 - 27 MHz Boost = 0 dB	-2		2	%
group delay variation	F = *fc* to 1.75 *fc* Boost = dB				
	fc = 27 MHz	-2		2	%
	18 < *fc* < 27 MHz	-3		3	%
	9 < *fc* < 18 MHz	-6		6	%
	fc < 9 MHz	-7		7	%
Filter total harmonic Distortion (Norm Out)	*fc* = 27 MHz, Boost = 0 dB VVIAP, VIAN = 20 mVp-pd, 18 MHz			1	%
	fc = 27 MHz, Boost = Max VVIAP, VIAN = 20 mVp-pd, 18 MHz			1	%
Filter total harmonic Distortion (Diff Out)	*fc* = 27 MHz, Boost = Max VVIAP, VIAN = 20 mVp-pd, 18 MHz			1.5	%
	fc = 27 MHz, Boost = Max VVIAP, VIAN = 20 mVp-pd, 18 MHz			2	%
Filter total harmonic Distortion (Norm Out)	*fc* = 27 MHz, Boost = 0 dB VVIAP, VIAN = 200 mVp-pd, 18 MHz			1	%
	fc = 27 MHz, Boost = Max VVIAP, VIAN = 200 mVp-pd, 18 MHz			1	%
Filter total harmonic Distortion (Diff Out)	*fc* = 27 MHz, Boost = 0 dB VVIAP, VIAN = 200 mVp-pd, 18 MHz			1.5	%
	fc = 27 MHz, Boost = Max VVIAP, VIAN = 200 mVp-pd, 18 MHz			2	%
Filter total harmonic Distortion (Norm Out)	*fc* = 27 MHz, Boost = 0 dB VVIAP, VIAN = 250 mVp-pd, 18 MHz			1	%
	fc = 27 MHz, Boost = Max VVIAP, VIAN = 250 mVp-pd, 18 MHz			1	%
Filter total harmonic Distortion (Diff Out)	*fc* = 27 MHz, Boost = 0 dB VVIAP, VIAN = 250 mVp-pd, 18 MHz			1.5	%
	fc = 27 MHz, Boost = Max VVIAP, VIAN = 250 mVp-pd, 18 MHz			2.6	%

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PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Filter total harmonic Distortion (Norm Out)	fc = 9 MHz, Boost = 0 dB VVIAP, VIAN = 20 mVp-pd, 6 MHz			1	%
	fc = 9 MHz, Boost = Max VVIAP, VIAN = 20 mVp-pd, 6 MHz			1	%
Filter total harmonic Distortion (Diff Out)	fc = 9 MHz, Boost = 0 dB VVIAP, VIAN = 20 mVp-pd, 6 MHz			1	%
	fc = 9 MHz, Boost = Max VVIAP, VIAN = 20 mVp-pd, 6 MHz			1.5	%
Filter total harmonic Distortion (Norm Out)	fc = 9 MHz, Boost = 0 dB VVIAP, VIAN = 200 mVp-pd, 6 MHz			1	%
	fc = 9 MHz, Boost = Max VVIAP, VIAN = 200 mVp-pd, 6 MHz			1	%
Filter total harmonic Distortion (Diff Out)	fc = 9 MHz, Boost = 0 dB VVIAP, VIAN = 200 mVp-pd, 6 MHz			1	%
	fc = 9 MHz, Boost = Max VVIAP, VIAN = 200 mVp-pd, 6 MHz			2.6	%
Filter total harmonic Distortion (Norm Out)	fc = 9 MHz, Boost = 0 dB VVIAP, VIAN = 250 mVp-pd, 6 MHz			1	%
	fc = 9 MHz, Boost = Max VVIAP, VIAN = 250 mVp-pd, 6 MHz			1.5	%
Filter total harmonic Distortion (Diff Out)	fc = 9 MHz, Boost = 0 dB VVIAP, VIAN = 250 mVp-pd, 6 MHz			1.5	%
	fc = 9 MHz, Boost = Max VVIAP, VIAN = 250 mVp-pd, 6 MHz			2.5	%
Output noise voltage differentiated output	(AGC included, Gain = 22V/V fc = 27 MHz, boost = 0 dB		5	8	mV rms
	fc = 27 MHz, boost = 13 dB		16.5	20	mV rms
normal output	fc = 27 MHz, boost = 0 dB		3.5	5	mV rms
	fc = 27 MHz, boost = 13 dB		7.5	12.5	mV rms
Filter output sink current		1.5	2		mA
Filter output offset voltage	fc = 9 MHz -127 MHz	-150		150	mV
Filter output source current		2			mA
Filter output resistance	Single ended			100	Ω
RX pin voltage	Ta = 27°C		600		mV
	Ta = 127°C		800		mV
RX resistance	1% fixed value		6.49		kΩ

DATA SEPARATOR CHARACTERISTICS

READ MODE

TVCO = 1.64 + (0.163 • RR/DACI),RR = 4.75 kΩ

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
RR range		1% fixed value		4.75		kΩ
Read clock rise time	TRRC	0.8 to 2V, CL < 15 pF CL = 40 pF (ATE)			5 8	ns
Read clock fall time	TFRC	2 to 0.8V, CL = 15 pF CL = 40 pF (ATE)			5 8	ns
RCLK high time	THRC	2V, CL < 15 pF	10			ns
RCLK low time	TLRC	0.8V, CL < 15 pF	10			ns
RCLK re-sync time			TORC		2 TORC	ns
NRZ out set-up and hold time	TNS, TNH		8			ns
1/2 symbol delay		TD = 0.5 • TVCO For reference only	0.9 TD		1.1 TD	ns

WRITE MODE

Write data rise time	TRWD	20 to 80% 110Ω to VCC, 160Ω to AGND			3	ns
Write data fall time	TFWD	80 to 20% 110Ω to VCC, 160Ω to AGND			3	ns
Write data clock rise time	TRWC	0.8 to 2V, CL < 15 pF			10	ns
Write data clock fall time	TFWC	2 to 0.8 V, CL < 15 pF			6	ns
NRZ set-up time	TSNRZ		5			ns
NRZ hold time	THNRZ		4			ns

DATA SYNCHRONIZATION

Unless otherwise specified, RR = 4.75k, FP = FM = 2.5V, 20 ≤ DACI ≤ 80

VCO center frequency period accuracy	TVCO		-15		15	%
VCO control gain rad/(V-S)	KVCO	ωi = 2πTVCO -2V < FP-FM < +2V DACI = 80	0.08 ωi		0.16 ωi	rad/(sV)
		DACI < = 65	0.12 ωi		0.18 ωi	rad/(sV)

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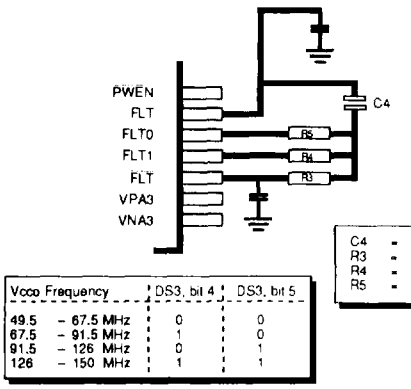
DATA SYNCHRONIZATION (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCO dynamic range	0V < FP - FM < 2V DACI = 80	10		25	%
	DACI = 65	18		30	%
	DACI ≤ 65	23		37	%
	-2V < FP - FM < 0V DACI ≤ 80	-23		-37	%
Phase det gain KD	DACI ≤ 80 Read (3T pattern):				
	KD = 0.0001308 • DACI/(6π RR) Idle: (with 3T preamble)	0.83		1.17	KD
	KD = 0.0001308 • DACI/(4π RR)	0.83		1.17	KD
KVCO x KD product accuracy		-26		26	%
VCO phase restart error ATE measurement accuracy	DR ≤ 100 Mbit/s	-0.1 -1		+0.1 +1	TVCO ns
Decode window loss ATE measurement accuracy	DR ≤ 100 Mbit/s	 -1.0		0.03 +1	TVCO ns
Decode window center	DR = 90 Mbit/s DR = 80 Mbit/s DR ≤ 60 Mbit/s	-0.09 -0.09 -0.03		+0.02 +0.02 +0.03	TVCO TVCO TVCO
Window shift error	DR ≤ 100 Mbit/s				
	WSDacCode = 1	-50		+50	%
	WSDacCode = 2	-25		+25	%
	WSDacCode > 2	-20		+20	%
Phase det window center	DR ≤ 100 Mbit/s	-0.1		+0.1	TVCO
ATE measurement accuracy		-1.0		+1	ns
On resistance from FM to Fn (RSON)	FS_N = 1 n = 0, 1			20	Ω
Off resistance from FN to Fn (RSOFF)	FS_N = 0 n = 0, 1	10M			Ω

DATA SEPARATOR CHARACTERISTICS (continued)



Unless otherwise specified:

RR = 4.75 kΩ,
20 ≤ DACI ≤80.

and the PLL filter components are as specified in the figure 18.

The Vco period, TVCO, is defined by the following equation:

TVCO = 1000/(6.974 +8.732 DACI / RR) [ns]

FIGURE 18: PLL Filter Components

All equations containing RR assumed to be expressed in kΩ.

APPLICATIONS INFORMATION

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME
0	WSO
1	WS1
2	WS2
3	WSD

The window shift magnitude is set as a percentage of the decode window, in 5% steps. The tolerance of the window shift magnitude is ±15%. Window shift should be set during idle mode or write mode.

WS2	WS1	WS0	SHIFT MAGNITUDE
0	0	0	No shift
0	0	1	5% (minimum shift)
0	1	0	10%
0	1	1	15%
1	0	0	20%
1	0	1	25%
1	1	0	30%
1	1	1	35% (maximum shift)

The window shift direction is set by bit 3 (WSD) in the WS register. A 1 sets a positive shift, a 0 sets a negative shift. For normal operation, the BYP bit in the serial port should be set to 0. This allows the window shift circuit to detect the No shift condition and bypass the window shift circuit. This will tend to minimize window loss and shift in the normal operating mode. When BYP is set to 1, the window shift circuit does not detect the no shift condition and uses the window shift circuitry. This is useful when testing the device. Note that no window shift function is available while operating the qualifier in viterbi mode.

WRITE PRECOMP CONTROL (proposed)

Write precomp magnitude is set by the value in the write precomp register DS2. The WP register bits are as follows:

BIT	NAME
0	EWO
1	EW1
2	EW2
3	LW0
4	LW1
5	LW2

The MWn bits set the level 1 Late magnitude while the LWn set the level 2 late magnitude. The precomp magnitude are calculated as follows:

TPC_{Early} = EWn x 0.05 x TREF

TPC_{Late} = LWn x 0.05 x TREF

where n = precomp magnitude scaling factor as shown below and TREF is the period of the reference frequency of the input signal provided at FREF/$\overline{FREF}$.

W2	W1	W0	PRECOMP MAGNITUDE SCALING FACTOR
0	0	0	No precomp
0	0	1	1X
0	1	0	2X
0	1	1	3X
1	0	0	4X
1	0	1	5X
1	1	0	6X
1	1	1	7X (maximum)

WRITE PRECOMP CONTROL (continued)

The following table defines the patterns decode by the precomp logic:

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	COMPENSATION
0	0	1	0	0	None
1	0	1	0	1	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Level 1 Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude.
Level 2 Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude

For normal operation, the bit 0 in the serial port register DS4 should be set to 0. This allows the precomp circuit to detect the no precomp condition (for both level 1 late and level 2 late) and bypass the precomp circuitry. When BYP is set to 1, the precomp circuit does not detect the No Precomp condition and forces the signal through the precomp circuitry. This is useful when testing the device.

TABLE 4: 1,7 RLL Encode

NRZ DATA				ENCODED WRITE DATA	
PRESENT BITS		NEXT BITS		CODE BITS	
0	0	0		1	0 0 1
0	0	1		0	0 0 0
0	0	1		1	0 1 0
1	0	0			1 0 1
1	0	1			0 1 0
0	1	0	0	0	0 0 1
0	1	0	0	1	0 1 0
0	1	1	0		0 0 0
0	1	0	1	0	0 0 1
0	1	0	1	1	0 0 0
0	1	1	1		0 0 0
1	1	0	0	0	0 1 0
1	1	1	0	0	1 0 0
1	1	0	1	0	1 0 0
1	1	1	1	0	1 0 0

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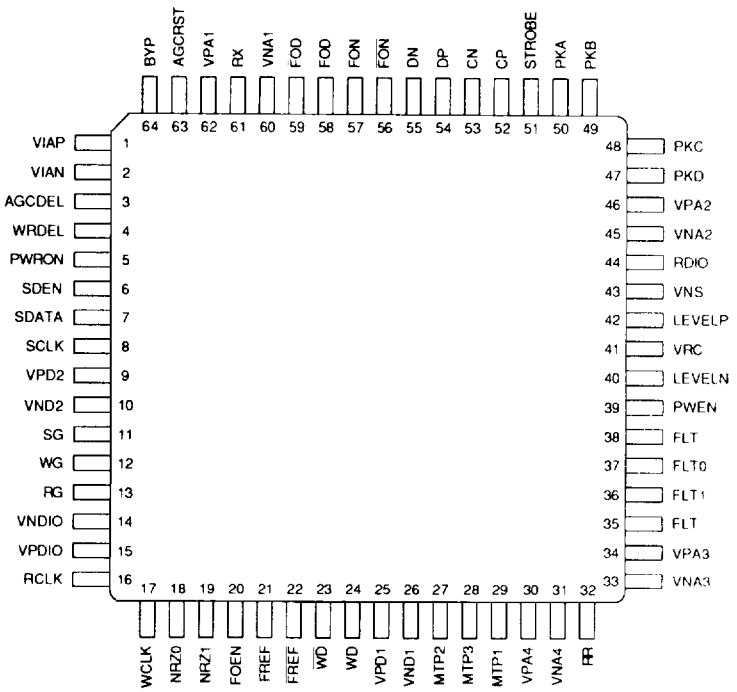
TABLE 5: 1,7 RLL Decode

PREVIOUS		PRESENT			NEXT		DECODED DATA	
Y	Y	Y	Y	Y	Y	Y	D	D
2	3	1	2	3	1	2	1	2
0	0	0	0	0			0	1
1	0	0	0	0			0	0
0	1	0	0	0			0	1
		1	0	0			1	1
	0	0	1	0	0	0	1	1
	0	0	1	0	1	0	1	0
	0	0	1	0	0	1	1	0
	1	0	1	0	0	0	0	1
	1	0	1	0	1	0	0	0
	1	0	1	0	0	1	0	0
0	0	0	0	1			0	1
1	0	0	0	1			0	0
0	1	0	0	1			0	0
		1	0	1			1	0

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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