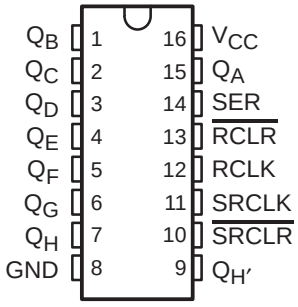
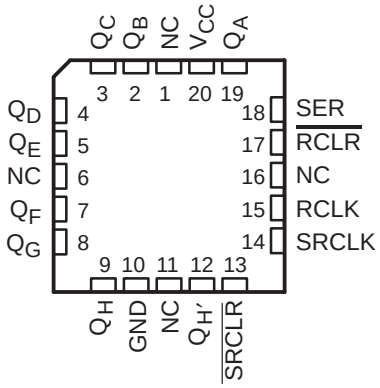
- ***EPIC*** ™ **(Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **8-Bit Serial-In, Parallel-Out Shift Registers With Storage**
- **Independent Direct Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Shift and Storage Registers**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

SN54LV594A . . . J OR W PACKAGE
SN74LV594A . . . D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV594A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’LV594A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on the shift and storage registers. A serial output ($Q_{H'}$) is provided for cascading purposes.

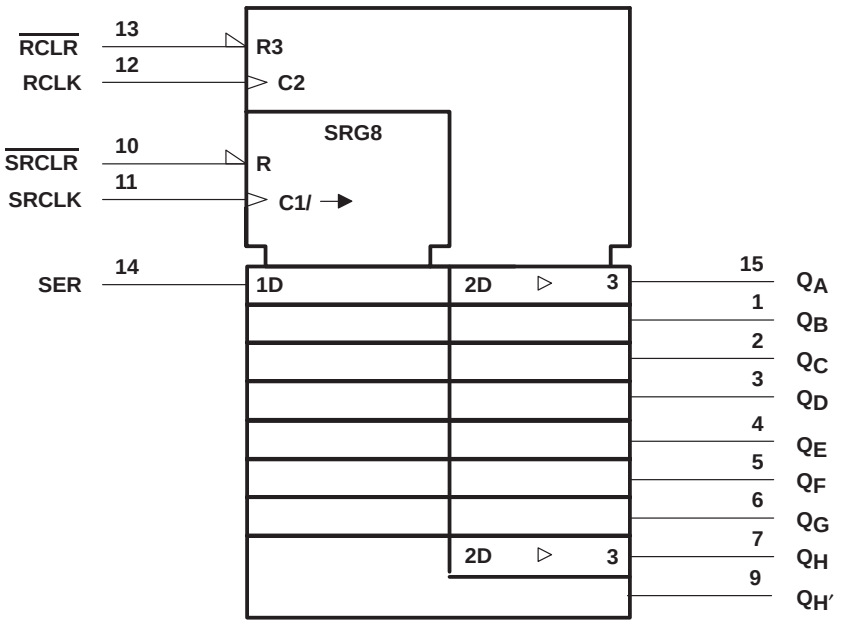
The shift-register (SRCLK) and storage-register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

The SN54LV594A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV594A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

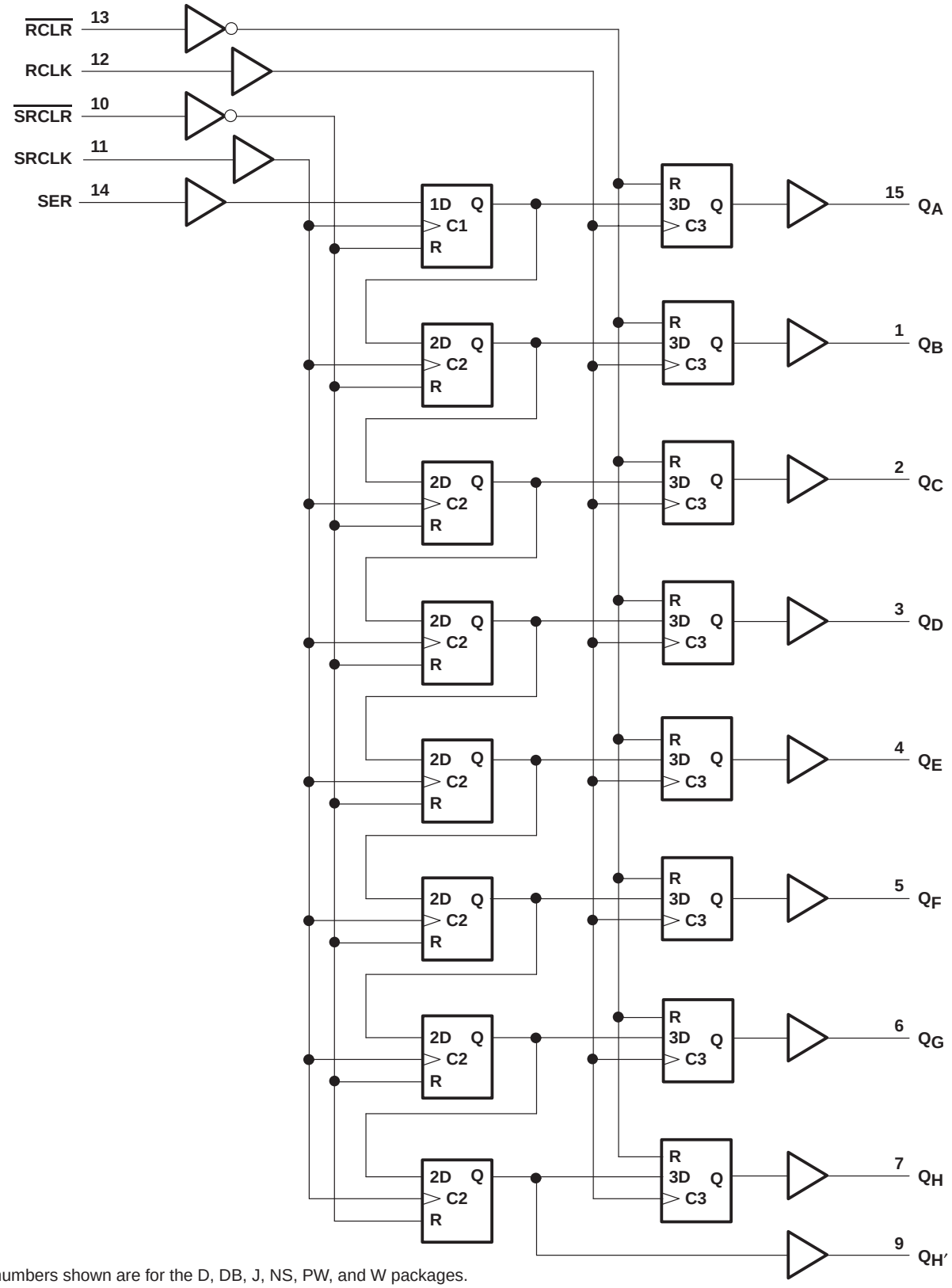
INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

logic symbol†



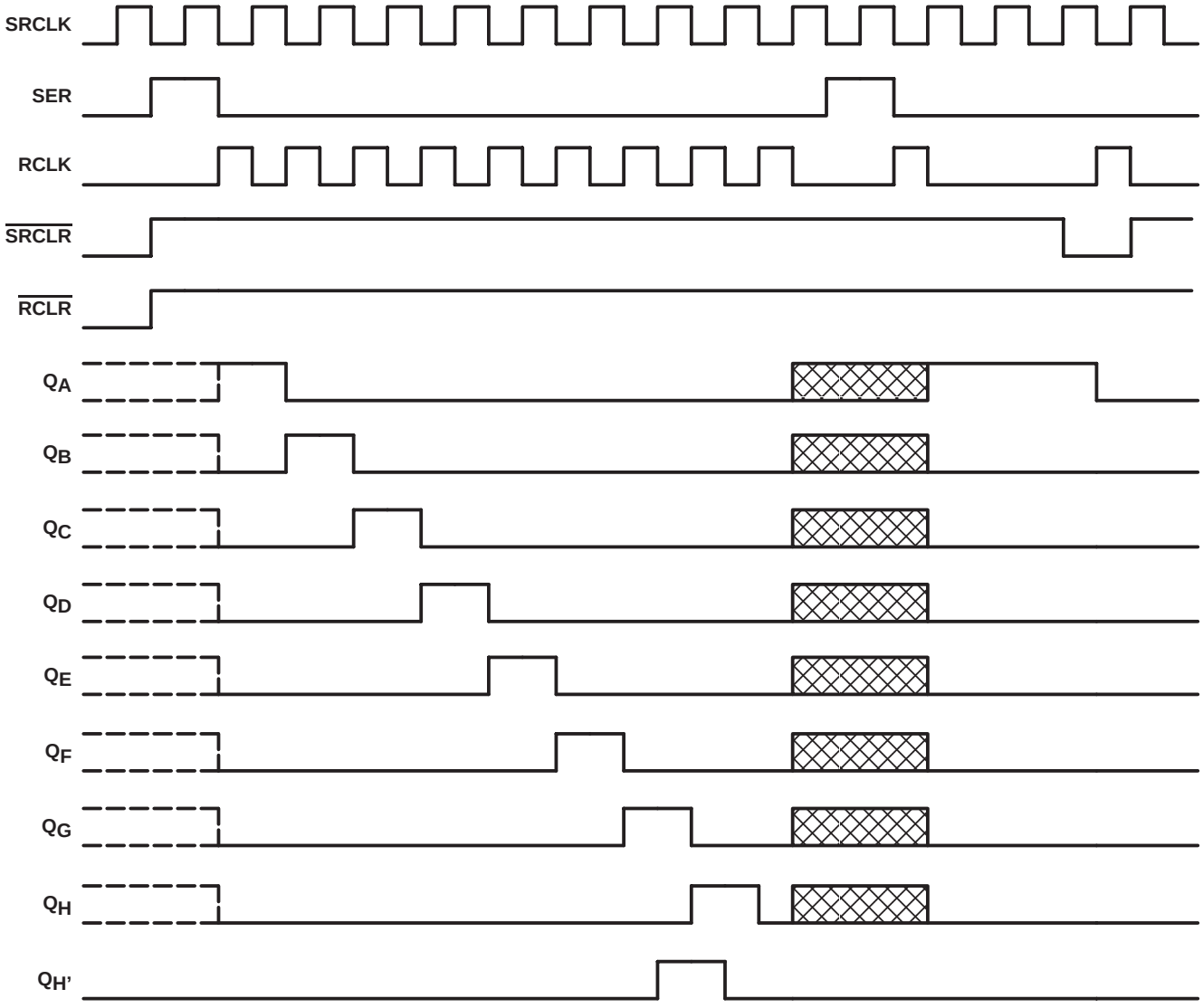
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, NS, PW, and W packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC}\times0.7$		$V_{CC}\times0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC}\times0.7$		$V_{CC}\times0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC}\times0.7$		$V_{CC}\times0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC}\times0.3$		$V_{CC}\times0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC}\times0.3$		$V_{CC}\times0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC}\times0.3$		$V_{CC}\times0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV594A			SN74LV594A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –6 mA	3 V	2.48			2.48			
	I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	5.5 V			±1			±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		3.5			3.5		pF
		5 V		2			2		

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	7		7.5		7.5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	6		6.5		6.5		
t_{su}	Setup time	SER before SRCLK↑	2.5		3		3		ns
		SRCLK↑ before RCLK↑†	8		9		9		
		$\overline{SRCLR}$ low before RCLK↑	8.5		9.5		9.5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	6		6.8		6.8		
		$\overline{RCLR}$ high (inactive) before RCLK↑	6.7		7.6		7.6		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		1.5		ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5.5		5.5		5.5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	5		5		5		
t_{su}	Setup time	SER before SRCLK↑	3.5		3.5		3.5		ns
		SRCLK↑ before RCLK↑†	8		8.5		8.5		
		$\overline{SRCLR}$ low before RCLK↑	8		9		9		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	4.2		4.8		4.8		
		$\overline{RCLR}$ high (inactive) before RCLK↑	4.6		5.3		5.3		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		1.5		ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5		5		5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	5.2		5.2		5.2		
t_{su}	Setup time	SER before SRCLK↑	3		3		3		ns
		SRCLK↑ before RCLK↑†	5		5		5		
		$\overline{SRCLR}$ low before RCLK↑	5		5		5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2.9		3.3		3.3		
		$\overline{RCLR}$ high (inactive) before RCLK↑	3.2		3.7		3.7		
t_h	Hold time	SER after SRCLK↑	2		2		2		ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	65	80		45		45		MHz
			C_L = 50 pF	60	70		40		40		
t_{PLH}*	RCLK	Q_A–Q_H	C_L = 15 pF		6.4	10.6	1	11.1	1	11.1	ns
t_{PHL}*					6.3	10.4	1	11.1	1	11.1	
t_{PLH}*	SRCLK	$Q_{H'}$			7.4	12.1	1	12.8	1	12.8	
t_{PHL}*					7.2	11.6	1	12.8	1	12.8	
t_{PHL}*	$\overline{RCLR}$	Q_A–Q_H			7.9	12.7	1	13.6	1	13.6	
t_{PHL}*	$\overline{SRCLR}$	$Q_{H'}$			7.4	11.9	1	13.1	1	13.1	
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		9.5	14.1	1	14.6	1	14.6	ns
t_{PHL}					10.8	15.5	1	17.2	1	17.2	
t_{PLH}	SRCLK	$Q_{H'}$			10.6	15.7	1	16.5	1	16.5	
t_{PHL}					11.3	16.1	1	18.6	1	18.6	
t_{PHL}	$\overline{RCLR}$	Q_A–Q_H			12.1	17.4	1	19	1	19	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			11.6	16.5	1	18.6	1	18.6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	80	120		70		70		MHz
			C_L = 50 pF	55	105		50		50		
t_{PLH}*	RCLK	Q_A–Q_H	C_L = 15 pF		4.6	8	1	8.5	1	8.5	ns
t_{PHL}*					4.9	8.2	1	8.8	1	8.8	
t_{PLH}*	SRCLK	$Q_{H'}$			5.4	9.1	1	9.7	1	9.7	
t_{PHL}*					5.5	9.2	1	9.9	1	9.9	
t_{PHL}*	$\overline{RCLR}$	Q_A–Q_H			6	9.8	1	10.6	1	10.6	
t_{PHL}*	$\overline{SRCLR}$	$Q_{H'}$			5.6	9.2	1	10	1	10	
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		6.9	10.5	1	11.1	1	11.1	ns
t_{PHL}					8.1	11.9	1	13.1	1	13.1	
t_{PLH}	SRCLK	$Q_{H'}$			7.7	11.7	1	12.4	1	12.4	
t_{PHL}					8.4	12.5	1	13.9	1	13.9	
t_{PHL}	$\overline{RCLR}$	Q_A–Q_H			9.1	13.1	1	14.4	1	14.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			8.5	12.4	1	14	1	14	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	135	170		115		115		MHz
			C_L = 50 pF	120	140		95		95		
t_{PLH}*	RCLK	Q_A–Q_H	C_L = 15 pF		3.3	6.2	1	6.5	1	6.5	ns
t_{PHL}*					3.7	6.5	1	6.9	1	6.9	
t_{PLH}*	SRCLK	$Q_{H'}$			3.7	6.8	1	7.2	1	7.2	
t_{PHL}*					4.1	7.2	1	7.6	1	7.6	
t_{PHL}*	$\overline{RCLR}$	Q_A–Q_H			4.5	7.6	1	8.2	1	8.2	
t_{PHL}*	$\overline{SRCLR}$	$Q_{H'}$			4.1	7.1	1	7.6	1	7.6	
t_{PLH}	RCLK	Q_A–Q_H	C_L = 50 pF		4.9	7.8	1	8.3	1	8.3	ns
t_{PHL}					5.8	8.9	1	9.7	1	9.7	
t_{PLH}	SRCLK	$Q_{H'}$			5.5	8.6	1	9.1	1	9.1	
t_{PHL}					6	9.2	1	10.1	1	10.1	
t_{PHL}	$\overline{RCLR}$	Q_A–Q_H			6.6	10	1	10.7	1	10.7	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$			6	9.2	1	10.1	1	10.1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

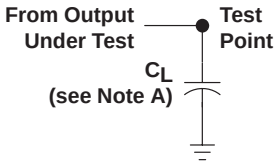
PARAMETER		SN74LV594A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

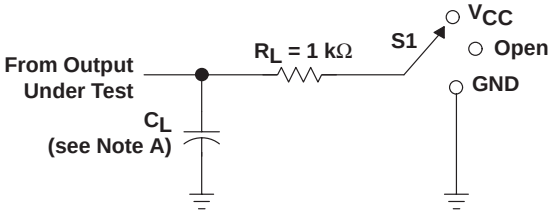
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	3.3 V	93	pF
			5 V	112	

PARAMETER MEASUREMENT INFORMATION

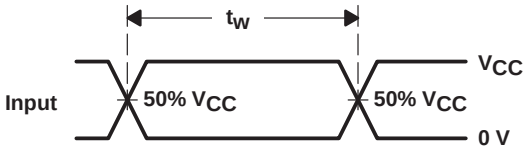


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

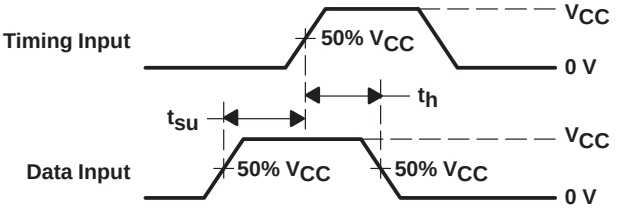


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

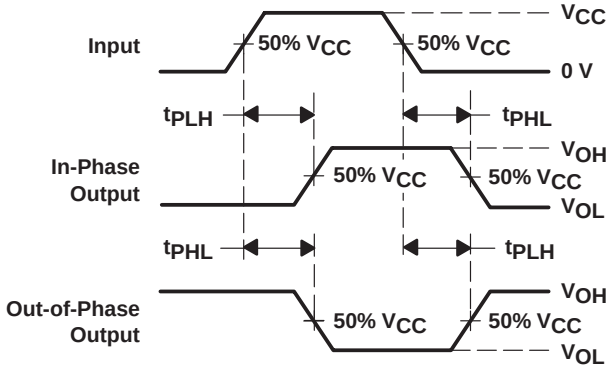
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



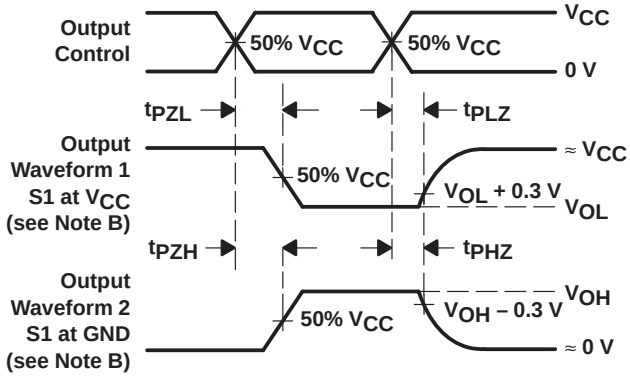
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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