National Semiconductor

MICROCIRCUIT DATA SHEET

MN100341-X REV 2B0

Original Creation Date: 10/04/96
Last Update Date: 05/07/04
Last Major Revision Date: 08/18/99

LOW POWER 8-BIT SHIFT REGISTER

General Description

The F100341 contains eight edge-trigged, D-type flipflops with individual inputs (Pn) and outputs (Qn) for parallel operation and with serial inputs (Dn) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transistion of the clock pulse and their outputs respond a propagation delay after the rising clock edge.

The circuit operating mode is determined by the Select inputs S0 and S1, which are internally decoded to select either "parallel entry" "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50K ohms pull down resistor.

Industry Part Number

100341

Prime Die

F341

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

100341DMQB
100341FMQB
100341J-QMLV
100341W-QMLV
100341WFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 35% power reduction of the 100141
- 2000V ESD protection
- Pin/Function compatible with 100141
- Voltage compensated operating range= -4.2V to -5.7V
- Available to industrial grade temperature range

CONTROLLING DOCUMENTS:

100341DMQB	5962-9459101MXA
100341FMQB	5962-9459101MYA
100341J-QMLV	5962-9459101VXA
100341W-QMLV	5962-9459101VYA
100341WFQMLV	5962F9459101VYA

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature (Tstg)	-65C to +150C
Maximum Junction Temperature (Tj)	
Ceramic	+175C
Plastic	+150C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	$\geq$2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Industrial	-40 C to +85C
Military	-55C to +125C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, Tc=-55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VM=-0.87V	1, 3	INPUTS		240	uA	1, 2
			1, 3	INPUTS		340	uA	3
IIL	Input Low Current	VEE=-4.2V, VM=-1.83V	1, 3	INPUTS	0.5		uA	1, 2, 3
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING:50 Ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING:50 OHMS to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading:50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading:50 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	mV	1, 2, 3
IEE	Power Supply Current	VEE=-4.2/-4.8V	1, 3	VEE	-168	-55	mA	1, 2, 3
		VEE=-5.7V	1, 3	VEE	-178		mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2V to -5.7V, LOADING: 50 Ohms to -2.0V, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH/tpHL(1)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	CP to Qn	0.5	2.3	ns	9
			2, 4	CP to Qn	0.5	2.8	ns	10
			2, 4	CP to Qn	0.5	2.5	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V	6	Qn	0.3	1.3	ns	9, 10, 11
tS(1)	Setup Time	VEE=-4.2/-5.7V	6	Dn to CP	0.6		ns	9, 10, 11
tS(2)	Setup Time	VEE=-4.2/-5.7V	6	Pn to CP	0.6		ns	9, 10, 11
tS(3)	Setup Time	VEE=-4.2/-5.7V	6	Sn to CP	1.6		ns	9
			6	Sn to CP	2.4		ns	10
			6	Sn to CP	1.7		ns	11
tH(1)	Hold Time	VEE=-4.2/-5.7V	6	Dn to CP	0.9		ns	9, 10, 11
tH(2)	Hold Time	VEE=-4.2/-5.7V	6	Pn to CP	0.9		ns	9, 10, 11
tH(3)	Hold Time	VEE=-4.2/-5.7V	6	Sn to CP	0.5		ns	9, 10, 11
tPW(H)	Pulse Width	VEE= -4.2/-5.7V	6	CP	2.0		ns	9, 10, 11
fmax	Maximum Clock Frequency	VEE= -4.2/-5.7V	6	CP	400		MHz	9, 11
			6	CP	300		MHz	10

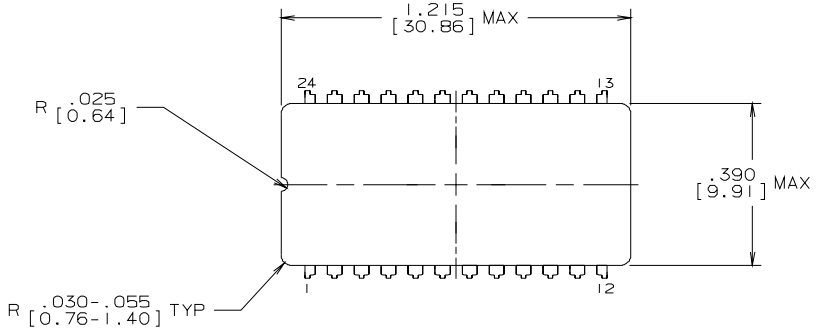
Note 1: Screen tested 100% on each device at +25C, +125C and -55C temperature, subgroups 1, 2, 3, 7 & 8.
Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125 & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature, subgroup A9, and at +125C & -55C temperature, subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature only, subgroup A9.
Note 6: Not tested at +25C, +125C & -55C temperature (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

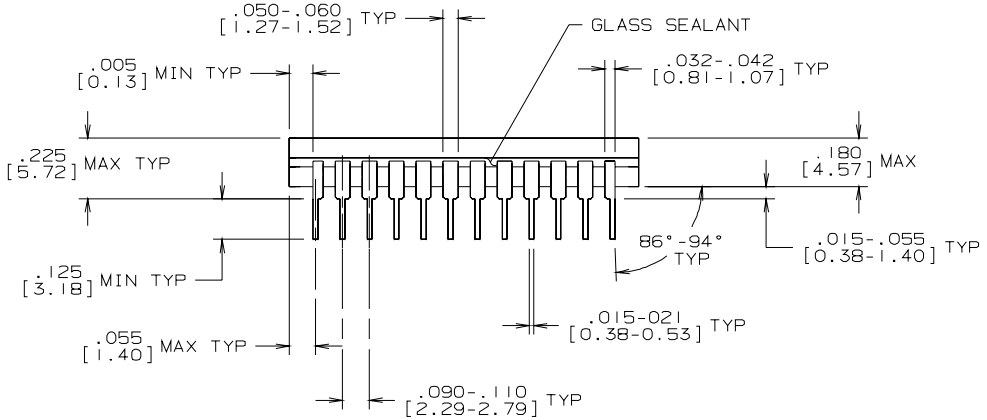
Graphics and Diagrams

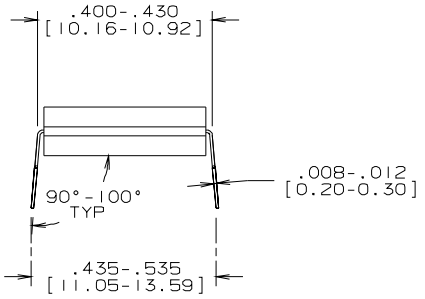
GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP (J), 24LD, .400 CENTERS (P/P DWG)
P000072A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000073A	CERPACK, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPACK, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN D.E.GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
MM

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 24 LEAD, .400 CENTERS

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-J24E	J

FORMERLY: N/A

SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
2A0	M0003556	05/07/04	Donald B. Miller	1) Page 5, fmax specification, change limits from being maximums to minimums. Also, change subgroup "11, 12" to read subgroup "9, 11" on the 400 MHz limit. 2) Page 4, VOHC specification, -1085mV limit, change the subgroup from "1" to "3".
2B0	M0004383	05/07/04	Rose Malone	Update MDS: MN100341-X, Rev. 2A0 to 2B0. Added NSID 100341WFQMLV to Main Table and to Features Section.