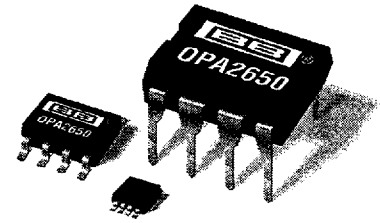
BURR-BROWN®



OPA2650

Dual Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 50mW/Chan.
- UNITY GAIN STABLE BANDWIDTH: 360MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW HARMONICS: –77dBc at 5MHz
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- HIGH OUTPUT CURRENT: 85mA

APPLICATIONS

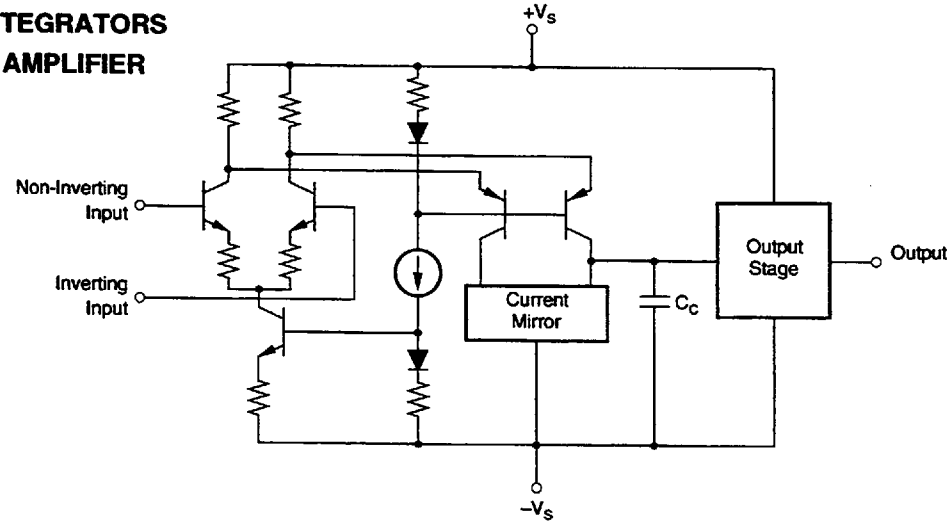
- HIGH RESOLUTION VIDEO
- BASEBAND AMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA2650 is a dual, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 360MHz as well as a 12-bit settling time of only 20ns. The low distortion allows its use in communications applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA2650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA2650 is also available in single (OPA650) and quad (OPA4650) configurations.



NOTE: Diagram shows only one-half of the OPA2650.

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PDS-1266C

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SPECIFICATIONS

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA2650P, U, E			OPA2650PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth[2]	G = +1		360			*[1]		MHz
	G = +2		108			*		MHz
	G = +5		32			*		MHz
	G = +10		16			*		MHz
Gain Bandwidth Product	G ≥ +5		160					MHz
Bandwidth for 0.1dB Flatness[2]	G = +2		21			*		MHz
Slew Rate[3]	G = +1, 2V Step		240			*		V/µs
Over Temperature Range			220			*		V/µs
Rise Time	G = +1, 0.2V Step		1			*		ns
Fall Time	G = +1, 0.2V Step		1			*		ns
Settling Time 0.01%	G = +1, 2V Step		20			*		ns
0.1%	G = +1, 2V Step		11			*		ns
1%	G = +1, 2V Step		6.7			*		ns
Spurious Free Dynamic Range	G = +1, f = 5.0MHz, V_O = 2Vp-p							
	R_L = 100Ω		72			*		dB
	R_L = 402Ω		77			*		dB
Differential Gain	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.01			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.025			*		Degrees
Crosstalk[2]	Input Referred, 5MHz, Channel-to-Channel		–84			*		dB
INPUT OFFSET VOLTAGE								
Input Offset Voltage	V_{CM} = 0V		±1	±5		±1	±3	mV
Average Drift			±3			*		µV/°C
Power Supply Rejection (+V_S)	Input Referred, V_S = ±4.5V to ±5.5V	60	76		70	*		dB
(–V_S)		47	54		50	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		5	20		*	10	µA
Over Temperature Range				30			20	µA
Input Offset Current	V_{CM} = 0V		0.5	1		0.2	0.5	µA
Over Temperature Range				3			2	µA
INPUT NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			43			*		nV/√Hz
f = 10kHz			9.4			*		nV/√Hz
f ≥ 1MHz			8.4			*		nV/√Hz
Integrated Noise								
f_B = 10Hz to 100MHz			84			*		µVrms
Input Bias Current Noise								
Noise Density, f ≥ 0.1MHz			1.2			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.8			*		V
Over Temperature Range		±2.2			*			V
Common-Mode Rejection	Input Referred, V_{CM} = ±0.5V	65	90		70	*		dB
INPUT IMPEDANCE								
Differential			15 ‖ 1			*		KΩ ‖ pF
Common-Mode			16 ‖ 1			*		MΩ ‖ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		47	*		dB
Over Temperature Range		43			45			dB
OUTPUT								
Voltage Output								
Over Temperature Range	No Load	±2.2	±3.0		±2.4	*		V
	R_L = 250Ω	±2.2	±2.5		±2.4	*		V
	R_L = 100Ω	±2.0	±2.3		±2.2	*		V
Output Current, Sourcing		75	110		*	*		mA
Over Temperature Range		65			*			mA
Output Current, Sinking		65	85		*	*		mA
Over Temperature Range		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	f < 100kHz, G = +1		0.08			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	Both Channels, V_S = ±5V		±11	±15.5		*	±13.5	mA
Over Temperature Range				±17.5		*	±16	mA
THERMAL CHARACTERISTICS								
Temperature Range	Specification: P, U, E, PB, UB	–40		+85	*		*	°C
Thermal Resistance, θ_{JA}	Junction to Ambient							
P 8-Pin DIP			100			*		°C/W
U SO-8			125			*		°C/W
E MSOP-8			150			*		°C/W

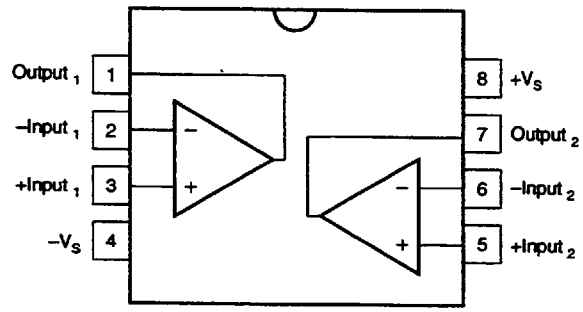
NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The demonstration boards show low parasitic layouts for this part. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±5.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, PB, U, UB, E	–40°C to +125°C
Lead Temperature (DIP, soldering, 10s)	+300°C
(SO-8 and MSOP-8, soldering, 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION

Top View DIP/SO-8/MSOP-8



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE/ORDERING INFORMATION

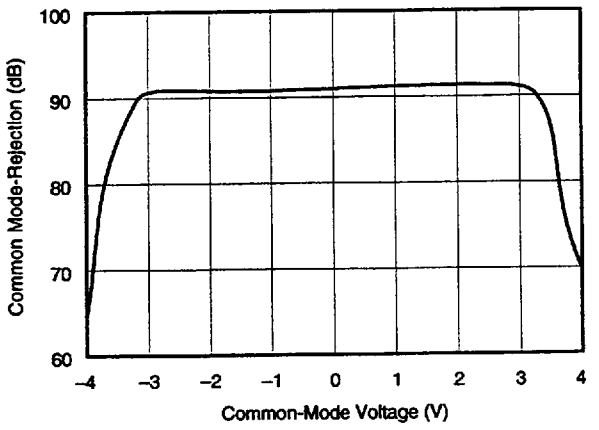
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER(3)
OPA2650P	8-Pin Plastic DIP	006	–40°C to +85°C	OPA2650P	OPA2650P
OPA2650PB	8-Pin Plastic DIP	006	–40°C to +85°C	OPA2650PB	OPA2650PB
OPA2650U	SO-8 Surface Mount	182	–40°C to +85°C	OPA2650U	OPA2650U
OPA2650UB	SO-8 Surface Mount	182	–40°C to +85°C	OPA2650UB	OPA2650UB
OPA2650E	MSOP-8	337	–40°C to +85°C	B50	OPA2650E-250 OPA2650E-2500

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade will be marked with a "B" by pin 8. (3) The MSOP-8 is available on 7" tape and reel with 250 parts, and on 14" tape and reel with 2500 parts. For example, ordering 250 pieces of "OPA2650E-250" will get a single 250 piece tape and reel. Refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

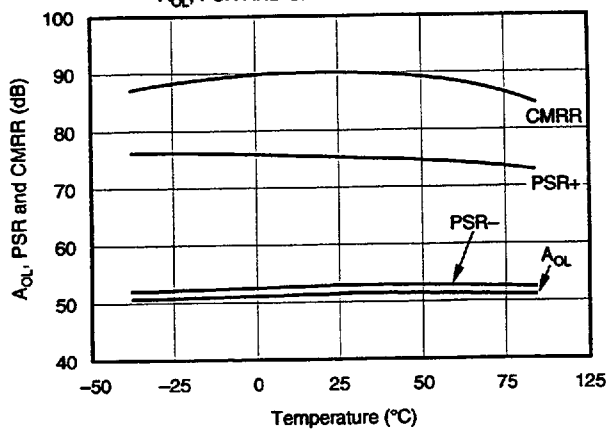
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

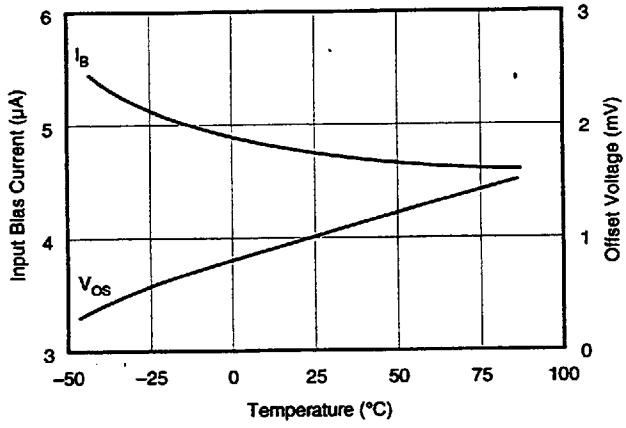
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



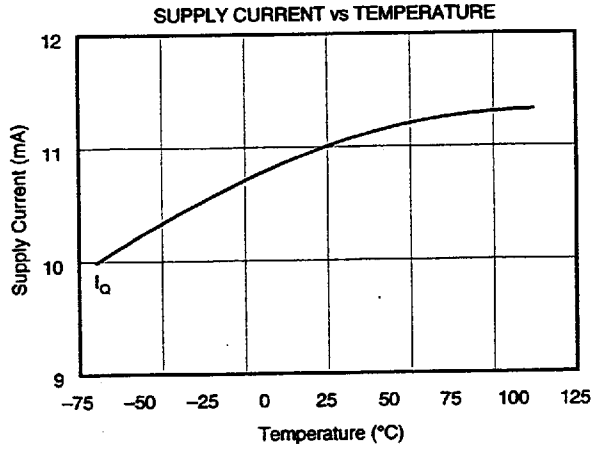
A_{OL}, PSR AND CMRR vs TEMPERATURE



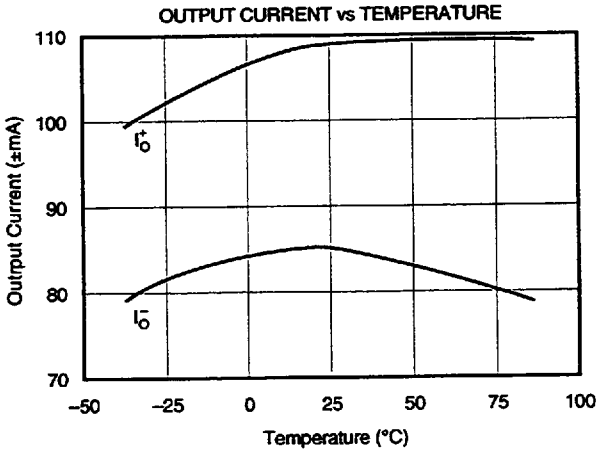
INPUT BIAS CURRENT vs TEMPERATURE



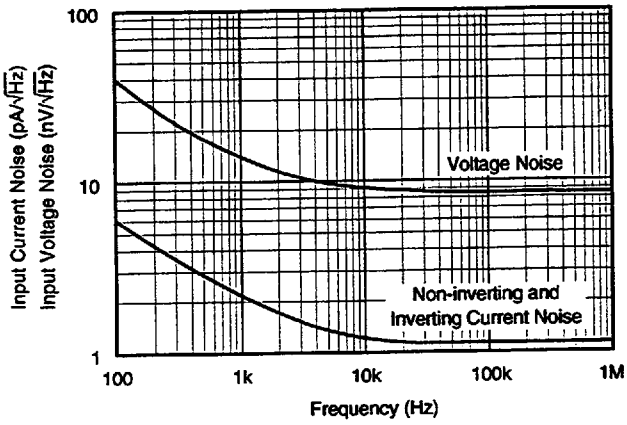
SUPPLY CURRENT vs TEMPERATURE



OUTPUT CURRENT vs TEMPERATURE



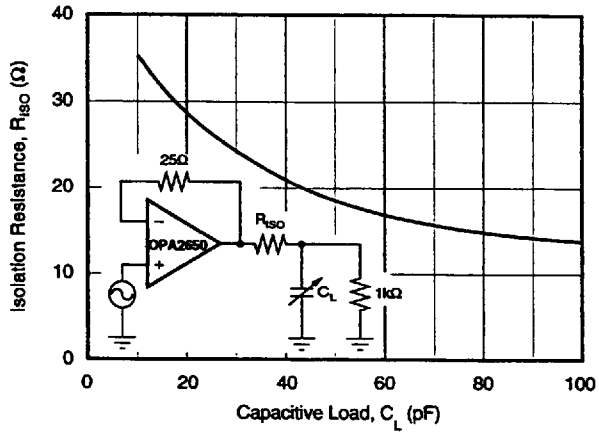
INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY



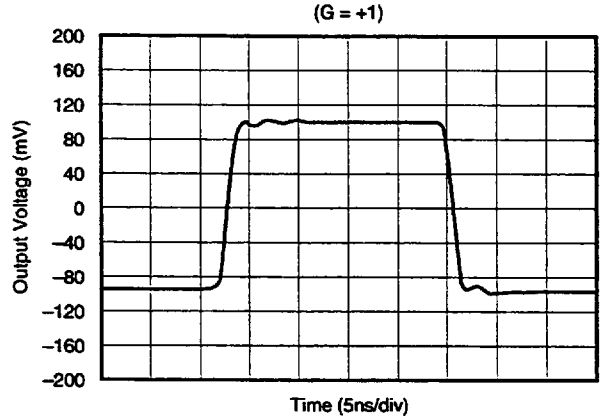
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

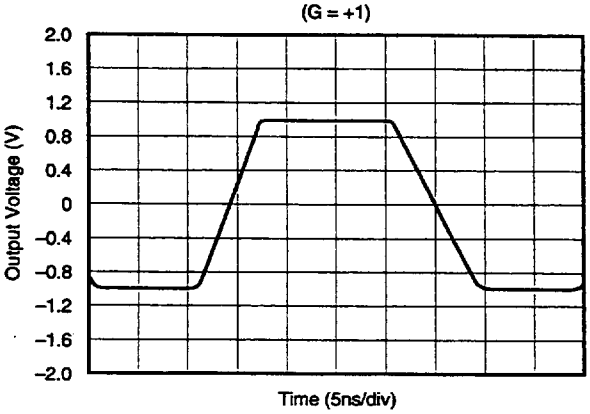
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



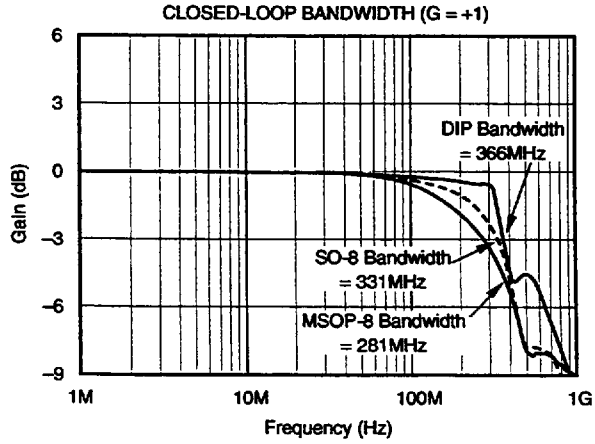
SMALL SIGNAL TRANSIENT RESPONSE (G = +1)



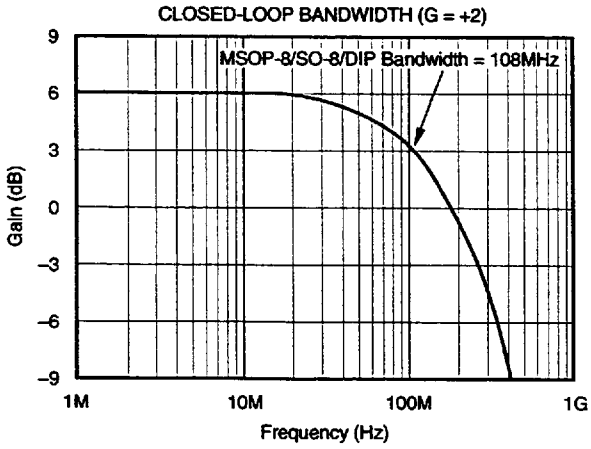
LARGE SIGNAL TRANSIENT RESPONSE (G = +1)



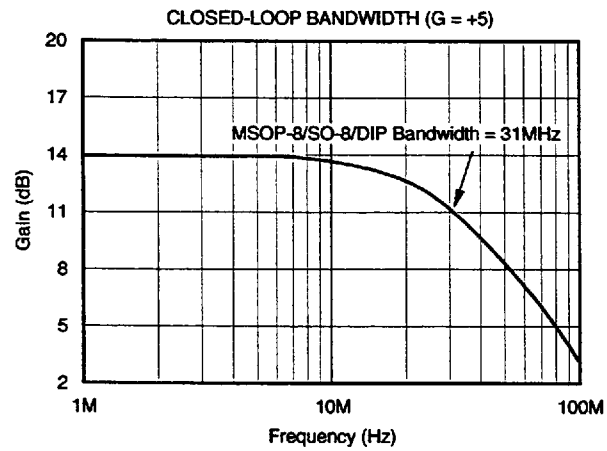
CLOSED-LOOP BANDWIDTH (G = +1)



CLOSED-LOOP BANDWIDTH (G = +2)



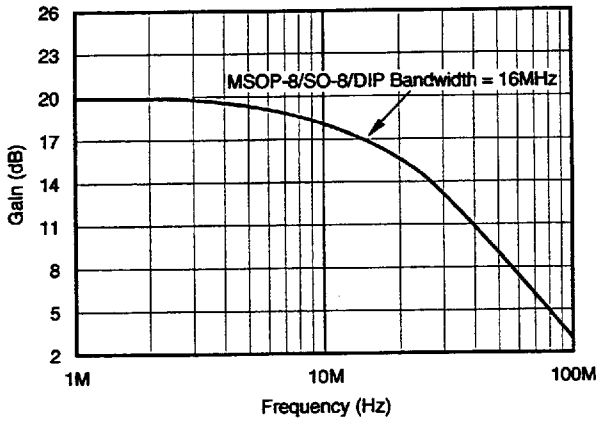
CLOSED-LOOP BANDWIDTH (G = +5)



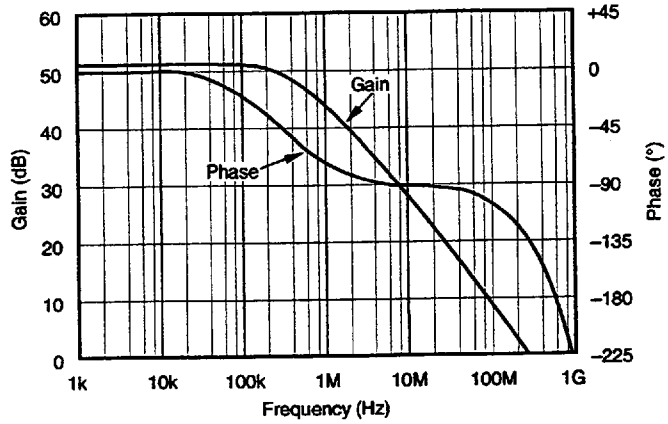
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

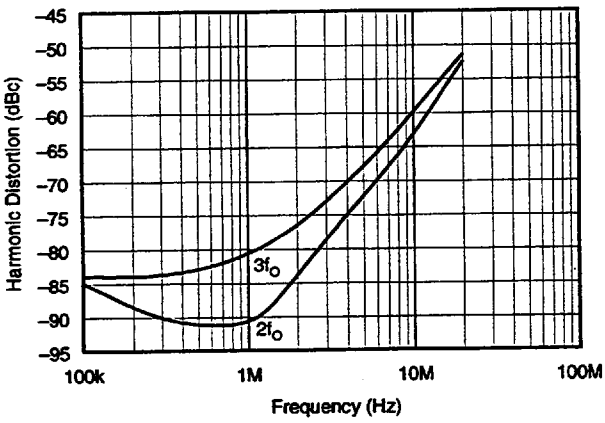
CLOSED-LOOP BANDWIDTH (G = +10)



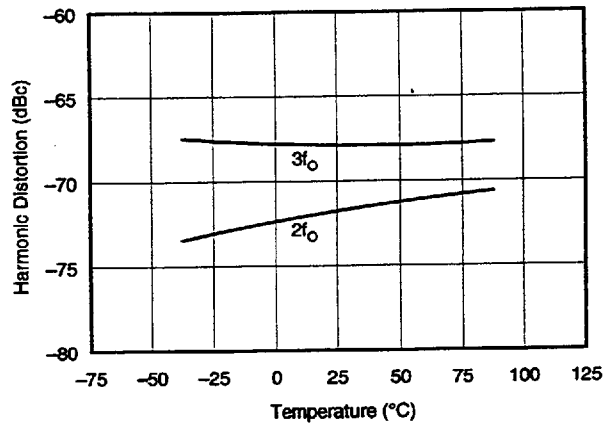
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



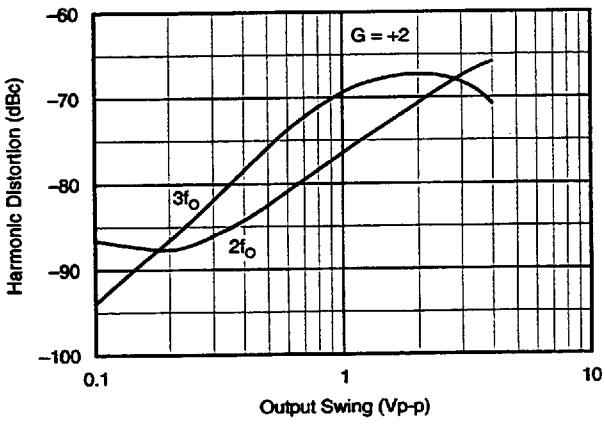
HARMONIC DISTORTION vs FREQUENCY (G = +1, V_O = 2Vp-p)



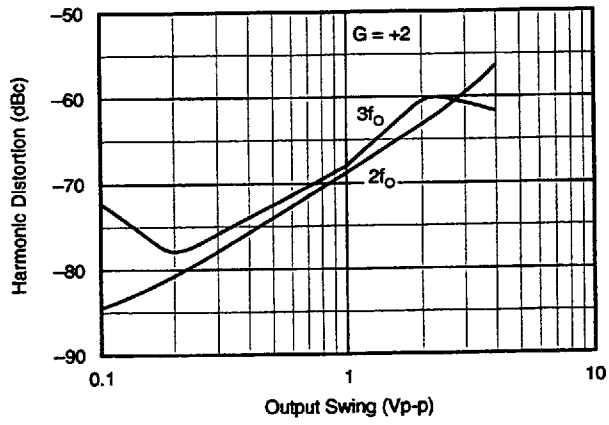
HARMONIC DISTORTION vs TEMPERATURE (G = +1, f_O = 5MHz)



5MHz HARMONIC DISTORTION vs OUTPUT SWING

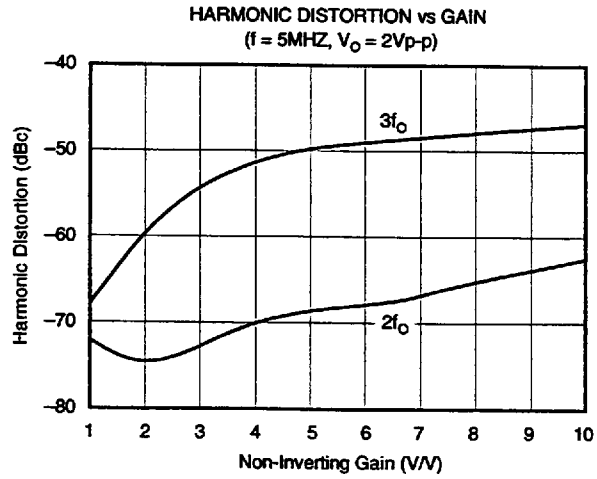


10MHz HARMONIC DISTORTION vs OUTPUT SWING



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA2650 is a dual low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA2650's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA2650 well suited for implementing filter and instrumentation designs. As a dual operational amplifier, OPA2650 is an ideal choice for designs requiring multiple channels where reduction of board space, power dissipation and cost are critical. Its AC performance is optimized to provide a gain bandwidth product of 160MHz and a fast 0.1% settling time of 11ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low DC input offset of ±1mV and drift of ±3µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the dual current feedback OPA2658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA2650 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA2650. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting the resistor, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit

operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for a unity gain follower. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA2650 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Sockets are not recommended for high speed parts like the OPA2650. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

SUPPLY VOLTAGES

The OPA2650 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

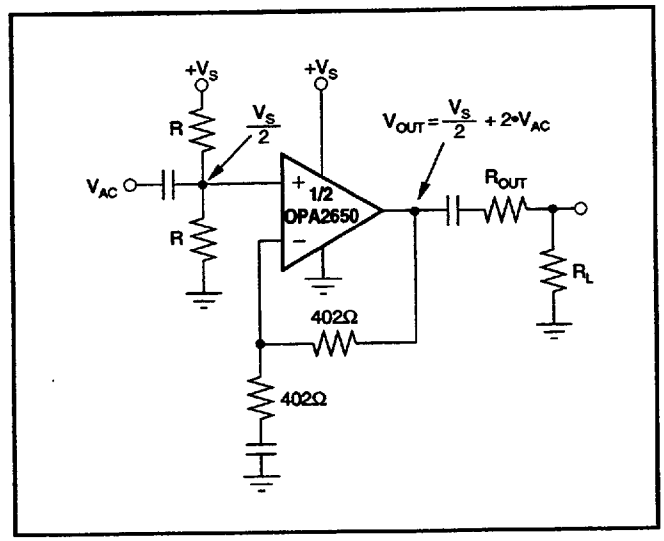


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 2 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce the output offset voltage caused by the amplifier's input offset current.

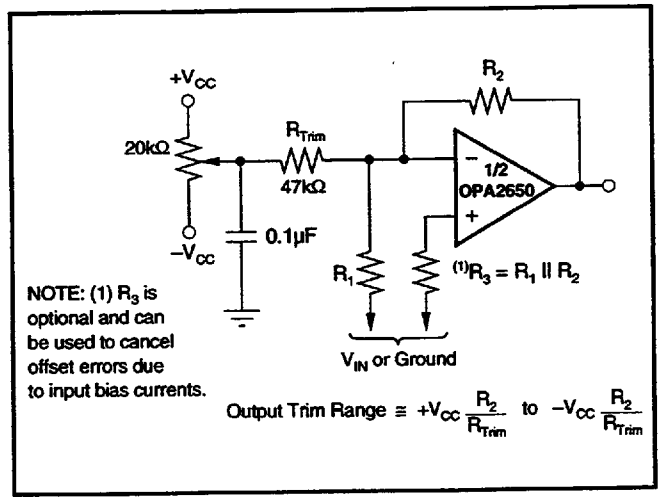


FIGURE 2. Offset Voltage Trim.

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA2650.

OUTPUT DRIVE CAPABILITY

The OPA2650 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA2650 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA2650 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain decreases with frequency.

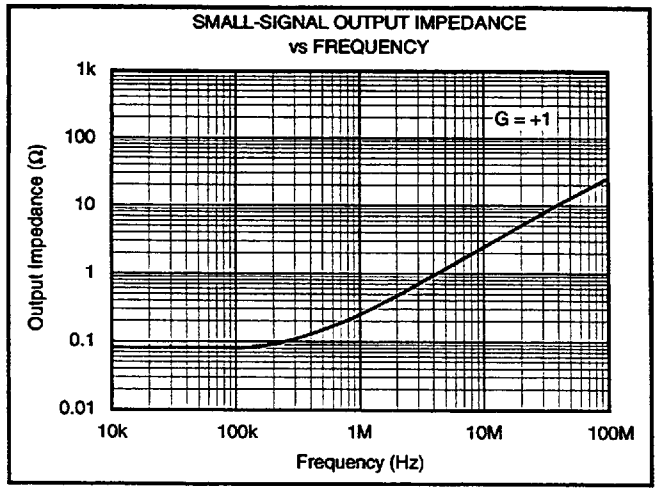


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA2650 will not require heatsinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

The total internal power dissipation (P_D) is a the sum of quiescent power (P_{DQ}) and additional power dissipated in the two output stages (P_{DL1} and P_{DL2}) while delivering load power. Quiescent power is simply the specified no-load supply current for both channels times the total supply voltage across the part. P_{DL1} and P_{DL2} will depend on the required output signals and loads. For a grounded resistive loads, and equal bipolar supplies, they would be at a maximum when the outputs are fixed at a voltage equal to 1/2 either supply voltage. Under this condition, $P_{DL1} = V_S^2/(4 \bullet R_{L1})$ where R_{L1} includes feedback network loading. P_{DL2} is calculated the same way.

Note that it is the power in the output stages, and not into the loads, that determines internal power dissipation.

Operating junction temperature (T_J) is given by $T_A + P_D \theta_{JA}$, where T_A is the ambient temperature.

As an example, compute the maximum T_J for an OPA2650U where both op amps are at G = +2, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, and at the specified maximum $T_A = +85°C$. This gives:

$$P_{DQ} = (10V \bullet 17.5mA) = 175mW$$

$$P_{DL1} = P_{DL2} = \frac{(5V)^2}{4 \bullet (100\Omega \,||\, 804\Omega)} = 70mW$$

$$P_D = 175mW + 2(70mW) = 315mW$$

$$T_J = 85°C + 0.315W \bullet 125°C/W = 124°C$$

CAPACITIVE LOADS

The OPA2650's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 15Ω to 30Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

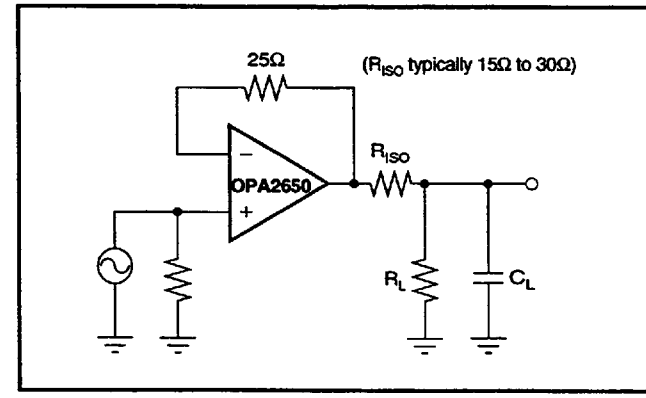


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

Each channel of the OPA2650 is internally compensated to be stable at unity gain with a nominal 60° phase margin. This lends itself well to wideband integrator and buffer applications. Phase margin and frequency response flatness will improve at higher gains. Recall that an inverting gain of −1 is equivalent to a gain of +2 for bandwidth purposes, i.e., noise gain = 2. The external compensation techniques developed for voltage feedback op amps can be applied to this device. For example, in the non-inverting configuration, placing a capacitor across the feedback resistor will reduce the gain to +1 starting at $f = (1/2\pi R_F C_F)$. Alternatively, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, thereby limiting the bandwidth for the inverting input signal through the gain-bandwidth product.

At higher gains, the gain-bandwidth of this voltage feedback topology will limit bandwidth according to the open-loop frequency response curve. For applications requiring a wider bandwidth at higher gains, consider the dual current feedback model, OPA2658. In applications where a large feedback resistor is required (such as photodiode transimpedance circuits), precautions must be taken to avoid gain peaking due to the pole formed by the feedback resistor and the capacitance on the inverting input. This pole can be compensated by connecting a small capacitor in parallel with the feedback resistor, creating a cancelling zero term. In other high-gain applications, use of a three-resistor "T" connection will reduce the feedback network impedance which reacts with the parasitic capacitance at the summing node.

PULSE SETTLING TIME

High speed amplifiers like the OPA2650 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a 2V step at a gain of +1 for the OPA2650 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which offers considerably higher open loop DC gain.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (dG) and Differential Phase (dP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as dG. dP is defined as the change in degrees of the closed-loop phase over the same output voltage change. dG and dP are both specified at the NTSC sub-carrier frequency of 3.58MHz. dG and dP increase closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA2650's harmonic distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

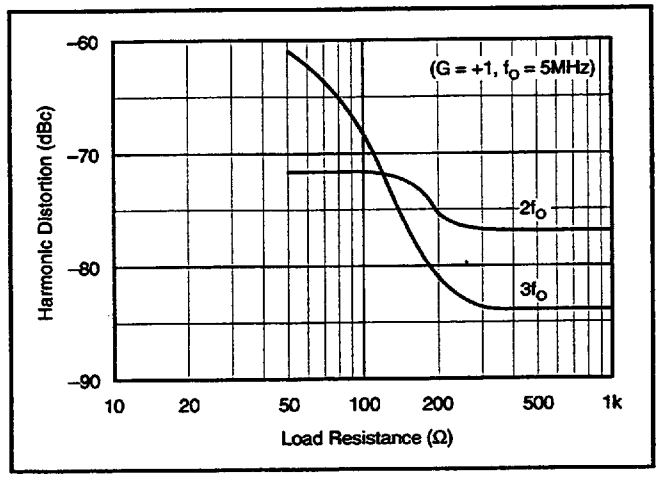


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

CROSSTALK

Crosstalk is the undesired result of the signal of one channel mixing with and reproducing itself in the output of the other channel. Crosstalk occurs in most multichannel integrated circuits. In dual devices, the effect of crosstalk is measured by driving one channel and observing the output of the undriven channel over various frequencies. The magnitude of this effect is referenced in terms of channel-to-channel crosstalk and expressed in decibels. "Input referred" points to the fact that there is a direct correlation between gain and crosstalk, therefore at increased gain, crosstalk also increases by a factor equal to that of the gain. Figure 6 illustrates the measured effect of crosstalk in the OPA2650U.

SPICE MODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available on a disk from the Burr-Brown Applications Department.

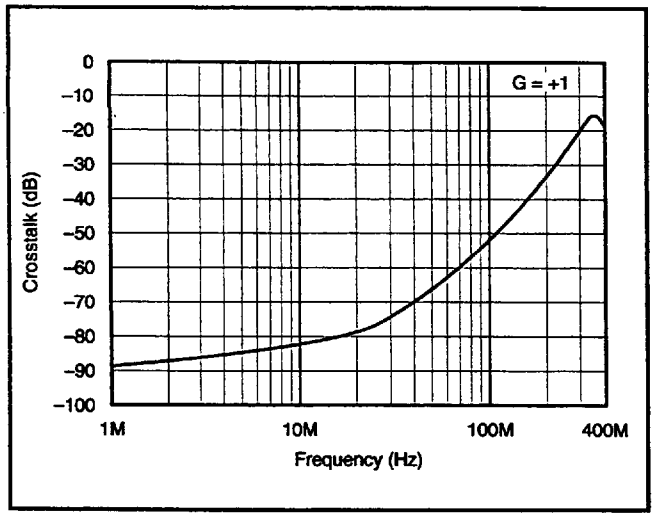


FIGURE 6. Channel-to-Channel Crosstalk.

DEMONSTRATION BOARDS

Demonstration boards are available for each OPA2650 package style. These boards implement a very low parasitic layout that will produce the excellent frequency and pulse responses shown in the Typical Performance Curves. For each package style, the recommended demonstration boards are:

DEMONSTRATION BOARD	PACKAGE	PRODUCT
DEM-OPA265xP	8-Pin DIP	OPA2650P OPA2650PB
DEM-OPA265xU	SO-8	OPA2650U OPA2650UB
DEM-OPA26xxE	MSOP-8	OPA2650E

Contact your local Burr-Brown sales office or distributor to order demonstration boards.

TYPICAL APPLICATION

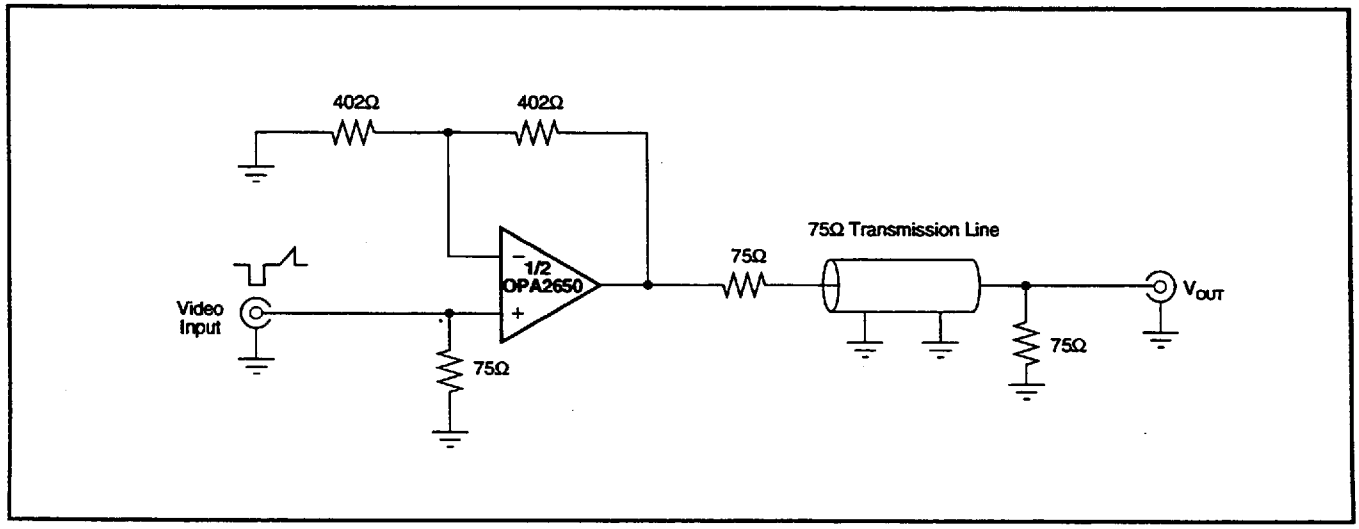


FIGURE 7. Low Distortion Video Amplifier.

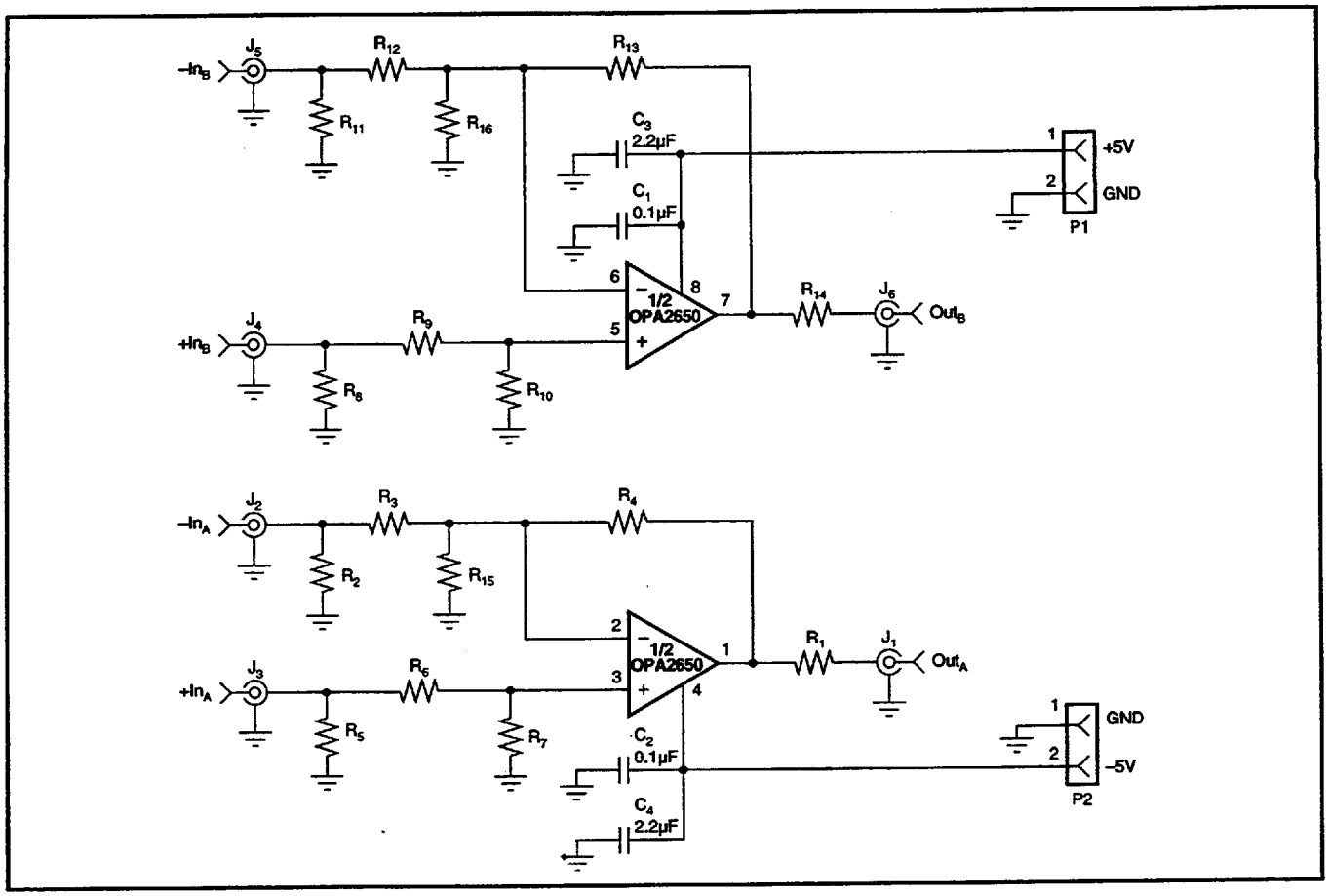


FIGURE 8. Circuit Detail for DEM-OPA265xP Demonstration Board.

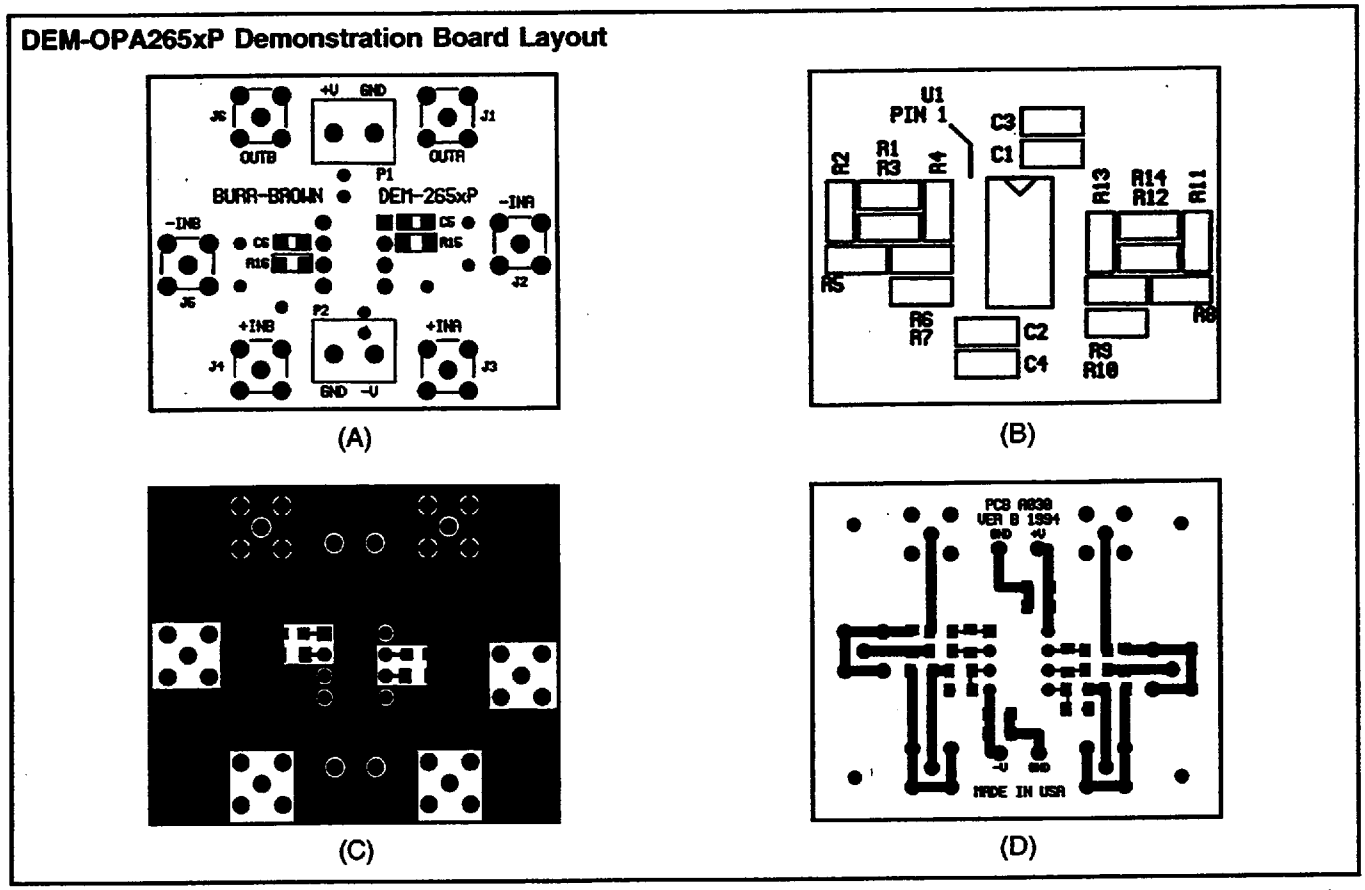


FIGURE 9. Evaluation Board Silkscreen (Solder Side). 9b. Evaluation Board Silkscreen (Component Side). 9c. Evaluation Board Layout (Solder Side). 9d. Evaluation Board (Component Side).

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP

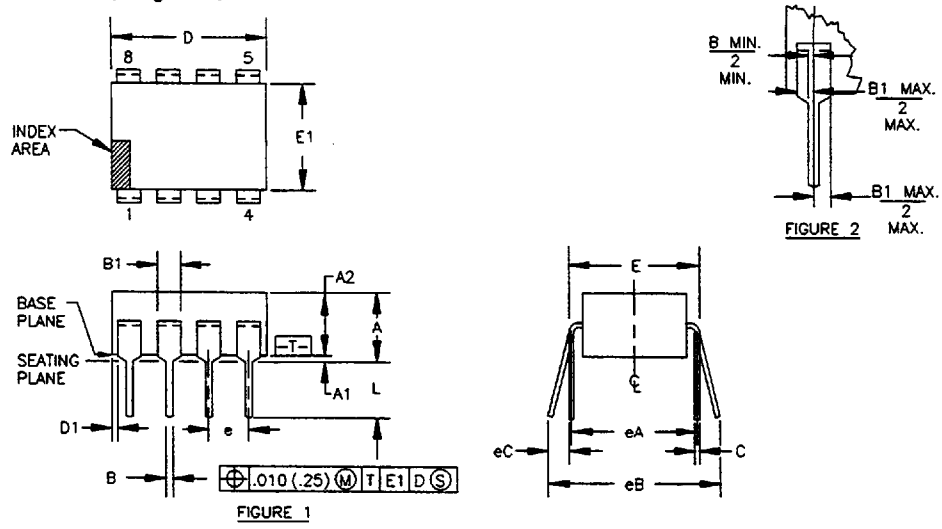


FIGURE 2

FIGURE 1

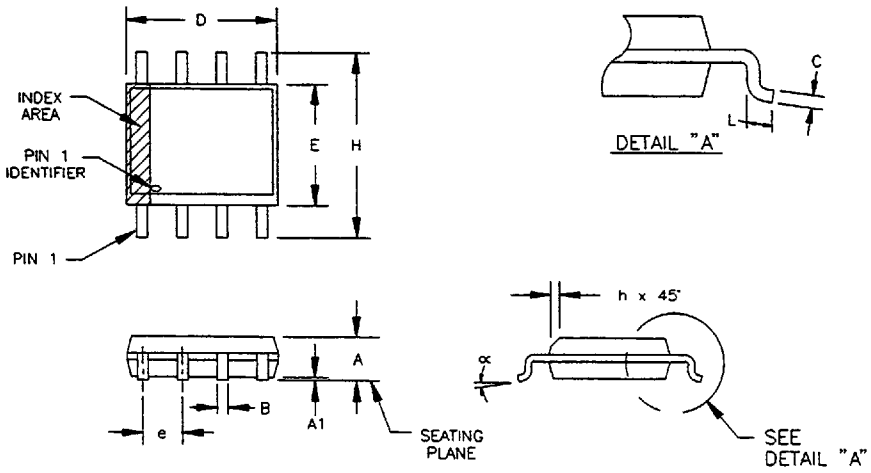
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
B	.014	.022	0.36	0.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	0.20	0.38	
D	.348	.430	8.84	10.92	4
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
L	.115	.160	2.92	4.06	3

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
N	8		8		7

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006	REV.: D
JEDEC NUMBER: MS-001	

Package Number 182 - 8-Lead SO-8 Surface Mount



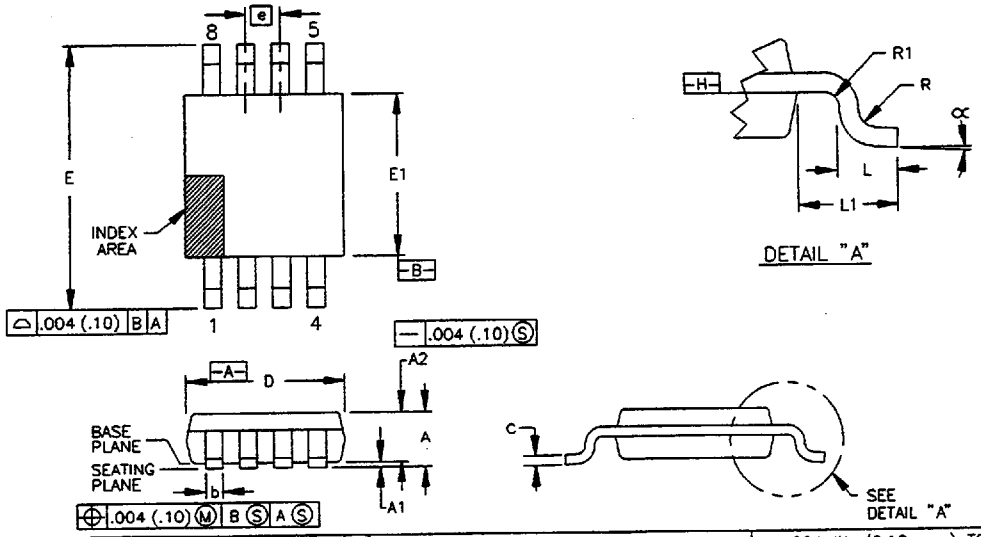
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.054	.068	1.37	1.73	
A1	.004	.009	0.10	0.23	
B	.014	.019	0.36	0.48	
C	.008	.0098	0.20	0.25	
D	.189	.196	4.80	4.98	
E	.150	.157	3.81	3.99	
e	.050 BASIC		1.27 BASIC		
H	.229	.244	5.82	6.20	
h	.010	.019	0.25	0.48	
L	.016	.050	0.41	1.27	
N	8		8		
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182	REV.: F
JEDEC NUMBER: MS-012	

PACKAGE DRAWINGS (CONT)

Package Number 337 - 8-Lead MSOP, .118 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.032	.043	0.81	1.10	
A1	.002	.006	0.05	0.15	
A2	.030	.038	0.76	0.97	
b	.011	.015	0.28	0.38	4
c	.005	.009	0.13	0.23	
D	.114	.122	2.90	3.10	2,8
E	.193 REF		4.90 REF		
E1	.114	.122	2.90	3.10	3,8
e	.0256 BASIC		0.65 BASIC		
L	.0175	.0255	0.45	0.65	
L1	.037 REF		0.94 REF		
N	8		8		6
R	.003	.009	0.08	0.23	
R1	.003	.009	0.08	0.23	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
∝	0°	6°	0°	6°	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES (ANGLES IN DEGREES), UNLESS OTHERWISE SPECIFIED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .004 IN. (0.10 mm) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. NO INTRUSION IS ALLOWED. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
8. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-.
9. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER:	ZZ337	REV.: C
JEDEC NUMBER:	NONE	