National Semiconductor

DP8340/NS32440 IBM 3270 Protocol Transmitter/Encoder

General Description

The DP8340/NS32440 generates a complete encoding of parallel data for high speed serial transmission which conforms to the protocol as defined by the IBM 3270 information display system standard. The DP8340/NS32440 converts parallel input data into a serial data stream. Although the IBM standard covers biphase serial data transmission over a coax line, the DP8340/NS32440 also adapts to general high speed serial data transmission over other than coax lines, at frequencies either higher or lower than the IBM standard.

The DP8340/NS32440 and its complementary chip, the DP8341 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter/receiver functions provides convenient addition of more receivers at one end of a biphase line without the need of unused transmitters. This is specifically advantageous in control units where typical biphase data is multiplexed over many biphase lines and the number of receivers generally exceeds the number of transmitters.

Features

- Ten bits per data byte transmission
- Single-byte or multi-byte transmission
- Internal parity generation (even or odd)
- Internal crystal controlled oscillator used for the generation of all required chip timing frequencies
- Clock output directly drives receiver (DP8341) clock input
- Input data holding register
- Automatic clear status response feature
- Line drivers at data outputs provide easy interface to biphase coax line or general transmission lines
- < 2 ns driver output skew
- Bipolar technology provides TTL input/output compatibility
- Data outputs power up/down glitch free
- Internal power up clear and reset
- Single +5V power supply

Connection Diagrams

Plastic Chip Carrier

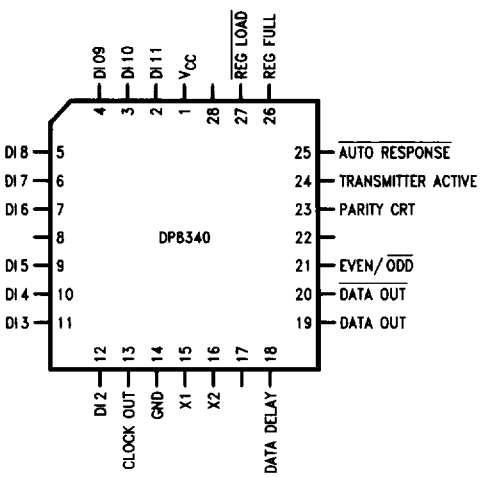

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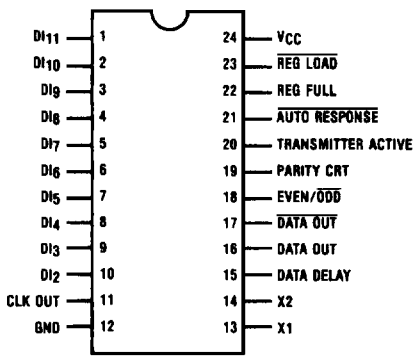
FIGURE 1

Dual-In-Line Package



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Top View

Order Number DP8340/NS32440 J, N or V
See NS Package Number J24A, N24A or V28A

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Block Diagram

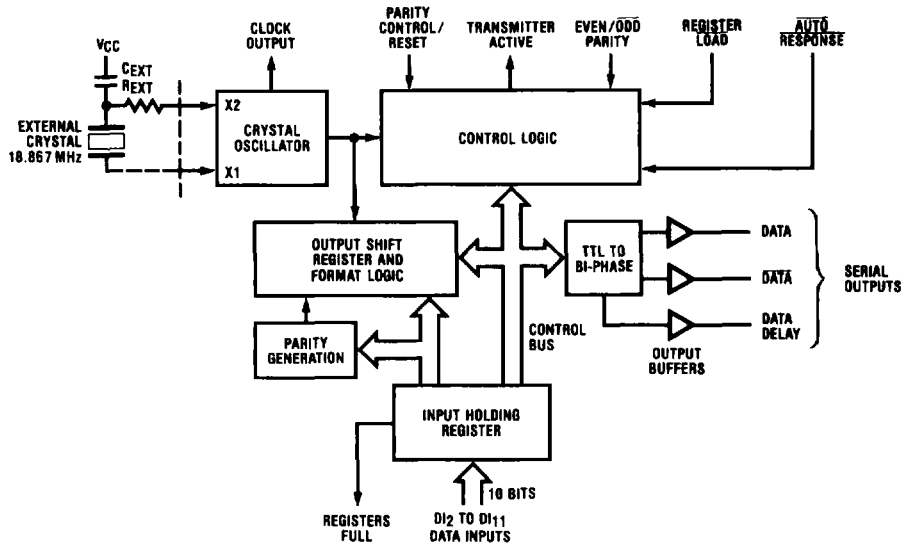

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FIGURE 2. DP8340/NS32440 Serial Bi-Phase Transmitter/Encoder Block Diagram

Functional Description

Figure 2 is a block diagram of the DP8340/NS32440 bi-phase Transmitter/Encoder. The transmitter/encoder contains a crsytal oscillator whose input is a crystal with a frequency eight (8) times the data rate. A Clock Output is provided to drive the DP8341 receiver/decoder Clock Input and other system components at the oscillator frequency. Additionally, the oscillator drives the control logic and output shift register/format logic blocks.

Data is parallel loaded from the sytem data bus to the transmitter/encoder's input holding register. This data is in turn loaded by the transmitter/encoder to its output shift register if this register was empty at the time of the load. During this load, message formatting and parity are generated. The formatted message is then shifted out at the bit rate frequency to the TTL to biphase block which generates the proper data bit formatting. The three data outputs, DATA, $\overline{\text{DATA}}$, and DATA DELAY provide for flexible interface to the coax line with a minimum of external components.

The Control Logic block interfaces to all blocks to insure proper chip operation and sequencing. It controls the type of parity generation through the Even/Odd Parity input. An additional feature provided by the transmitter/encoder is generation of odd parity and placement in bit 10 position while still maintaining even or odd parity in the bit 12 position. This is the format of data word bytes and other commands in the 3270 Standard. The Parity Control input is the pin which controls when this operation is in effect.

Another feature of the transmitter/encoder is the internal TT/AR (Transmission Turnaround/Auto Response) capability. After each Write type message from the control unit in the 3270 Standard, the receiving unit must respond with clean status (bits 2 through 11). With the transmitter/encoder, this function is accomplished simply by forcing the $\overline{\text{Auto-Response}}$ input to the Logic "0" state.

Operation of the transmitter/encoder is automatic. After the first data byte is loaded, the Transmitter Active output is set and the transmitter/encoder immediately formats the input data and serially shifts it out its data outputs. If the message is a multi-byte message, the internal format logic will modify the message data format for multibyte as long as the next byte is loaded to the input holding register before the last data bit of the previous data byte is transferred out of the internal output shift register. After all data is shifted out of the transmitter/encoder the Transmitter Active output will return to the inactive state.

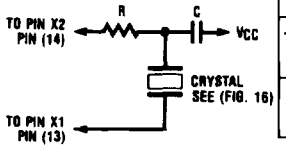
Detailed Pin/Functional Description

Crystal Inputs X1 and X2

The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the osicllator; however, overtone mode crystals may be used.

Crystal Specifications (Parallel Resonant)

Type	AT-cut crystal
Tolerance	0.005% at 25°C
Stability	0.01% from 0°C to +70°C
Resonance	Fundamental (Parallel)
Maximum Series Resistance	Dependent on Frequency (For 18.867 MHz, 50Ω)
Load Capacitance	15 pF



FREQ	R	C
10 MHz to 20 MHz	500Ω ±10%	30 pF
>20 MHz	120Ω ±10%	15 pF

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FIGURE 3. Connection Diagram

If the DP8340/NS32440 transmitter is clocked by a system (clock crystal oscillator not used), pin 13 (X1 input) should be clocked directly using a Schottky series (74S) circuit. Pin 14 (X2 input) may be left open. The clocking frequency must be set at eight times the data bit rate. Maximum input frequency is 28 MHz. For the IBM 3270 Interface, this frequency is 18.867 MHz. At this frequency, the serial bit rate will be 2.358 Mbits/sec.

Clock Output

The Clock Output is a buffered output derived directly from the crystal oscillator block and clocks at the oscillator frequency. It is designed to directly drvie the DP8341 receiver/decoder Clock Input as well as other system components.

Registers Full

This output is used as a flag by the external operating system. A logic "1" (active state) on this output indicates that both the internal output shift register and the input holding register contain active data. No additional data should be loaded until this output returns to the logic "0" state (inactive state).

Transmitter Active

This output will be in the logic "1" state while the transmitter/encoder is about to transmit or in the process of transmitting data. Otherwise, it will assume the logic "0" state indicating no data presently in either the input holding or output shift registers.

$\overline{\text{Register Load}}$

The $\overline{\text{Register Load}}$ input is used to load data from the Data Inputs to the input holding register. The loading function is edge sensitive, the data present during the logic "0" state of this input is loaded, and the input data must be valid before the logic "0" to logic "1" transition. It is after this transition that the transmitter/encoder begins formatting of data for serial transmission.

$\overline{\text{Auto Response}}$ (TT/AR)

This input provides for automatic clear data transmission (all bits in logic "0") without the need of loading all zero's. When a logic "0" is forced on this inpiut the transmitter/encoder immediately responds with transmission of "clean status". This function is necessary after the completion of each write type command and in other functions in the 3270 specification. In the logic "1" state the transmitter/encoder transmits data entered on the Data Inputs.

Even/$\overline{\text{Odd}}$ Parity

This input sets the internal logic of the DP8340/NS32440 transmitter/encoder to generate either even or odd parity for the data byte in the bit 12 position. When this pin is in the logic "0" state odd parity is generated. In the logic "1" state even parity is generated. This feature is useful when the control unit is performing a loop back check and at the same time the controller wishes to verify proper data transmission with its receiver/decoder.

Parity Control/Reset

Depending on the type of message transmitted, it is at times necessary in the IBM 3270 specification to generate an additional parity bit in the bit 10 position. The bit generated is odd parity on the previous eight (8) bits of data. When the Parity Control input is in the logic "1" state the data entered at the Data Bit 10 position is placed in the transmitted word. With the Parity Control input in the logic "0" state the Data Bit 10 input is ignored and odd parity on the previous data bits is placed in the normal bit 10 position while overall word parity (bit 12) is even or odd (controlled by Even/$\overline{\text{Odd}}$ Parity input). This eliminates the need for external logic to generate the parity on the data bits.

Truth Table

Parity Control Input	Transmitted Data Bit 10
Logic "1"	Data entered on Data Input 10
Logic "0"	Odd Parity on 8-bit data byte

When this input is driven to a voltage that exceeds the power supply level (9V to 13V) the transmitter/encoder is reset.

Serial Outputs—DATA, $\overline{\text{DATA}}$, and DATA DELAY

These three output pins provide for convenient application of data to the biphase Coax line (see *Figure 15* for application). The Data outputs are a direct bit representation of the biphase data while the DATA DELAY output provides the necessary increment to clearly define the four (4) DC levels of the pulse. The DATA and $\overline{\text{DATA}}$ outputs add flexibility to the DP8340/NS32440 transmitter/encoder for use in high speed differential line driving applications.

Functional Timing Waveforms—Message Format

Single Byte Transmission

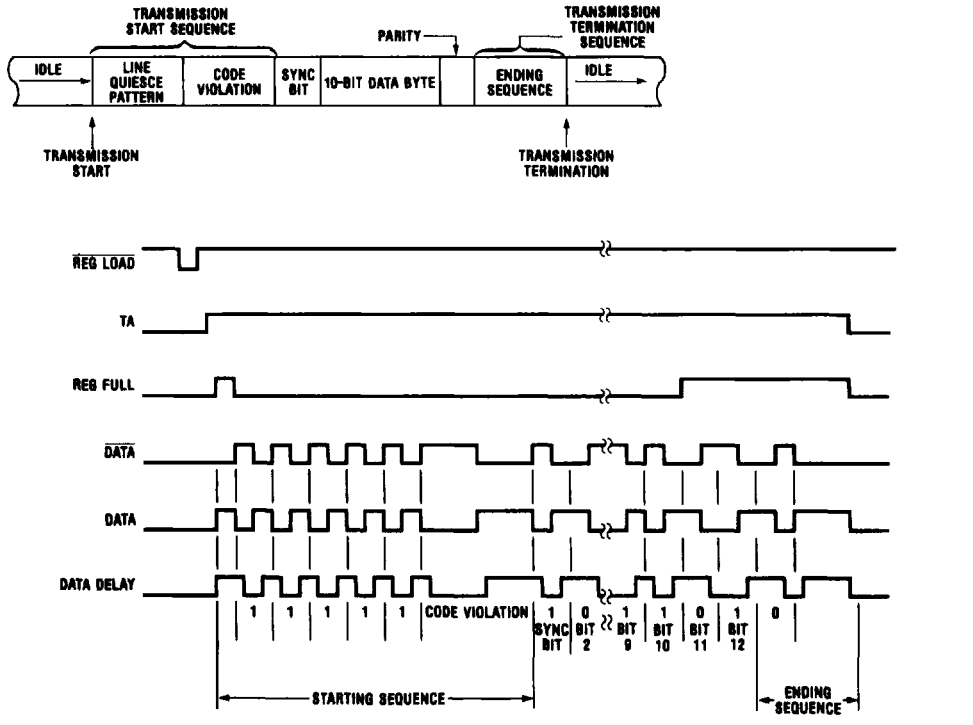

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FIGURE 4. Overall Timing Waveforms for Single Byte

Multi-Byte Transmission

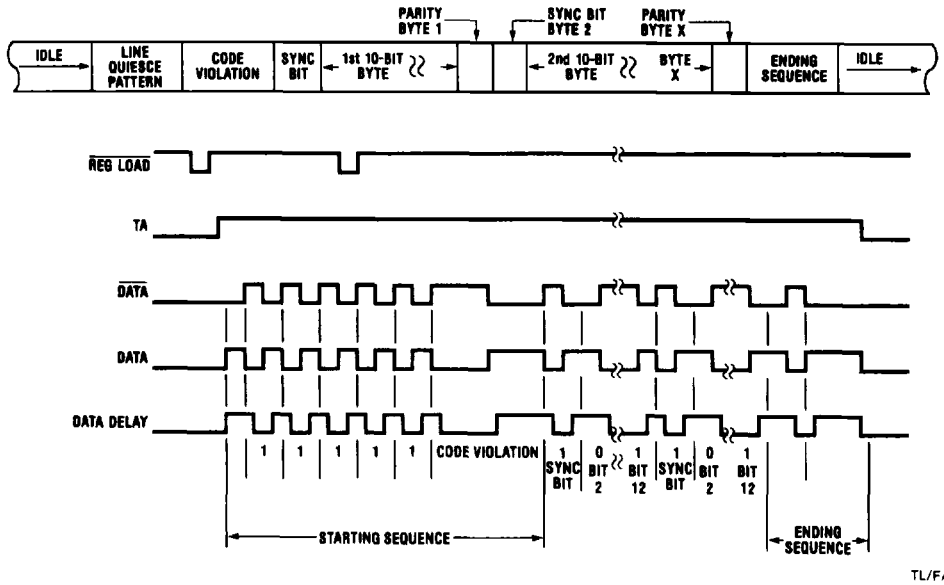

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FIGURE 5. Overall Timing Waveforms for Multi-Byte

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Maximum Power Dissipation @25°C*

Cavity Package	2237 mW
Dual-In-Line Package	2500 mW
Plastic Chip Carrier	1720 mw

*Derate cavity package 14.9 mW/°C above 25°C; derate dual-in-line package 20 mW/°C above 25°C; derate PCC package 13.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Ambient Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage (All Inputs Except X1 and X2)		2.0			V
V_{IL}	Logic "0" Input Voltage (All Inputs Except X1 and X2)				0.8	V
V_{CLAMP}	Input Clamp Voltage (All Inputs Except X1 and X2)	I_{IN} = −12 mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current Register Load Input	V_{CC} = 5.25V, V_{IN} = 5.25V		0.3	120	μA
	All Others Except X1 and X2			0.1	40	μA
I_{IL}	Logic "0" Input Current Register Load Input	V_{CC} = 5.25V, V_{IN} = 0.5V		−15	−300	μA
	All Inputs Except X1 and X2			−5	−100	μA
V_{OH1}	Logic "1" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	I_{OH} = −100 μA	3.2	3.9		V
		I_{OH} = −1 mA	2.5	3.4		V
V_{OH2}	Logic "1" for CKL OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	I_{OH} = −10 mA	2.6	3.0		V
V_{OL1}	Logic "0" All Outputs Except CLK OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	I_{OL} = 5 mA		0.35	0.5	V
V_{OL2}	Logic "0" for CLK OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	I_{OL} = 20 mA		0.4	0.6	V
I_{OS1}	Short Circuit Current for All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	V_{OUT} = 0V (Note 4)	−10	−30	−100	mA
I_{OS2}	Short Circuit Current for DATA, $\overline{DATA}$, and DATA DELAY Outputs	V_{OUT} = 0V (Note 4)	−50	−140	−350	mA
I_{OS3}	Short Circuit Current for CLK OUT	(Note 4)	−30	−90	−200	mA
I_{CC}	Power Supply Current	V_{CC} = 5.25V		170	250	mA

Timing Characteristics Oscillator Frequency = 18.867 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	$\overline{REG\ LOAD}$ to Transmitter Active (T_A) Positive Edge	Load Circuit 1 *Figure 7*		60	90	ns
t_{pd2}	$\overline{REG\ LOAD}$ to REG Full; Positive Edge	Load Circuit 1 *Figure 7*		45	75	ns
t_{pd3}	Register Full to T_A; Negative Edge	Load Circuit 1 *Figure 7*		40	70	ns
t_{pd4}	Positive Edge of $\overline{REG\ LOAD}$ to Positive Edge of DATA	Load Circuits 1 & 2 *Figure 9*		50	80	ns

Timing Characteristics Oscillator Frequency = 18.867 MHz (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd5}	$\overline{\text{REG LOAD}}$ to $\overline{\text{DATA}}$; Positive Edge	Load Circuits 1 & 2 *Figure 9*, (Note 6)		380	475	ns
t_{pd6}	$\overline{\text{REG LOAD}}$ to DATA DELAY; Positive Edge	Load Circuits 1 & 2 *Figure 9*, (Note 6)		160	250	ns
t_{pd7}	Positive Edge of $\overline{\text{DATA}}$ to Negative Edge of DATA DELAY	Load Circuit 2 *Figure 9*, (Note 6)		100	115	ns
t_{pd8}	Positive Edge of DATA DELAY to Negative Edge of $\overline{\text{DATA}}$	Load Circuit 2 *Figure 9*, (Note 6)		110	125	ns
t_{pd9}, t_{pd10}	Skew between DATA and $\overline{\text{DATA}}$	Load Circuit 2 *Figure 9*		2	6	ns
t_{pd11}	Negative Edge of Auto Response to Positive Edge of TA	Load Circuit 1 *Figure 10*		70	110	ns
t_{pd12}	Maximum Time Delay to Load Second Byte after Positive Edge of REG FULL	Load Circuit 1 *Figure 8*, (Note 6)			$4 \times T - 50$	ns
t_{pd13}	X1 to CLK OUT; Positive Edge	Load Circuit 2 *Figure 13*		21	30	ns
t_{pd14}	X1 to CLK OUT; Negative Edge	Load Circuit 2 *Figure 13*		23	33	ns
t_{pd15}	Negative Edge of AR to Positive Edge of REG FULL	Load Circuit 1 *Figure 10*		45	75	ns
t_{pd16}	Skew between TA and REG FULL during Auto Response	Load Circuit 1 *Figure 10*		50	80	ns
t_{pd17}	$\overline{\text{REG LOAD}}$ to REG FULL; Positive Edge for Second Byte	Load Circuit 1 *Figure 14*		45	75	ns
t_{pw1}	$\overline{\text{REG LOAD}}$ Pulse Width	*Figure 12*	40			ns
t_{pw2}	First REG FULL Pulse Width (Note 5)	Load Circuit 1 *Figure 7*, (Note 6)		$8 \times T + 60$	$8 \times T + 100$	ns
t_{pw3}	REG FULL Pulse Width prior to Ending Sequence (Note 5)	Load Circuit 1, *Figure 7*, (Note 6)		$5 \times B$		ns
t_{pw4}	Pulse Width for Auto Response	*Figure 10*	40			ns
t_S	Data Setup Time prior to REG LOAD Positive Edge, Hold Time (t_H) = 0 ns	*Figure 12*		15	25	ns
t_{r1}	Rise Time for DATA, $\overline{\text{DATA}}$, and DATA DELAY Output Waveform	Load Circuit 2 *Figure 11*		7	13	ns
t_{f1}	Fall Time for DATA, $\overline{\text{DATA}}$, and DATA DELAY Output Waveform	Load Circuit 2 *Figure 11*		5	11	ns
t_{r2}	Rise Time for TA and REG FULL	Load Circuit 1 *Figure 15*		20	30	ns
t_{f2}	Fall Time for TA and REG FULL	Load Circuit 1 *Figure 15*		15	25	ns
f_{MAX}	Data Rate Frequency (Clock Input must be 8X this Frequency)	(Note 7)	DC		3.5	Mbits/s

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute basis.

Note 4: Only one output should be shorted at a time. Output should not be shorted for more than one second at a time.

Note 5: T = 1/(Oscillator Frequency), unit for T should be ns. B = 8T

Note 6: Oscillator Frequency Dependent.

Note 7: For the IBM 3270 Interface, the data rate frequency is 2.358 Mbits/s. 28 MHz clock frequency corresponds to 3.75% jitter when referenced to *Figure 10* of DP8341 Datasheet.

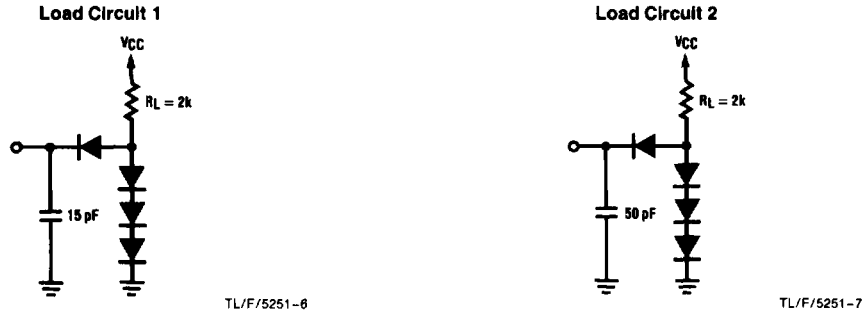

FIGURE 6. Test Load Circuits

Timing Waveforms

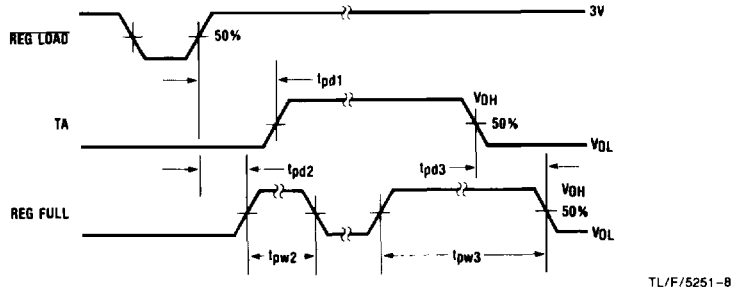

FIGURE 7. Timing Waveforms for Single Byte Transfer

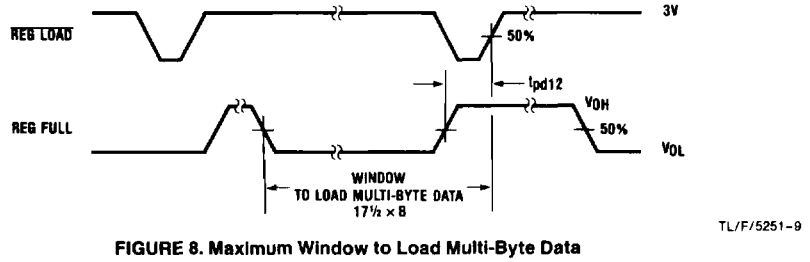

FIGURE 8. Maximum Window to Load Multi-Byte Data

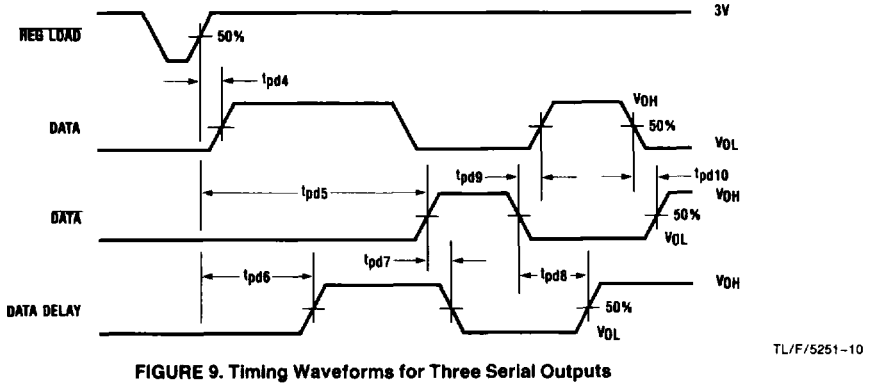

FIGURE 9. Timing Waveforms for Three Serial Outputs

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Timing Waveforms (Continued)

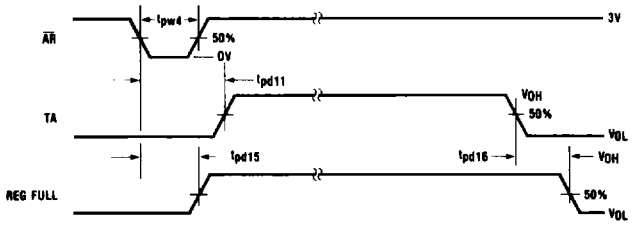

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FIGURE 10. Timing Waveforms for Auto-Response

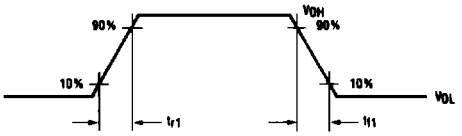

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FIGURE 11. Output Waveform for DATA, DATA, DATA DELAY (Load Circuit 2)

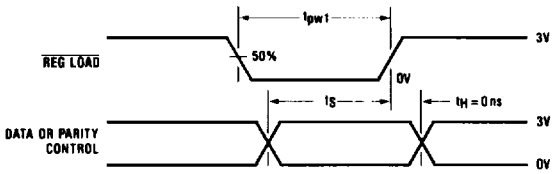

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FIGURE 12. Register Load Waveform Requirement

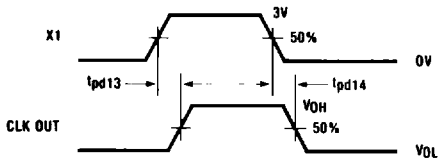

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FIGURE 13. Timing Waveforms for Clock Pulse

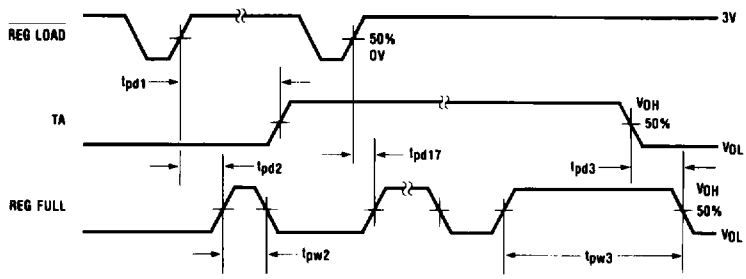

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FIGURE 14. Timing Waveforms for Two Byte Transfer

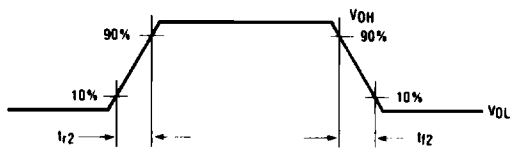

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FIGURE 15. Rise and Fall Time Measurement for TA and REG Full

Typical Applications

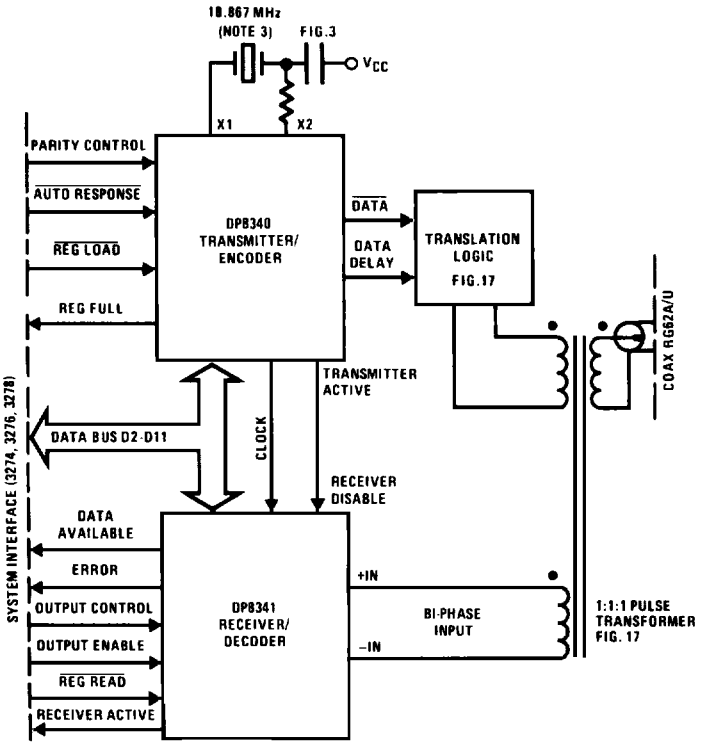

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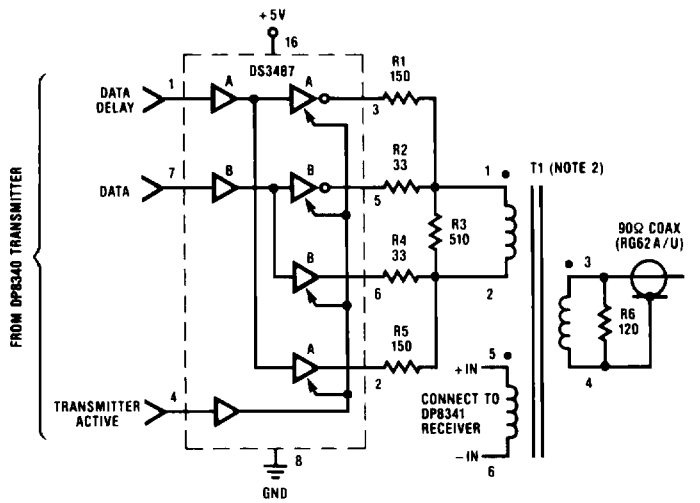
FIGURE 16. Typical Applications for IBM 3270 Interface



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Note 1: Resistance values are in Ω, ±5%, ¼ W

Note 2: T1 is a 1:1:1 pulse transformer, L_{MIN} = 500 μH for 18 MHz system clock. Pulse Engineering Part No. 5762/Surface Mount, 5762M/PE-85762. Technitrol Part No. 11LHA, Valor Electronics Part No. CT1501 or equivalent transformers.

Note 3: Crystal manufacturer's Midland Ross Corp. NEL Unit Part No. NE-18A (C2560N) @ 18.867 MHz and the Viking Group of San Jose, CA Part No. VXB46NS @ 18.867 MHz.

FIGURE 17. Translation Logic