

# SN75ALS1711 TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS117B – APRIL 1991 – REVISED MAY 1995

- Three Bidirectional Transceivers
- Driver/Receiver Meets or Exceeds the Requirements of ANSI Standard RS-485 and ANSI Standard X3.131-1986 (SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Wide Positive and Negative Input/Output Bus Voltages Ranges . . .  $-7\text{ V}$  to  $12\text{ V}$
- Driver Output Capacity . . .  $\pm 60\text{ mA}$
- Driver Positive and Negative Current Limiting
- Thermal Shutdown Protection
- Receiver Input Sensitivity . . .  $\pm 200\text{ mV Max}$
- Receiver Input Impedance . . .  $12\text{ k}\Omega\text{ Min}$
- Receiver Input Hysteresis . . .  $50\text{ mV Typ}$
- Operates From a Single 5-V Supply
- Low Supply-Current Requirements  
72 mA Max
- Glitch-Free Power-up and Power-Down Protection

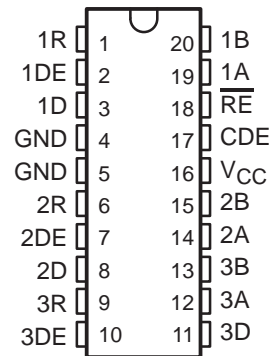
## description

The SN75ALS1711 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets ANSI Standard RS-485 and ANSI Standard X3.131-1986 (SCSI).

The SN75ALS1711 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC}$  is at 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS1711 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**DW OR N PACKAGE  
(TOP VIEW)**



## Function Tables

**EACH DRIVER**

INPUT D	ENABLES		OUTPUTS	
	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

**EACH RECEIVER**

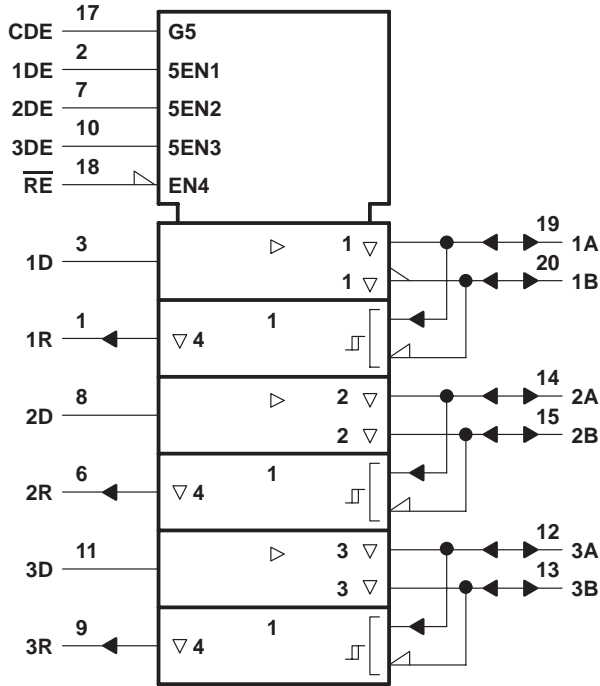
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{\text{RE}}$	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$V_{ID} = -0.2\text{ V to } 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open	L	H

H = high level, L = low-level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

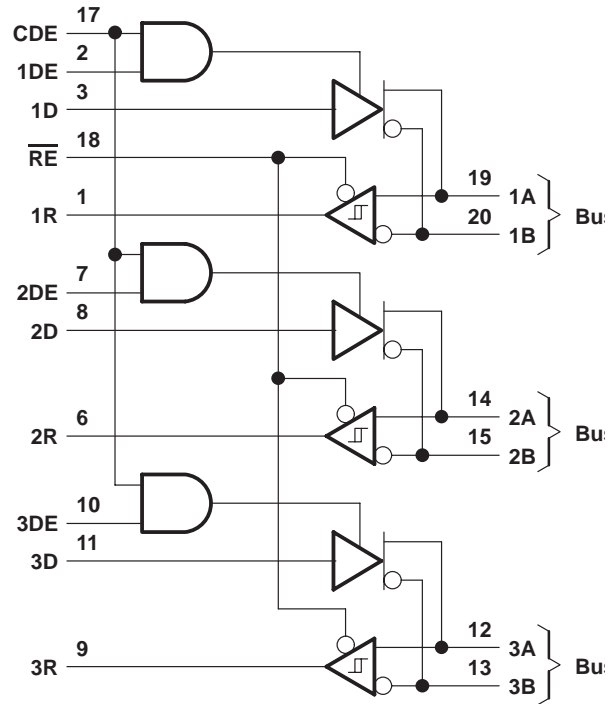
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## logic symbol†

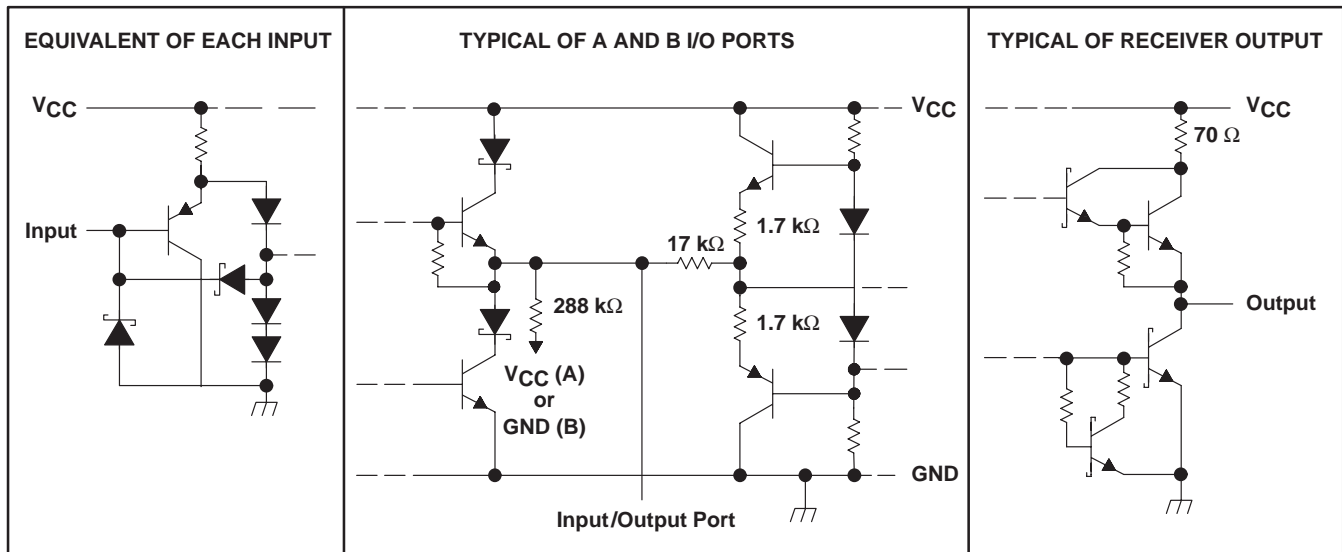


## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematics of inputs and outputs



All values are nominal.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Enable input voltage range, $V_I$	–0.5 V to $V_{CC} + 0.5$ V
Input voltage range, $V_I$ : Driver	–0.5 V to $V_{CC} + 0.5$ V
Receiver	–9 V to 14 V
Output voltage range, $V_O$ : Driver	–9 V to 14 V
Receiver	–0.5 V to $V_{CC} + 0.5$ V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

## recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Common-mode input voltage at any bus terminal, $V_{IC}$ (see Note 2)		–7‡		12	V
High-level input voltage, $V_{IH}$	D, DE, $\overline{RE}$ , CDE	2			V
Low-level input voltage, $V_{IL}$	D, DE, $\overline{RE}$ , CDE			0.8	V
High-level output current, $I_{OH}$	Driver			–60	mA
	Receiver			–400	μA
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	
Operating free-air temperature, $T_A$		0		70	°C

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

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## TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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### DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA			-1.5	V	
V <sub>O</sub>	Output voltage	I <sub>O</sub> = 0	0		6	V	
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0	1.5		5	V	
V <sub>OD2</sub>	Differential output voltage	R <sub>L</sub> = 54 Ω, See Figure 1	1.5		5	V	
V <sub>OD3</sub>	Differential output voltage	See Note 3 and Figure 2	1.5		5	V	
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage‡	R <sub>L</sub> = 54 Ω, See Figure 1			±0.2	V	
V <sub>OC</sub>	Common-mode output voltage	R <sub>L</sub> = 54 Ω, See Figure 1			3 -1	V	
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage‡	R <sub>L</sub> = 54 Ω, See Figure 1			±0.2	V	
I <sub>OZ</sub>	High-impedance state output current	Output disabled, V <sub>CC</sub> = 5.25 V	V <sub>O</sub> = 12 V		1	mA	
			V <sub>O</sub> = 7 V		-0.8		
I <sub>IH</sub>	High-level input current, DE, EN, CDE	V <sub>IH</sub> = 2.4 V			20	μA	
I <sub>IL</sub>	Low-level input current, DE, EN, CDE	V <sub>IL</sub> = 0.4 V			-200	μA	
I <sub>OS</sub>	Short-circuit output current	V <sub>O</sub> = 12 V			-250	mA	
		V <sub>O</sub> = 7 V			250		
I <sub>CC</sub>	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

‡ Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

### switching characteristics, V<sub>CC</sub> = 5 V ± 5%, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>PLH</sub>	Differential propagation delay time, low- to high-level output	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 100 pF, See Figure 3	8	13	22	ns	
t <sub>PHL</sub>	Differential propagation delay time, high- to low-level output		8	15	22		
t <sub>PZH</sub>	Output enable time to high level	R <sub>L</sub> = 110 Ω, See Figure 4	S1 open, S2 closed	30	50	60	ns
t <sub>PHZ</sub>	Output disable time from high level			4	16	30	
t <sub>PZL</sub>	Output enable time to low level		S1 closed, S2 open	16	26	45	
t <sub>PLZ</sub>	Output disable time from low level			4	8	20	



## RECEIVER SECTION

**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$ , $I_O = -0.4\text{ mA}$			0.2	V
$V_{IT-}$	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$ , $I_O = 4\text{ mA}$	$-0.2\ddagger$			V
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			50		mV
$V_{IK}$	Input clamp voltage, $\overline{RE}$	$I_I = 18\text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$I_{OH} = -0.4\text{ mA}$	2.4			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$			0.5	V
$I_{OZ}$	High-impedance-state output current	$V_{CC} = 5.25\text{ V}$ , $V_O = 0.4\text{ V to } 2.4\text{ V}$			$\pm 20$	$\mu\text{A}$
$I_I$	Line input current	Other input at 0, See Note 3			1	mA
			$V_I = 12\text{ V}$		-0.8	
$I_{IH}$	High-level input current, $\overline{RE}$	$V_{IH} = 2.4\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current, $\overline{RE}$	$V_{IL} = 0.4\text{ V}$			-200	$\mu\text{A}$
$r_i$	Input resistance		12			k $\Omega$
$I_{OS}$	Short-circuit output current $\S$	$V_O = 0$	-15		-130	mA
$I_{CC}$	Supply current	No load	Outputs enabled	48	72	mA
			Outputs disabled	30	48	

† All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Not more than one output should be shorted at one time.

NOTE 3: This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

### switching characteristics, $V_{CC} = 5\text{ V} \pm 5\%$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figures 5 and 6	13	20	37	ns
$t_{PHL}$	Propagation delay time, high- to low-level output		13	20	37	
$t_{PZH}$	Output enable time to high level	See Figures 5 and 7	3	9	20	ns
$t_{PHZ}$	Output disable time from high level					
$t_{PZL}$	Output enable time to low level		5	10	20	
$t_{PZL}$	Output enable time to low level					

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## PARAMETER MEASUREMENT INFORMATION

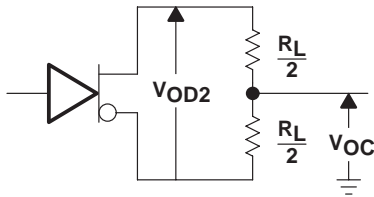


Figure 1. Driver  $V_{OD2}$  and  $V_{OC}$

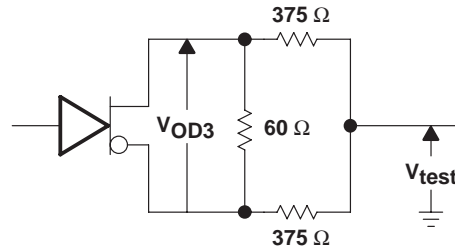


Figure 2. Driver  $V_{OD3}$

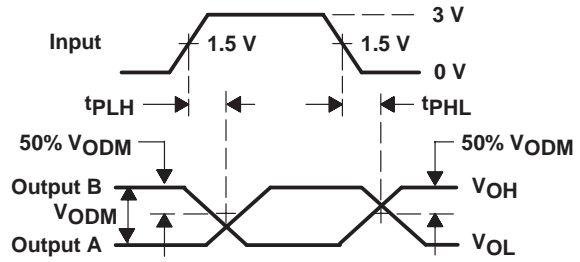
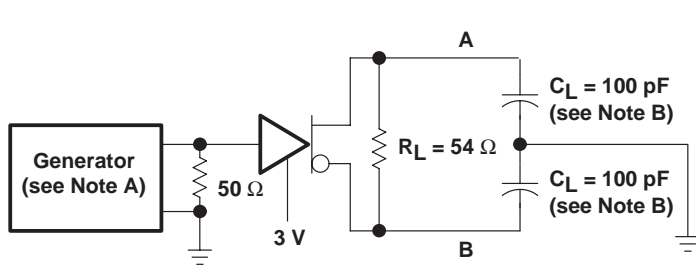
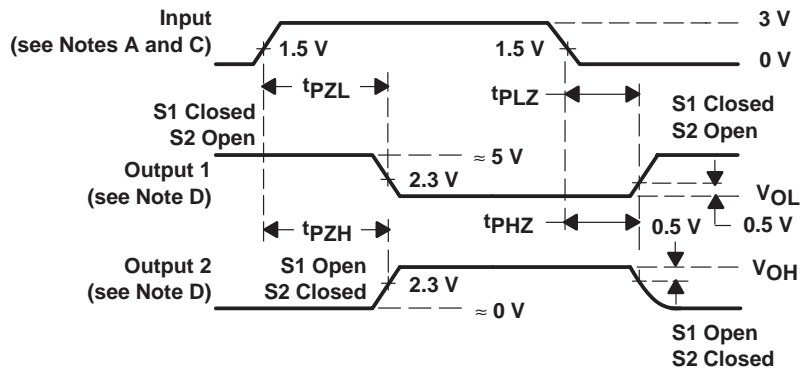
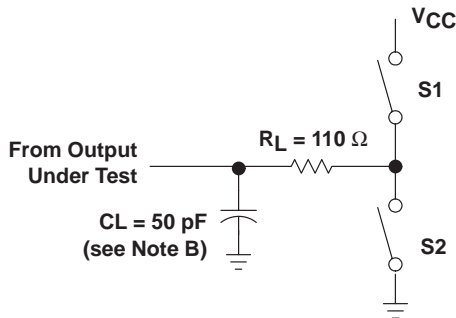


Figure 3. Driver Propagation Delay Times



- NOTES: A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. Each enable is tested separately.  
 D. Output 1 and output 2 are outputs with internal conditions such that the output is low or high except when disabled by the output control.

Figure 4. Driver Enable/Disable Times

PARAMETER MEASUREMENT INFORMATION

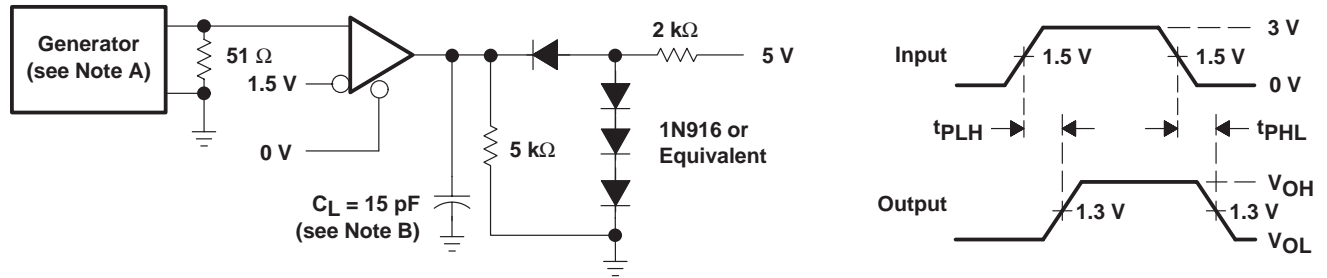
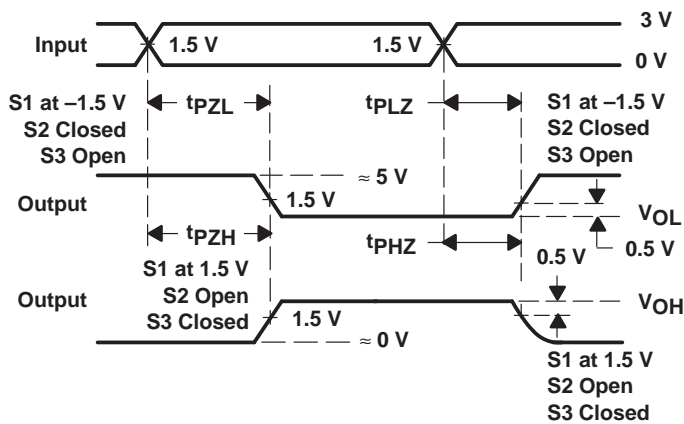
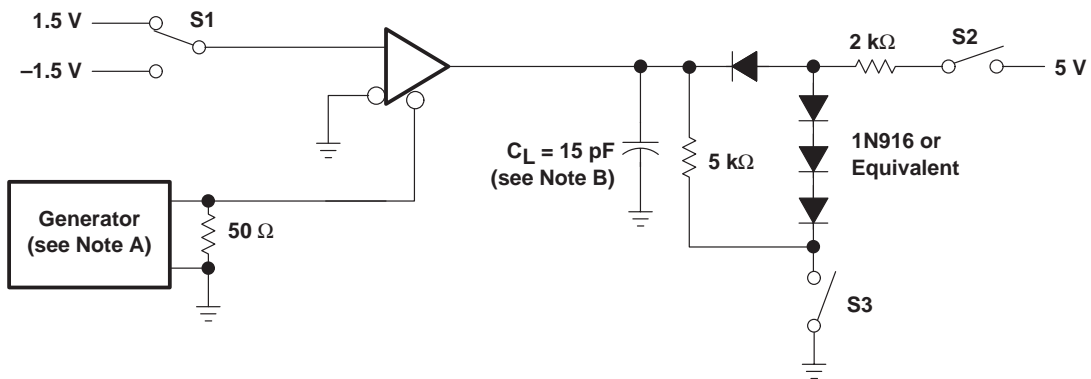


Figure 5. Receiver Propagation Delay Times



NOTES: A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 6. Receiver Enable/Disable Times

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75ALS1711N	OBSOLETE	PDIP	N	20		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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