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T-45-07-00

National Semiconductor

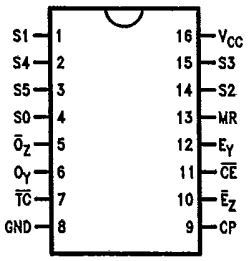
5497/DM7497
Synchronous Modulo-64 Bit Rate Multiplier

General Description

The '97 contains a synchronous 6-stage binary counter and six decoding gates that serve to gate the clock through to the output at a sub-multiple of the input frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S0–S5) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. An asynchronous Master Reset input prevents counting and resets the counter.

Connection Diagram

Dual-In-Line Package



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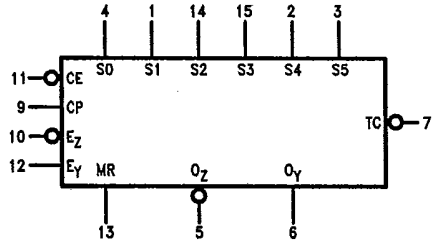
Order Number 5497DMQB, 5497FMQB or DM7497N
See NS Package Number J16A, N16E or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S0–S5	Rate Select Inputs
$\overline{E}_Z$	$\overline{O}_Z$ Enable Input (Active LOW)
E_Y	O_Y Enable Input
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{O}_Z$	Gated Clock Output (Active LOW)
O_Y	Complement Output (Active HIGH)
$\overline{TC}$	Terminal Count Output (Active LOW)

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutual device operation.*

Recommended Operating Conditions

Symbol	Parameter	5497			DM7497			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(L)$	Setup Time LOW, $\overline{CE}$ to CP Rising	25			25			ns
$t_h(H)$	Hold Time HIGH, $\overline{CE}$ to CP Rising	0			0			ns
$t_h(L)$	Hold Time LOW, $\overline{CE}$ to CP Falling	0			0			ns
$t_w(H)$	CP Pulse Width HIGH	20			20			ns
$t_w(L)$	CP Pulse Width LOW	20						ns
$t_w(H)$	MR Pulse Width HIGH	15			15			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V Clock Inputs	DM74			40	µA
			54			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Clock Inputs	DM74			−1.6	mA
			54			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current With Outputs High	V_{CC} = Max				120	mA

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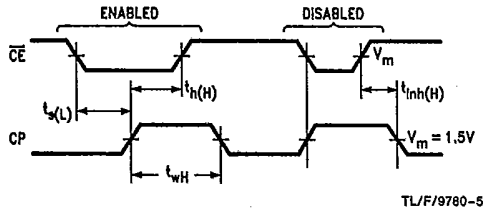
Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	5497 C_L = 15 pF, R_L = 400Ω		DM7497 C_L = 15 pF, R_L = 400Ω		Units
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	25		25		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to $\overline{O}_Z$		18 23		18 23	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to O_Y		30 33		30 33	ns
t_{PLH} t_{PHL}	Propagation Delay E_Y to O_Y		14 10		14 10	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to O_Y		23 23		23 23	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{O}_Z$		14 14		14 14	ns
t_{PLH} t_{PHL}	Propagation Delay CP to O_Y		39 30		39 30	ns
t_{PLH} t_{PHL}	Propagation Delay CP to O_Z		18 26		18 26	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		35 33		30 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{TC}$		25 21		20 21	ns
t_{PLH}	Propagation Delay MR to O_Y		43		36	ns
t_{PHL}	Propagation Delay MR to $\overline{O}_Z$		34		23	ns

Timing Diagrams



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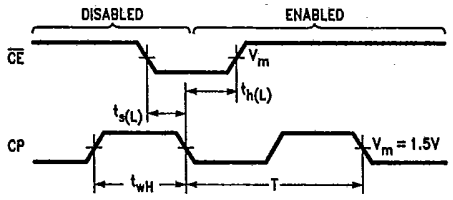

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Functional Description

The '97 contains six JK flip-flops connected as a synchronous modulo-64 binary counter. A LOW signal on the Count Enable ($\overline{CE}$) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (63), with all Qs HIGH, the Terminal Count ($\overline{TC}$) output will be LOW if $\overline{CE}$ is LOW. A HIGH signal on Master Reset (MR) resets the flip-flops and prevents counting, although output pulses can still occur if the clock is running, $\overline{E}_Z$ is LOW and S5 is HIGH.

The flip-flop outputs are decoded by a 6-wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted CP and Z-enable ($\overline{E}_Z$) functions, as well as one of the Select (S0–S5) inputs. The Z output, $\overline{O}_Z$ is normally HIGH and goes LOW when CP and $\overline{E}_Z$ are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled by the counter at different times and different rates relative to the clock. For example, the gate to which S5 is connected is enabled during every other clock period, assuming S5 is HIGH. Thus, during one complete cycle of the counter (64 clocks) the S5 gate is enabled 32 times and can therefore gate 32 clocks per cycle to the output. The S4 gate is enabled 16 times per cycle, the S3 gate 8 times per cycle, etc. The output pulse rate thus depends on the clock rate and which of the S0–S5 inputs is HIGH.

$$f_{out} = \frac{m}{64} \bullet f_{in}$$

Where: $m = S5 \bullet 2^5 + S4 \bullet 2^4 + S3 \bullet 2_3 + S2 \bullet 2^2 + S1 \bullet 2^1 + S0 \bullet 2^0$

Thus by appropriate choice of signals applied to the S0–S5 inputs, the output pulse rate can range from $1/64$ to $63/64$ of the clock rate, as suggested in Rate Select Table. There is no output pulse when the counter is in the "all ones" condition. When m is 1, 2, 4, 8, 16 or 32, the output pulses are evenly spaced, assuming that the clock frequency is constant. For any other value of m the output pulses are not evenly spaced, since the pulse train is formed by interleaving pulses passed by two or more of the AND gates. The Pulse Pattern Table indicates the output pattern for several values of m. In each row, a one means that the $\overline{O}_Z$ output will be HIGH during that entire clock period, while a zero means that $\overline{O}_Z$ will be LOW when the clock is LOW in that period. The first column in the output field coincides with the "all zeroes" condition of the counter, while the last column represents the "all ones" condition. The pulse pattern for any particular value of m can be deduced by factoring it into the sum of appropriate powers of two (e.g. $19 = 16 + 2 + 1$) and combining the pulses (i.e., the zeroes) shown for each for the relevant powers of two (e.g. for $m = 16$, 2 and 1).

The Y output O_Y is the complement of $\overline{O}_Z$ and is thus normally LOW. A LOW signal on the Y-enable input, E_Y, disables O_Y. To expand the multiplier to 12-bit rate select, two packages can be cascaded as shown in *Figure A*. Both circuits operate from the basic clock, with the $\overline{TC}$ output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only $1/64$ the rate of the first and a full cycle of the two counters combined requires 4096 clocks. Each rate select input of the first package has 64 times the weight of its counterpart in the second package.

$$f_{out} = \frac{m_1 + m_2}{64 \bullet 64} \bullet f_{in}$$

Where: $m_1 = S5 \bullet 2^{11} + S4 \bullet 2^{10} + S3 \bullet 2^9 + S2 \bullet 2^8 + S1 \bullet 2^7 + S0 \bullet 2^6$ (first package)

$m_2 = S5 \bullet 2^5 + S4 \bullet 2^4 + S3 \bullet 2^3 + S2 \bullet 2_2 + S1 \bullet 2^1 + S0 \bullet 2^0$ (second package)

Combined output pulses are obtained in *Figure A* by letting the Z output of the first circuit act as the Y-enable function for the second, with the interleaved pulses obtained from the Y output of the second package being opposite in phase to the clock.

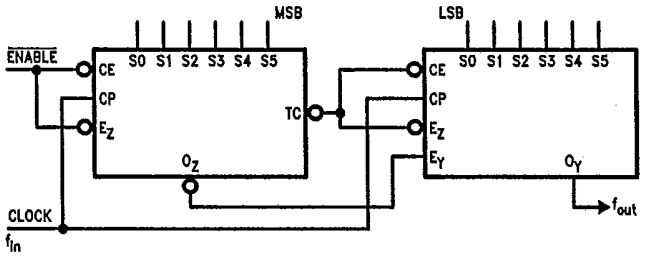

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FIGURE A. Cascading for 12-Bit Rate Select

Functional Description (Continued)

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Mode and Rate Select Table (Note 1)

Inputs									Clock Pulses	Outputs				Notes
MR	$\overline{CE}$	$\overline{E}_Z$	S5	S4	S3	S2	S1	S0		E_Y	O_Y	O_Z	$\overline{TC}$	
H	X	H	X	X	X	X	X	X	X	H	L	H	H	2
L	L	L	L	L	L	L	L	L	64	H	L	H	1	3
L	L	L	L	L	L	L	L	H	64	H	1	1	1	3
L	L	L	L	L	L	L	H	L	64	H	2	2	1	3
L	L	L	L	L	L	H	L	L	64	H	4	4	1	3
L	L	L	L	L	H	L	L	L	64	H	8	8	1	3
L	L	L	L	H	L	L	L	L	64	H	16	16	1	3
L	L	L	H	L	L	L	L	L	64	H	32	32	1	3
L	L	L	H	H	H	H	H	H	64	H	63	62	1	3
L	L	L	H	H	H	H	H	H	64	L	H	63	1	4
L	L	L	H	L	L	L	L	L	64	H	40	40	1	5

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Note 1: Numerals indicate number of pulses per cycle.

Note 2: This is a simplified illustration of the clear function. CP and $\overline{E}_Z$ also affect the logic level of O_Y and $\overline{O}_Z$. A LOW signal on E_Y will cause O_Y to remain HIGH.

Note 3: Each rate illustrated assumes S0–S5 are constant throughout the cycle; however, these illustrations in no way prohibit variable-rate operation.

Note 4: E_Y is used to inhibit output Y.

Note 5: $f_{out} = m \bullet \frac{f_{in}}{64} = \frac{(32 + 8)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

Pulse Pattern Table

m	Output Pulse Pattern at $\overline{O}_Z$
1	11111111111111111111111111111110111111111111111111111111111111
2	11111111111111101111111111111111111111111111111111101111111111111
3	11111111111111101111111111111111101111111111111111101111111111111
4	11111110111111111111111101111111111111111011111111111111101111111
5	11111110111111111111111101111111011111110111111111111111101111111
6	11111110111111101111111011111111111111110111111101111111011111111
8	11101111111011111110111111101111111011111110111111101111110111111
10	11101111111011111110111111101111111011111110111101110111011111101111
12	11101110111011111110111011101111111011101110111111110111011101111
14	11101110111011101110111011101111111011101110111011101110111011101111
16	10111011101110111011101110111011101110111011101110111011101110111011
20	10111010101110111011101010111011101110101011101110111011101110111011
24	10101011101010111010101110101011111010111010101110101011101010111011
28	10101010101010111010101010101011101010101010101110101010101010111011
32	010101... ...0101

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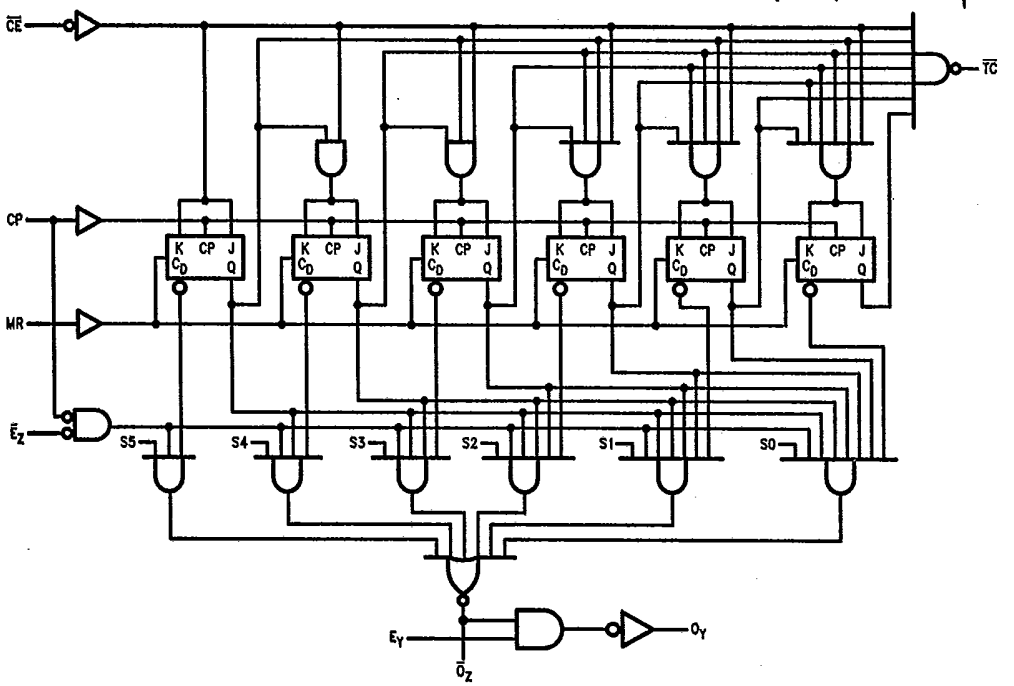
Logic Diagram



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