

TLV2432, TLV2432A, TLV2434, TLV2434A Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

SLOS168F – NOVEMBER 1996 – REVISED MARCH 2001

- Output Swing Includes Both Supply Rails
- Extended Common-Mode Input Voltage Range . . . 0 V to 4.5 V (Min) with 5-V Single Supply
- No Phase Inversion
- Low Noise . . . 18 nV/√Hz Typ at f = 1 kHz
- Low Input Offset Voltage
950 μV Max at T_A = 25°C (TLV243xA)
- Low Input Bias Current . . . 1 pA Typ
- Very Low Supply Current . . . 125 μA Per Channel Max
- 600-Ω Output Drive
- Macromodel Included
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

description

The TLV243x and TLV243xA are low-voltage operational amplifier from Texas Instruments. The common-mode input voltage range for each device is extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. The TLV243x only requires 100 μA (typ) of supply current per channel, making it ideal for battery-powered applications. The TLV243x also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecom applications.

The other members in the TLV243x family are the high-power, TLV244x, and micro-power, TLV2422, versions.

The TLV243x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV243xA is available and has a maximum input offset voltage of 950 μV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

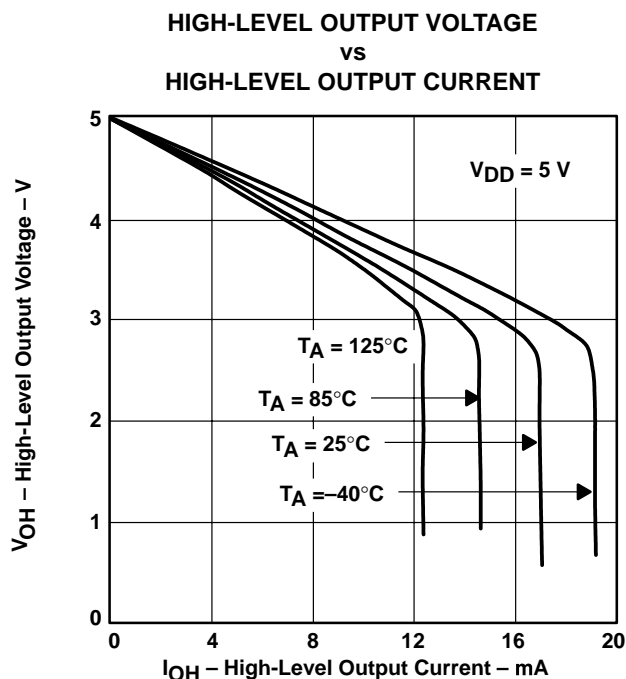


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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TLV2432 and TLV2432A AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	2.5 mV	TLV2432CD	—	—	TLV2432CPW	—
–40°C to 85°C	950 μV 2.5 mV	TLV2432AID TLV2432ID	— —	— —	TLV2432AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLV2432AQD TLV2432QD	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLV2432AMFK TLV2432MFK	TLV2432AMJG TLV2432MJG	— —	TLV2432AMU TLV2432MU

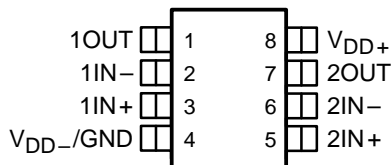
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2432CDR). The PW package is available only left-end taped and reeled.

TLV2434 AVAILABLE OPTIONS

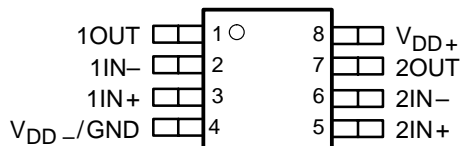
T _A	V _{IO} max AT 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
0°C to 70°C	2.5 mV	TLV2434CD	TLV2434CPW
–40°C to 125°C	950 μV 2.5 mV	TLV2434AID TLV2434ID	TLV2434AIPW TLV2434IPW

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2434CDR). The PW package is available only left-end taped and reeled.

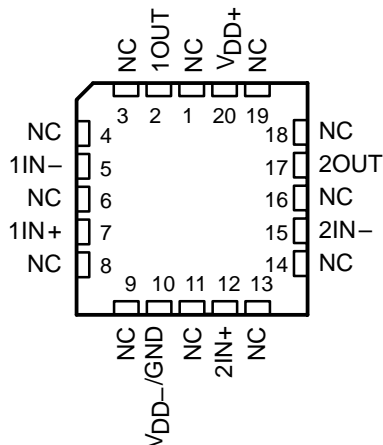
**TLV2432
D OR JG PACKAGE
(TOP VIEW)**



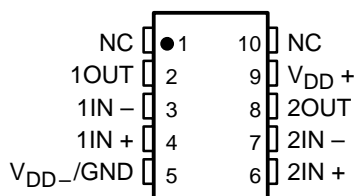
**TLV2432
PW PACKAGE
(TOP VIEW)**



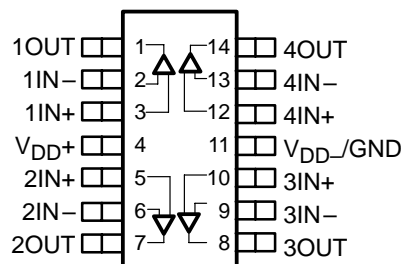
**TLV2432
FK PACKAGE
(TOP VIEW)**



**TLV2432
U PACKAGE
(TOP VIEW)**



**TLV2434
D OR PW PACKAGE
(TOP VIEW)**



NC – No internal connection

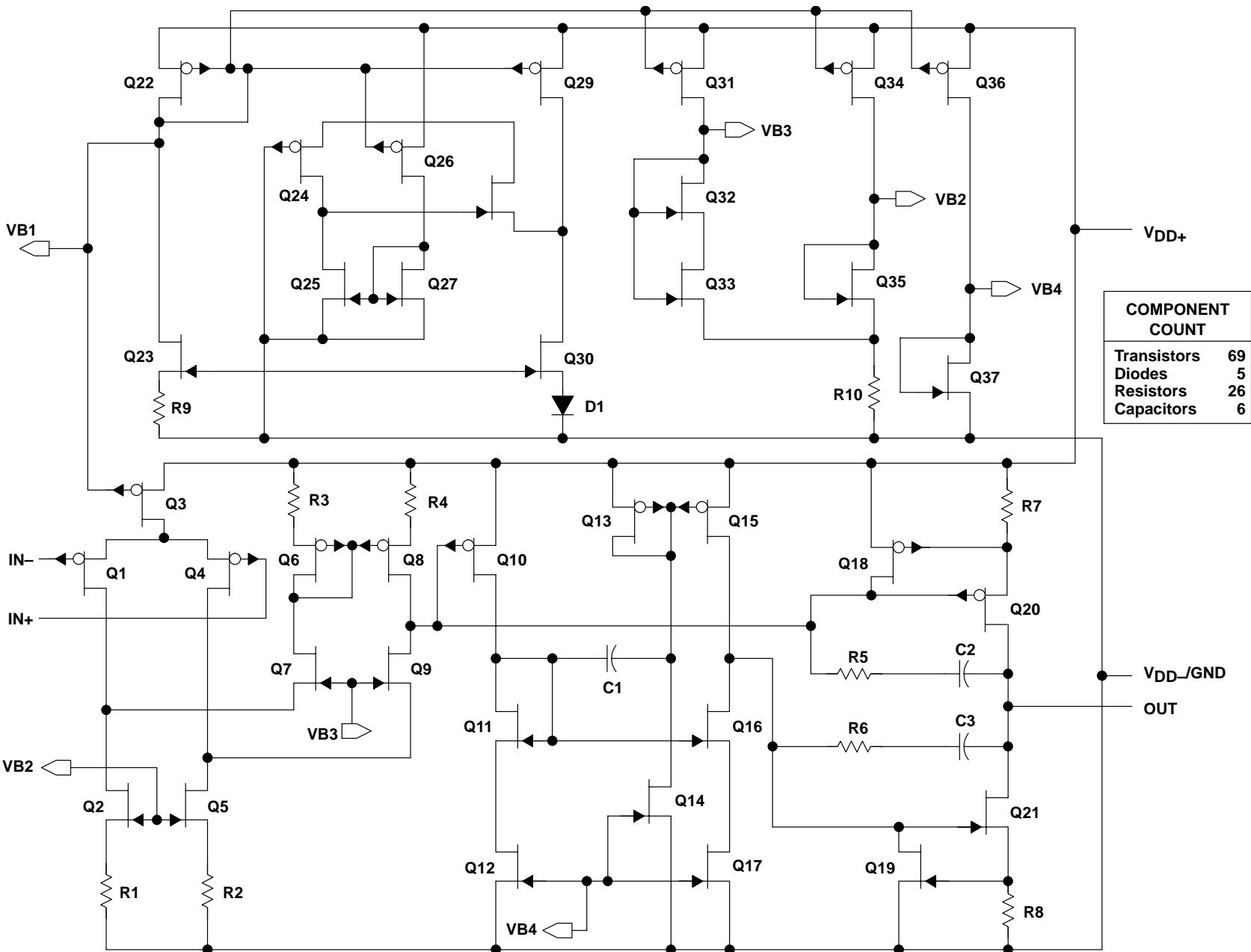


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equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage, V_I (any input, see Note 1): C and I suffix	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix (dual)	-40°C to 85°C
I suffix (quad)	-40°C to 125°C
Q suffix	-40°C to 125°C
M suffix	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14)	1022 mW	7.6 mW/°C	900 mW	777 mW	450 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW (8)	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW (14)	720 mW	5.6 mW/°C	634 mW	547 mW	317 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 0.8$	V_{DD-}	$V_{DD+} - 0.8$	V_{DD-}	$V_{DD+} - 0.8$	V_{DD-}	$V_{DD+} - 0.8$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	125	-40	125	-55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A^\dagger	TLV243x			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm \pm 1.5\text{ V},$ $R_S = 50\ \Omega$	TLV243xC, TLV243xI	25°C	300	2000	μV	
			Full range	2500			
		TLV243xAI	25°C	300	950		
			Full range	1500			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm \pm 1.5\text{ V},$ $R_S = 50\ \Omega$		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current			25°C	0.5	60	pA	
			Full range	150			
I_{IB} Input bias current			25°C	1	60	pA	
			Full range	150			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV},$ $R_S = 50\ \Omega$		25°C	0 to 2.5	-0.25 to 2.75	V	
			Full range	0 to 2.2			
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$		25°C	2.98		V	
			25°C	$I_{OH} = -3\text{ mA}$	2.5		
					Full range		2.25
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$		25°C	0.02		V	
			25°C	0.83			
	$V_{IC} = 1.5\text{ V},$ $I_{OL} = 3\text{ mA}$	Full range	1				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }2\text{ V}$	$R_L = 2\text{ k}\Omega^\ddagger$	25°C	1.5	2.5	V/mV	
			Full range	1			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	750			
$r_{i(d)}$ Differential input resistance			25°C	1000		$\text{G}\Omega$	
$r_{i(c)}$ Common-mode input resistance			25°C	1000		$\text{G}\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$		25°C	8		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$		25°C	130		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.5\text{ V},$ $V_O = 1.5\text{ V},$ $R_S = 50\ \Omega$		25°C	70	83	dB	
			Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load		25°C	80	95	dB	
			Full range	80			
I_{DD} Supply current (per channel)	$V_O = 1.5\text{ V},$ No load		25°C	98	125	μA	
			Full range	125			

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is -40°C to 85°C. Full range for the quad I suffix is -40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV243x			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }2\text{ V}$, $C_L = 100\text{ pF}‡$	$R_L = 2\text{ k}\Omega‡$	25°C	0.15	0.25	V/ μs
			Full range	0.1		
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C	120		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		25°C	22		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C	2.7		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C	4		
I_n Equivalent input noise current			25°C	0.6		fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 1\text{ kHz}$, $R_L = 2\text{ k}\Omega‡$	$A_V = 1$	25°C	0.065%		
		$A_V = 10$		0.5%		
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}‡$	$R_L = 2\text{ k}\Omega‡$	25°C	0.5		MHz
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $R_L = 2\text{ k}\Omega‡$	$A_V = 1$, $C_L = 100\text{ pF}‡$	25°C	220		kHz
t_s Settling time	$A_V = -1$, Step = 0.5 V to 2.5 V, $R_L = 2\text{ k}\Omega‡$, $C_L = 100\text{ pF}‡$	To 0.1%	25°C	6.4		μs
		To 0.01%		14.1		
ϕ_m Phase margin at unity gain	$R_L = 2\text{ k}\Omega‡$	$C_L = 100\text{ pF}‡$	25°C	62°		
Gain margin			25°C	11		

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is –40°C to 85°C. Full range for the quad I suffix is –40°C to 125°C.

‡ Referenced to 2.5 V



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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A †	TLV243xQ, TLV243xM			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 1.5\text{ V},$ $R_S = 50\ \Omega$	TLV243xQ, TLV243xM	25°C	300	2000	μV	
			Full range	2500			
		TLV243xAQ, TLV243xAM	25°C	300	950		
			Full range	2000			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 1.5\text{ V},$ $R_S = 50\ \Omega$		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current			25°C	0.5	60	pA	
			Full range	150			
I_{IB} Input bias current			25°C	1	60	pA	
			Full range	300			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV},$ $R_S = 50\ \Omega$		25°C	0 to 2.5	-0.25 to 2.75	V	
			Full range	0 to 2.2			
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$		25°C	2.98		V	
			25°C	2.5			
			Full range	2.25			
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$		25°C	0.02		V	
			25°C	0.83			
	$V_{IC} = 1.5\text{ V},$ $I_{OL} = 3\text{ mA}$	Full range	1				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }2\text{ V}$	$R_L = 2\text{ k}\Omega$ ‡	25°C	1.5	2.5	V/mV	
		$R_L = 1\text{ M}\Omega$ ‡	Full range	0.5			
			25°C	750			
$r_{i(d)}$ Differential input resistance			25°C	1000		$\text{G}\Omega$	
$r_{i(c)}$ Common-mode input resistance			25°C	1000		$\text{G}\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$		25°C	8		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$		25°C	130		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.5\text{ V},$ $V_O = 1.5\text{ V},$ $R_S = 50\ \Omega$		25°C	70	83	dB	
			Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load		25°C	80	95	dB	
			Full range	80			
I_{DD} Supply current	$V_O = 1.5\text{ V},$ No load		25°C	195	250	μA	
			Full range	260			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV243xQ, TLV243xM, TLV243xAQ, TLV243xAM			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }2\text{ V},$ $C_L = 100\text{ pF}‡$ $R_L = 2\text{ k}\Omega‡$	25°C	0.15	0.25		V/ μs
		Full range	0.1			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	120		nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C	22			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	2.7		μV	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	4			
I_n Equivalent input noise current		25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 1\text{ kHz},$ $R_L = 2\text{ k}\Omega‡$	25°C	$A_V = 1$	0.065%		
			$A_V = 10$	0.5%		
Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}‡$ $R_L = 2\text{ k}\Omega‡$	25°C	0.5		MHz	
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V},$ $R_L = 2\text{ k}\Omega‡$ $A_V = 1,$ $C_L = 100\text{ pF}‡$	25°C	220		kHz	
t_s Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V, $R_L = 2\text{ k}\Omega‡$ $C_L = 100\text{ pF}‡$	25°C	To 0.1%	6.4		μs
			To 0.01%	14.1		
ϕ_m Phase margin at unity gain	$R_L = 2\text{ k}\Omega‡$ $C_L = 100\text{ pF}‡$	25°C	62°			
Gain margin		25°C	11		dB	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A^\dagger	TLV243x			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	TLV243x	25°C	300	2000	μV	
			Full range	2500			
		TLV243xA	25°C	300	950		
			Full range	1500			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm \pm 2.5\text{ V},$ $R_S = 50\ \Omega$		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current			25°C	0.5	60	pA	
			Full range	150			
I_{IB} Input bias current			25°C	1	60	pA	
			Full range	150			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV},$ $R_S = 50\ \Omega$		25°C	0 to 4.5	-0.25 to 4.75	V	
			Full range	0 to 4.2			
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$		25°C	4.97		V	
			25°C	$I_{OH} = -5\text{ mA}$	4		4.35
					Full range		4
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$		25°C	0.01		V	
			25°C	0.8			
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 5\text{ mA}$	Full range	1.25				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 2\text{ k}\Omega^\ddagger$	25°C	2.5	3.8	V/mV	
			Full range	1.5			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	950			
$r_{i(d)}$ Differential input resistance			25°C	1000		$\text{G}\Omega$	
$r_{i(c)}$ Common-mode input resistance			25°C	1000		$\text{G}\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$		25°C	8		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$		25°C	130		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }4.5\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$		25°C	70	90	dB	
			Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load		25°C	80	95	dB	
			Full range	80			
I_{DD} Supply current (per channel)	$V_O = 2.5\text{ V},$ No load		25°C	100	125	μA	
			Full range	125			

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is -40°C to 85°C. Full range for the quad I suffix is -40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV243x			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}, R_L = 2\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	0.15	0.25		V/ μs
		Full range	0.1			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	100		nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C	18			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	1.9		μV	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	2.8			
I_n Equivalent input noise current		25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 1.5\text{ V to }3.5\text{ V}, f = 1\text{ kHz}, R_L = 2\text{ k}\Omega\ddagger$	$A_V = 1$	0.045%			
		$A_V = 10$	0.4%			
Gain-bandwidth product	$f = 10\text{ kHz}, R_L = 2\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	0.55		MHz	
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}, R_L = 2\text{ k}\Omega\ddagger, A_V = 1, C_L = 100\text{ pF}\ddagger$	25°C	100		kHz	
t_s Settling time	$A_V = -1, \text{ Step} = 1.5\text{ V to }3.5\text{ V}, R_L = 2\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	$T_o = 0.1\%$	6.4		μs	
		$T_o = 0.01\%$	13.1			
ϕ_m Phase margin at unity gain	$R_L = 2\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	66°			
Gain margin		25°C	11		dB	

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is –40°C to 85°C. Full range for the quad I suffix is –40°C to 125°C.

‡ Referenced to 2.5 V



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A †	TLV243xQ, TLV243xM			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	TLV2453x	25°C	300	2000	μV	
			Full range	2500			
		TLV2453xA	25°C	300	950		
			Full range	2000			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current			25°C	0.5	60	pA	
	Full range	150					
I_{IB} Input bias current			25°C	1	60	pA	
			Full range	300			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV},$ $R_S = 50\ \Omega$		25°C	0 to 4.5	-0.25 to 4.75	V	
			Full range	0 to 4.2			
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$		25°C	4.97		V	
	$I_{OH} = -5\text{ mA}$		25°C	4	4.35		
			Full range	4			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$		25°C	0.01		V	
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 5\text{ mA}$		25°C	0.8			
			Full range	1.25			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$		25°C	2.5	3.8	V/mV	
			Full range	0.5			
			25°C	950			
$r_{i(d)}$ Differential input resistance			25°C	1000		$\text{G}\Omega$	
$r_{i(c)}$ Common-mode input resistance			25°C	1000		$\text{G}\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$		25°C	8		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$		25°C	130		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }4.5\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$		25°C	70	90	dB	
			Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load		25°C	80	95	dB	
			Full range	80			
I_{DD} Supply current	$V_O = 2.5\text{ V},$ No load		25°C	200	250	μA	
			Full range	270			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV243xQ, TLV243xM, TLV243xAQ, TLV243xAM			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V},$ $R_L = 2\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	25°C	0.15	0.25		V/ μs
		Full range	0.1			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	100		nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C	18			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	1.9		μV	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	2.8			
I_n Equivalent input noise current		25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 1.5\text{ V to }3.5\text{ V},$ $f = 1\text{ kHz},$ $R_L = 2\text{ k}\Omega\ddagger$	$A_V = 1$	0.045%			
		$A_V = 10$	0.4%			
Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}\ddagger$	$R_L = 2\text{ k}\Omega\ddagger,$ 25°C	0.55		MHz	
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 2\text{ k}\Omega\ddagger,$	$A_V = 1,$ $C_L = 100\text{ pF}\ddagger$ 25°C	100		kHz	
t_s Settling time	$A_V = -1,$ Step = 1.5 V to 3.5 V, $R_L = 2\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	To 0.1%	6.4		μs	
		To 0.01%	13.1			
ϕ_m Phase margin at unity gain	$R_L = 2\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	25°C	66°			
Gain margin		25°C	11		dB	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V



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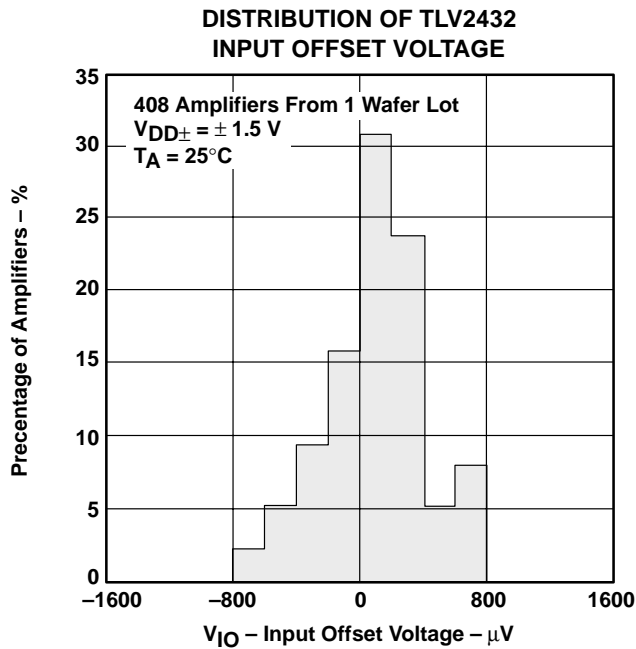


Figure 2

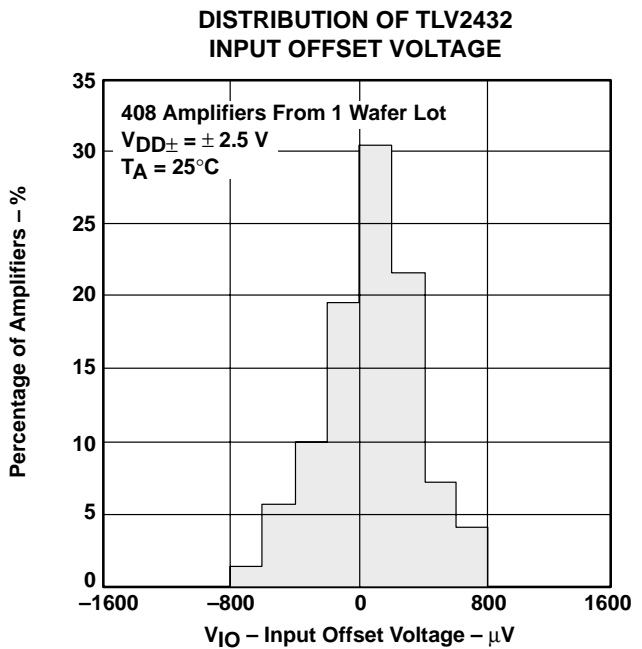


Figure 3

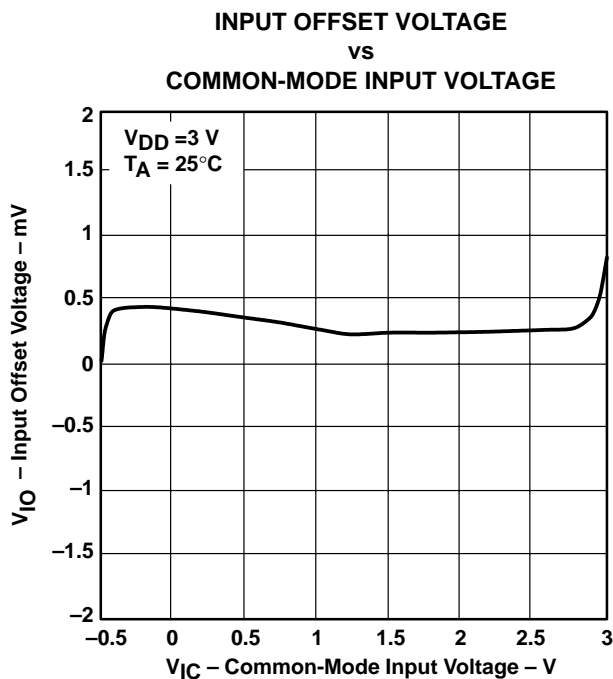


Figure 4

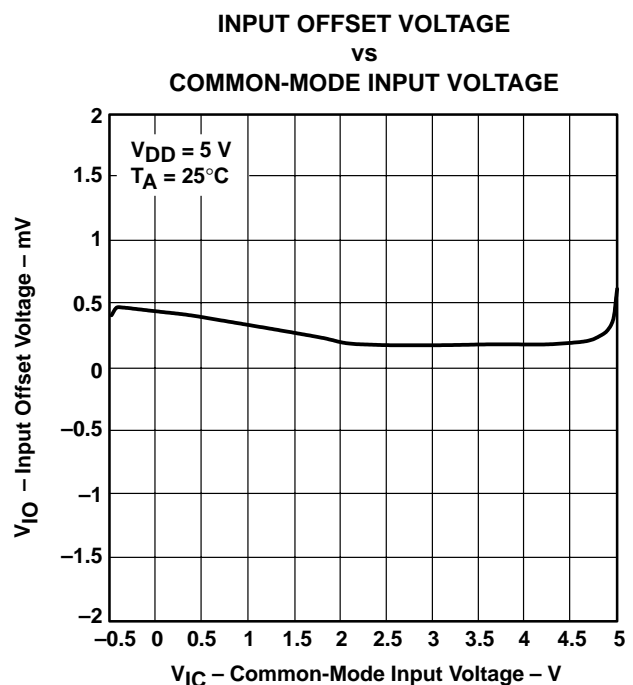


Figure 5



TYPICAL CHARACTERISTICS

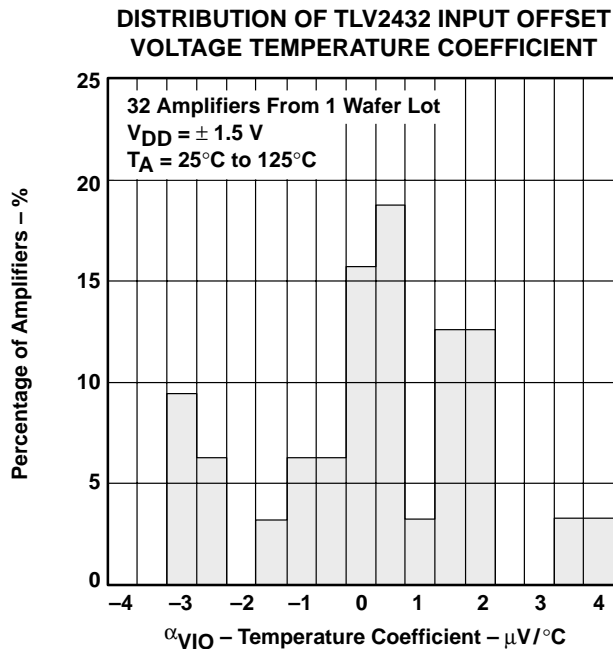


Figure 6

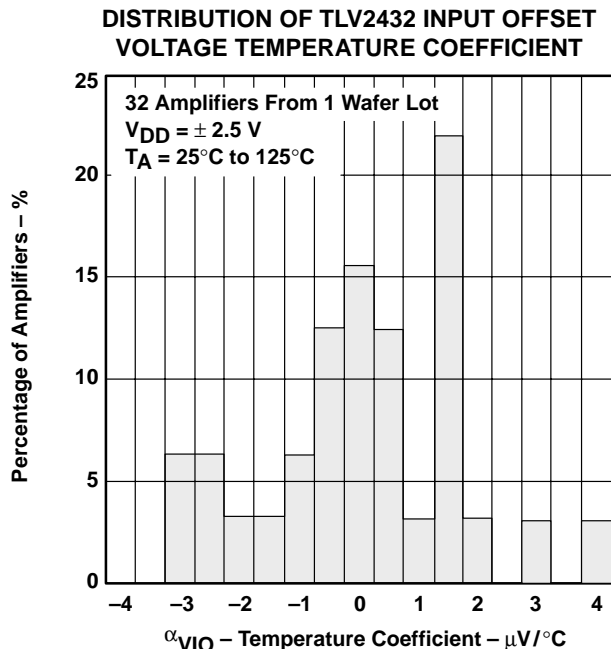


Figure 7

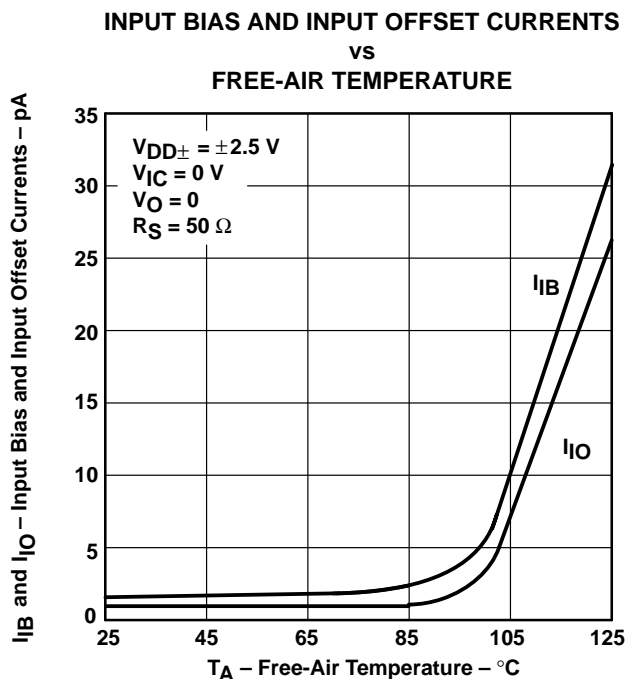


Figure 8

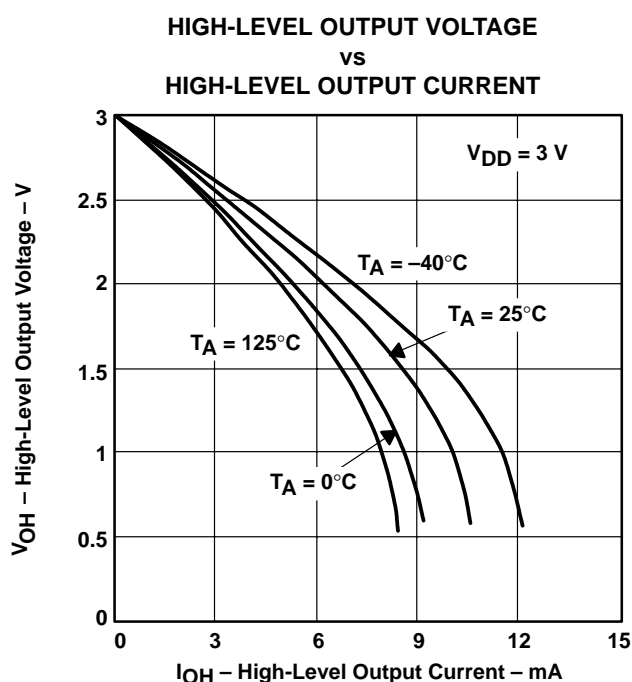


Figure 9

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TYPICAL CHARACTERISTICS

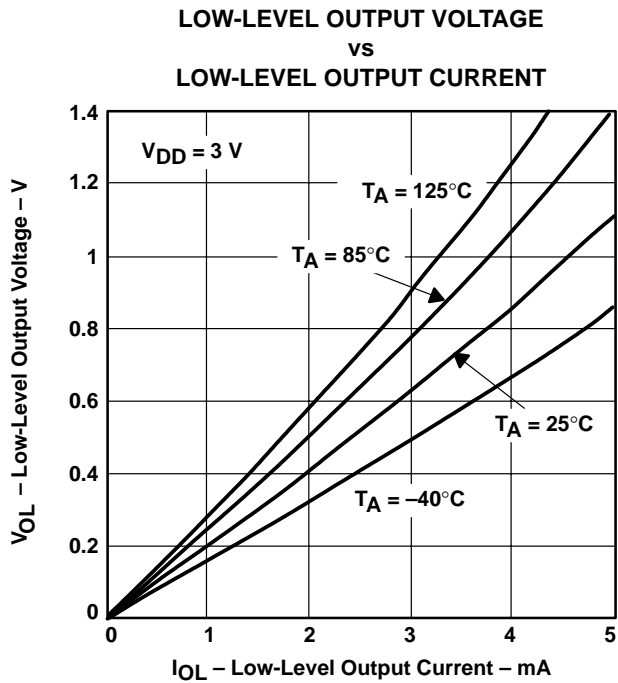


Figure 10

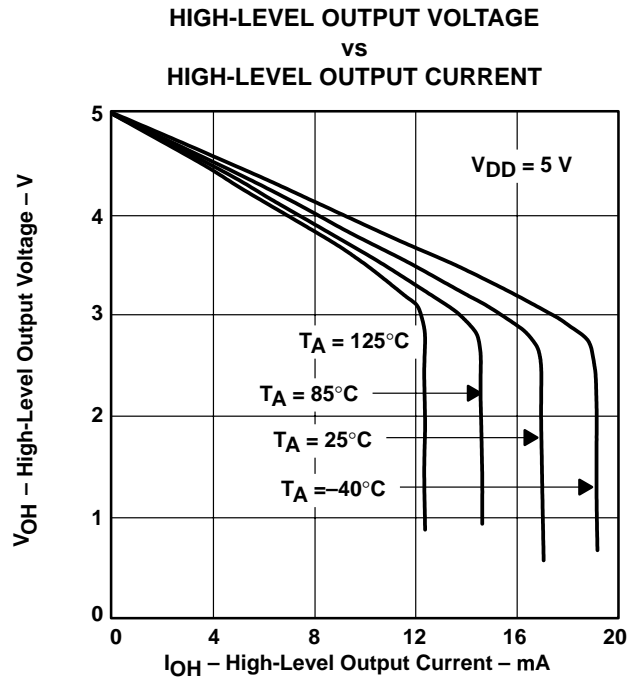


Figure 11

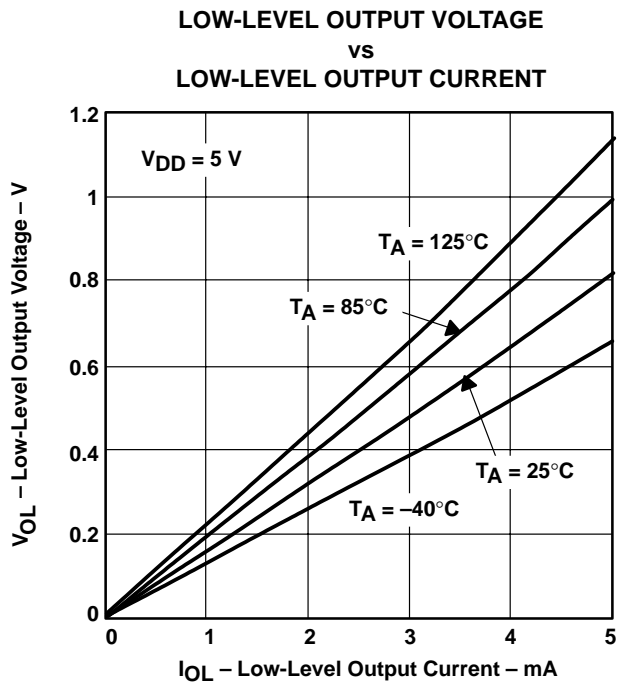


Figure 12

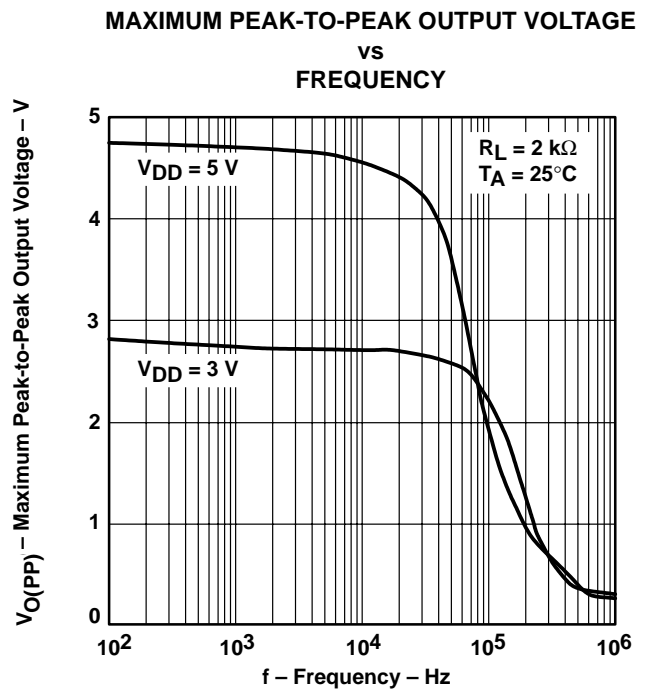


Figure 13



TYPICAL CHARACTERISTICS

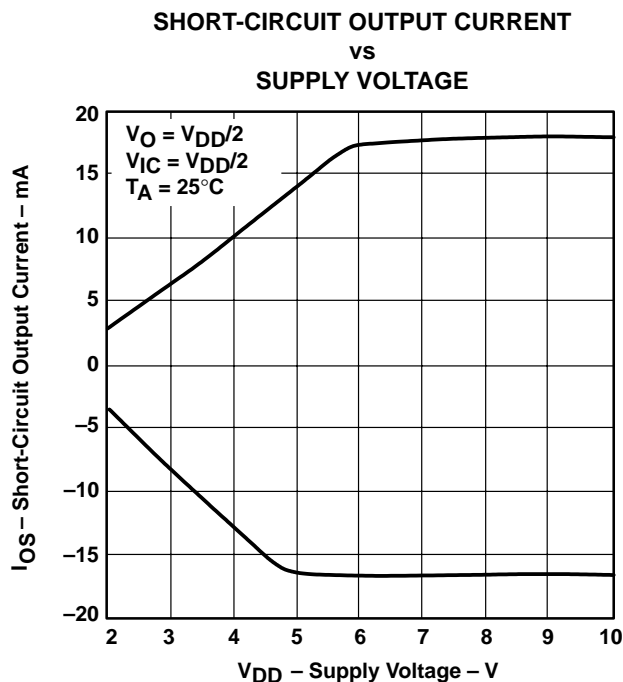


Figure 14

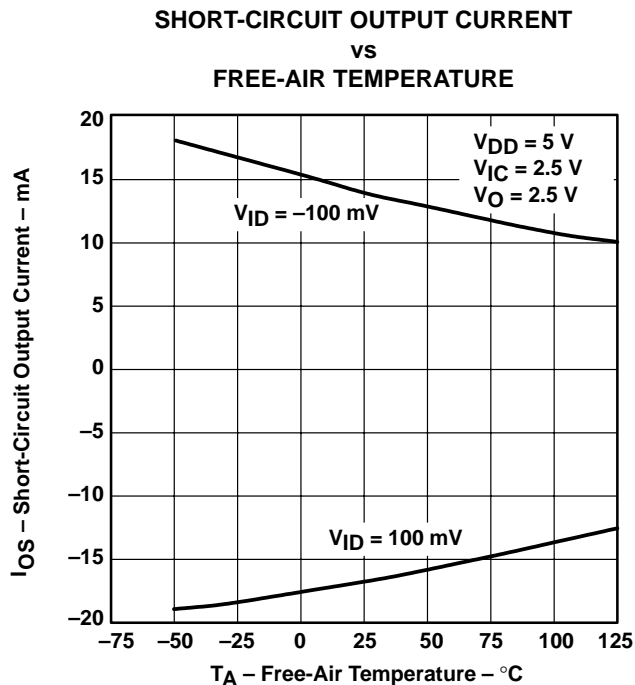


Figure 15

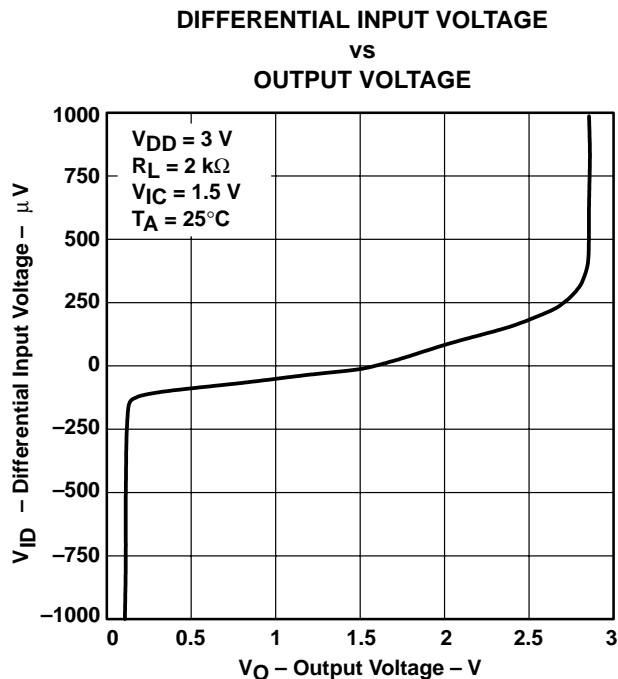


Figure 16

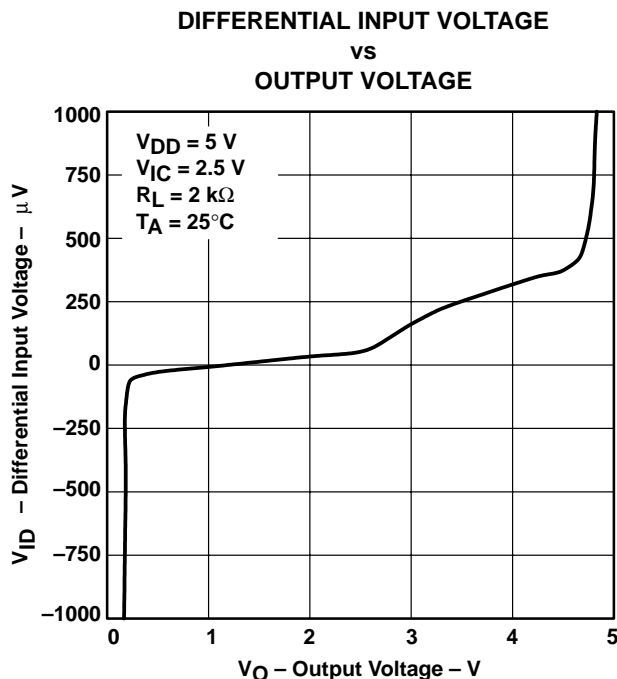


Figure 17

TYPICAL CHARACTERISTICS

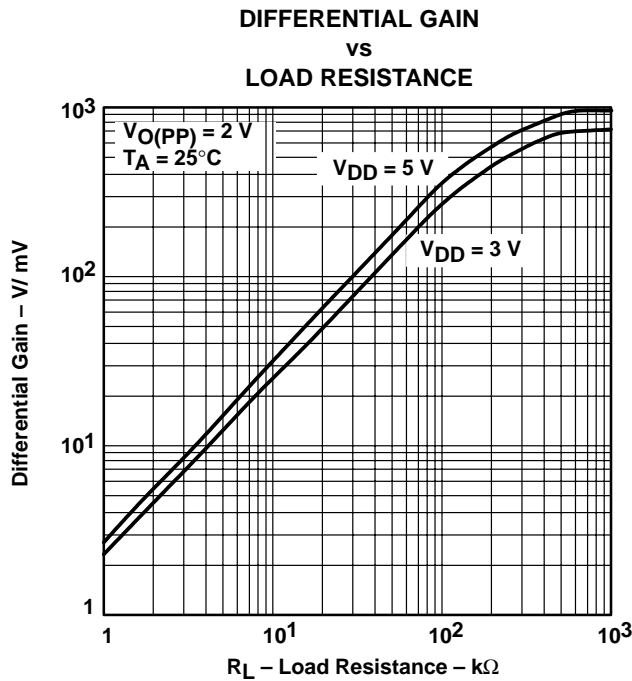


Figure 18

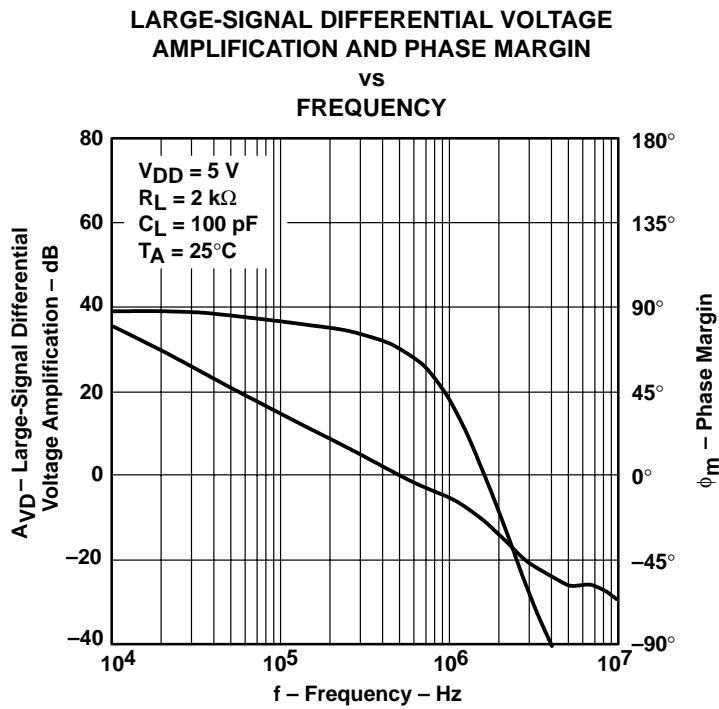


Figure 19

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN

vs
 FREQUENCY

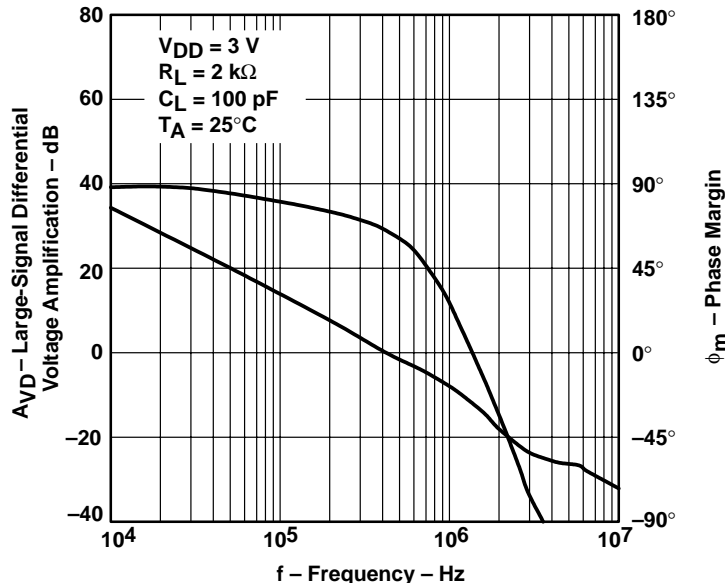


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE

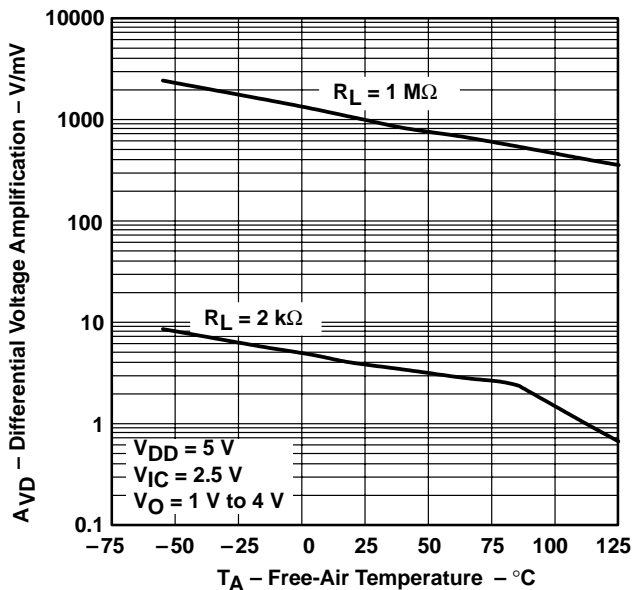


Figure 21

DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE

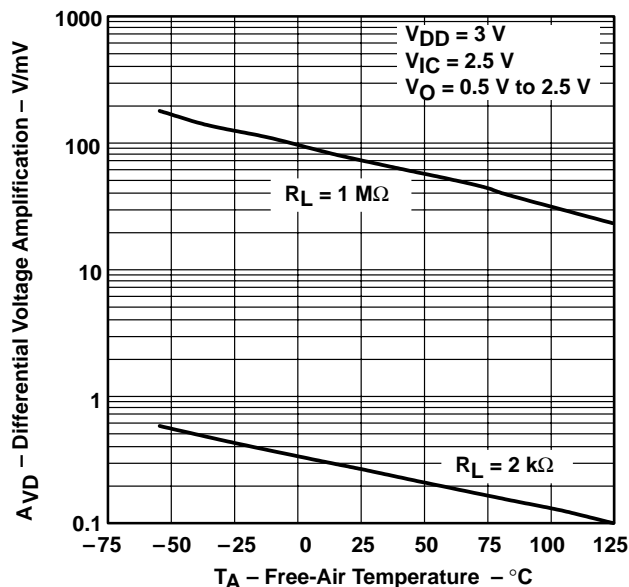


Figure 22

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**OUTPUT IMPEDANCE
VS
FREQUENCY**

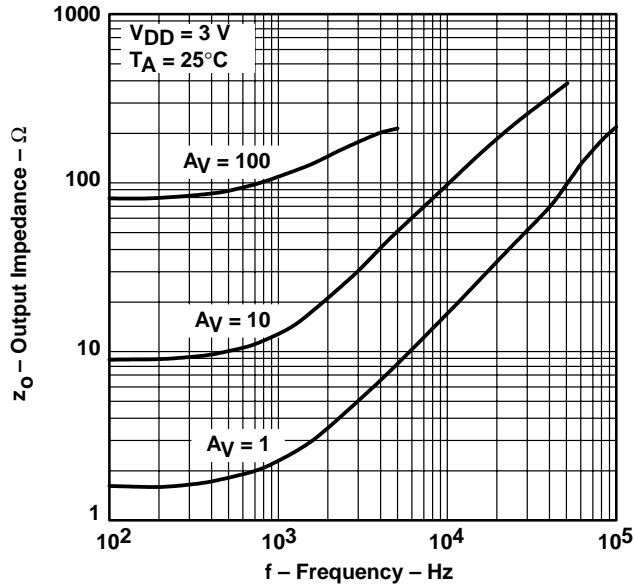


Figure 23

**OUTPUT IMPEDANCE
VS
FREQUENCY**

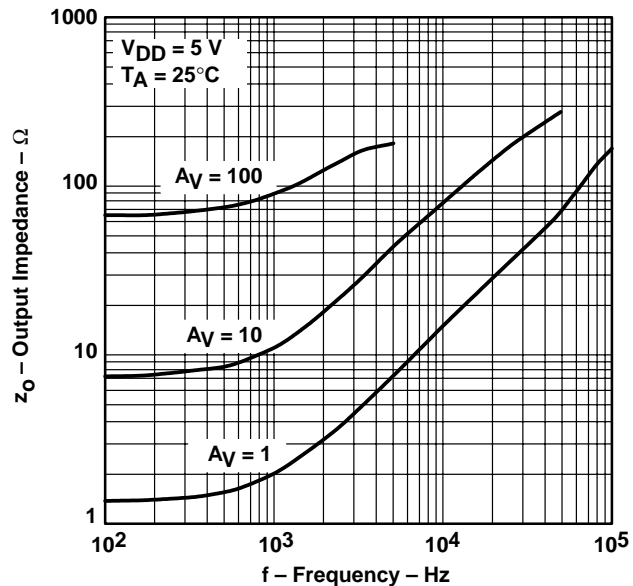


Figure 24

**COMMON-MODE REJECTION RATIO
VS
FREQUENCY**

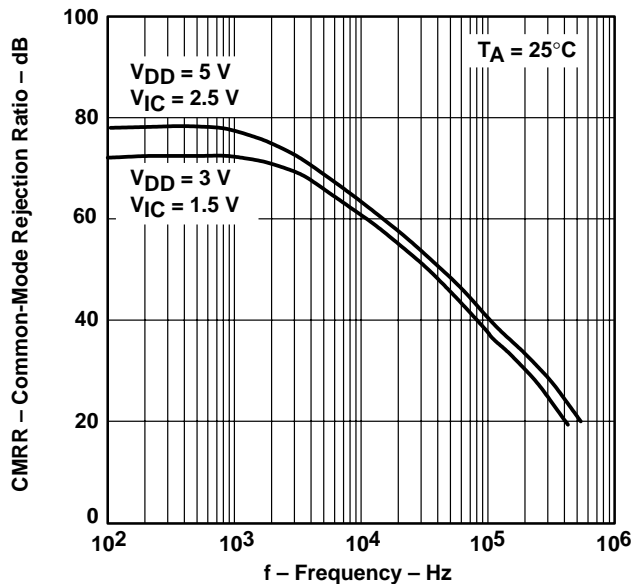


Figure 25

**COMMON-MODE REJECTION RATIO
VS
FREE-AIR TEMPERATURE**

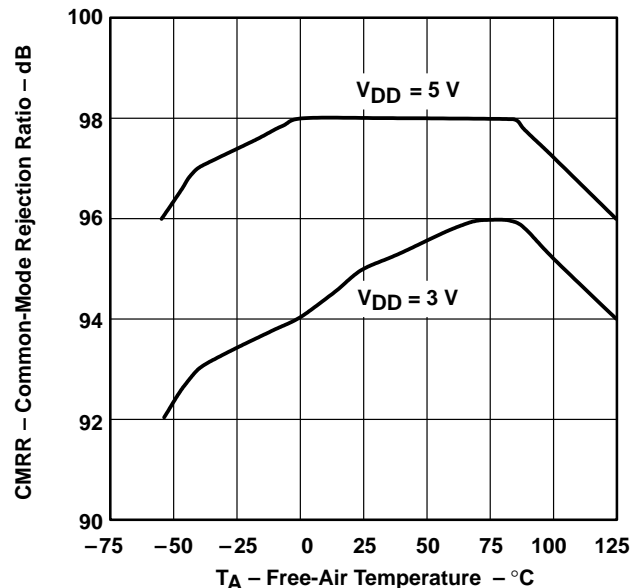


Figure 26



TYPICAL CHARACTERISTICS

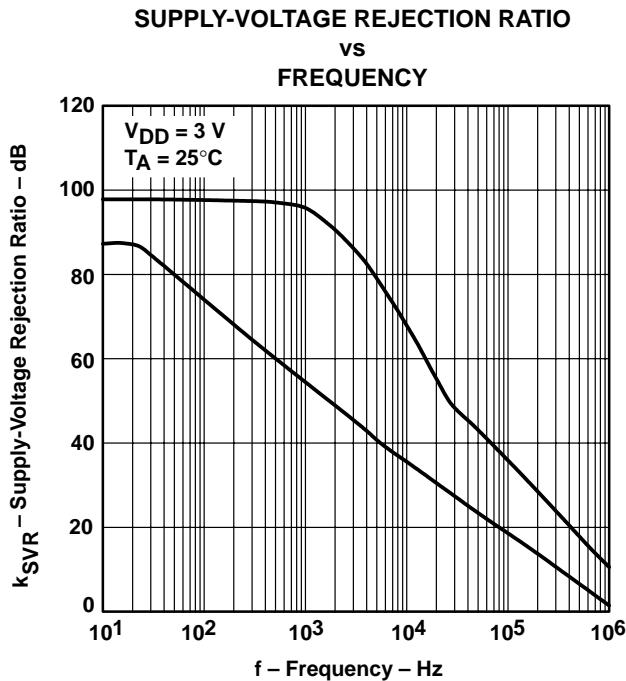


Figure 27

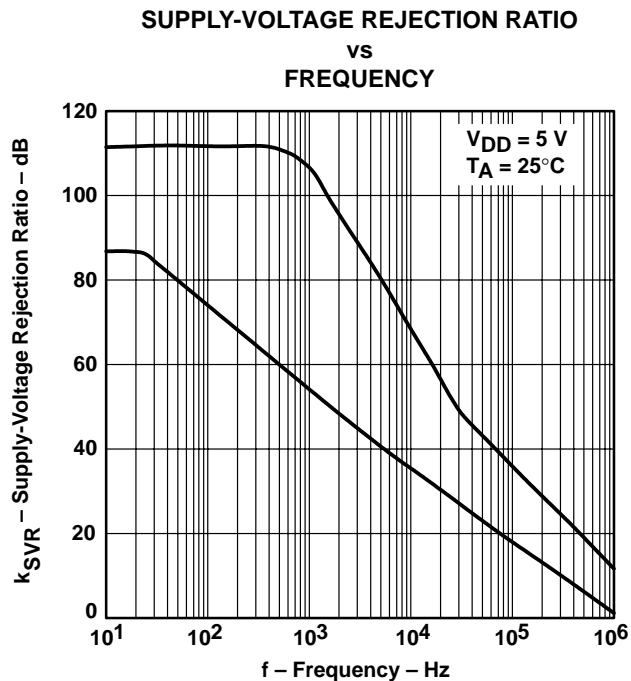


Figure 28

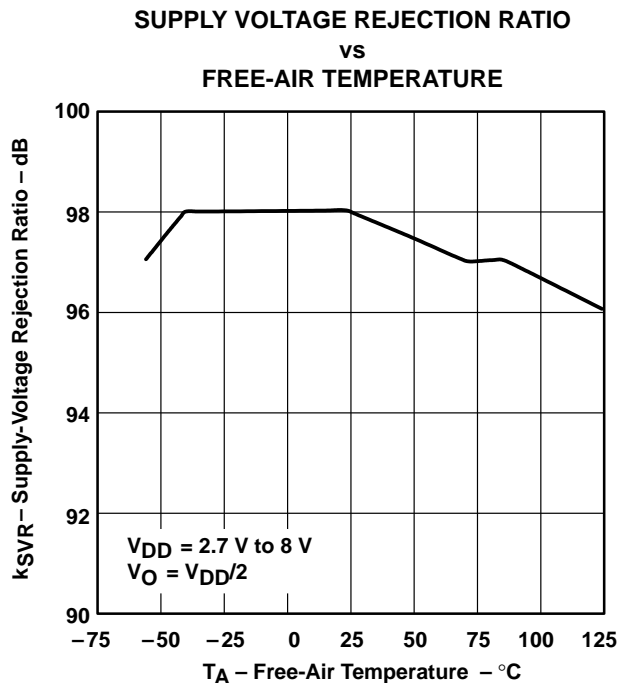


Figure 29

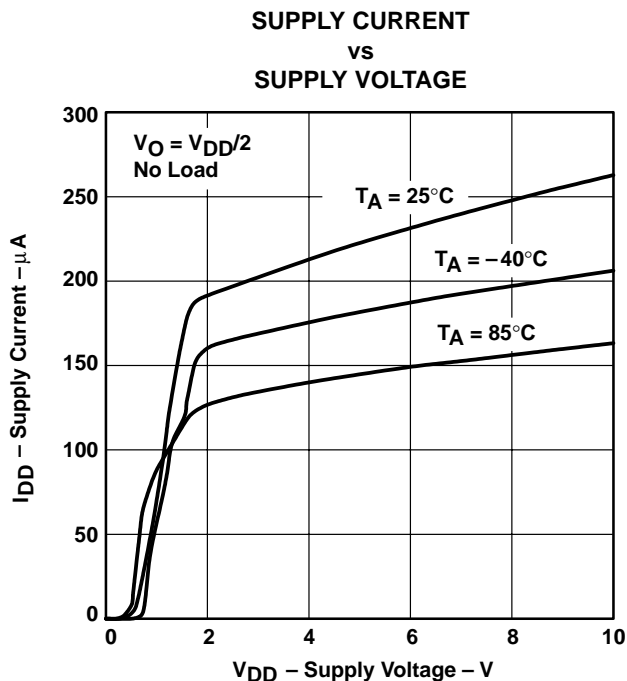


Figure 30

TYPICAL CHARACTERISTICS

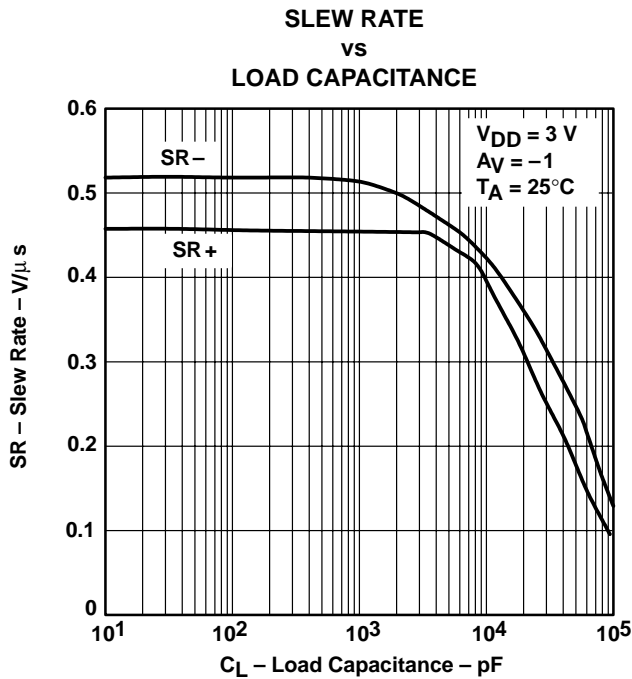


Figure 31

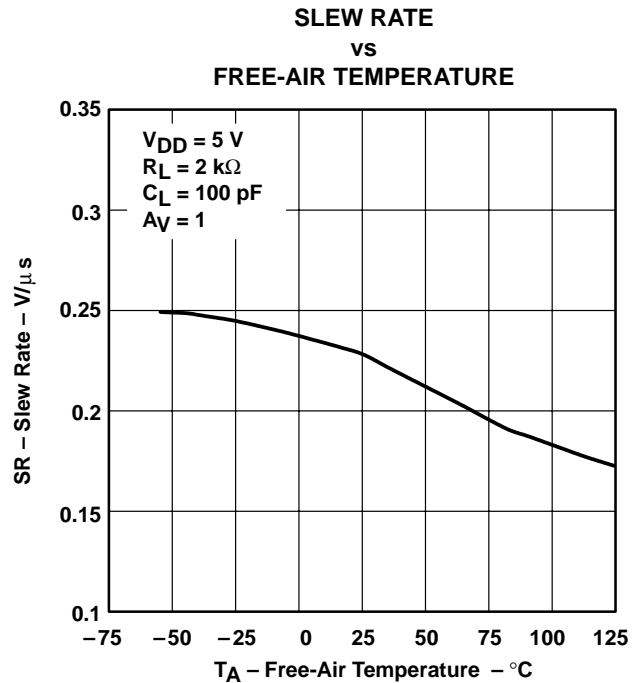


Figure 32

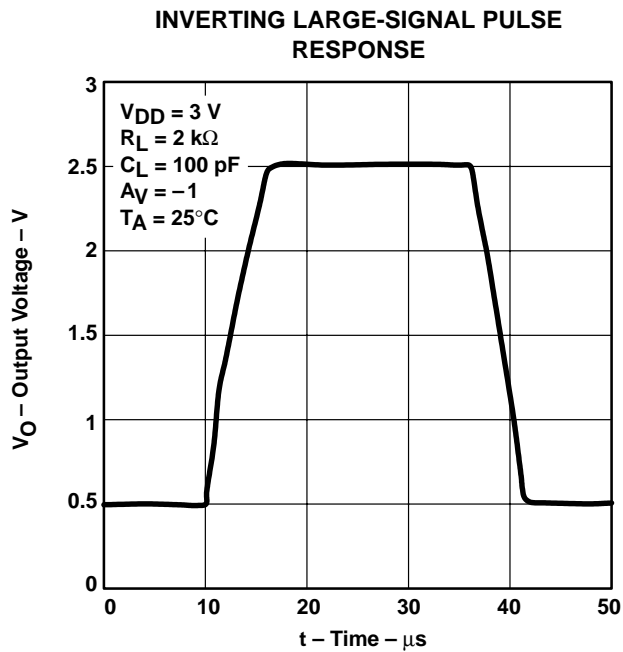


Figure 33

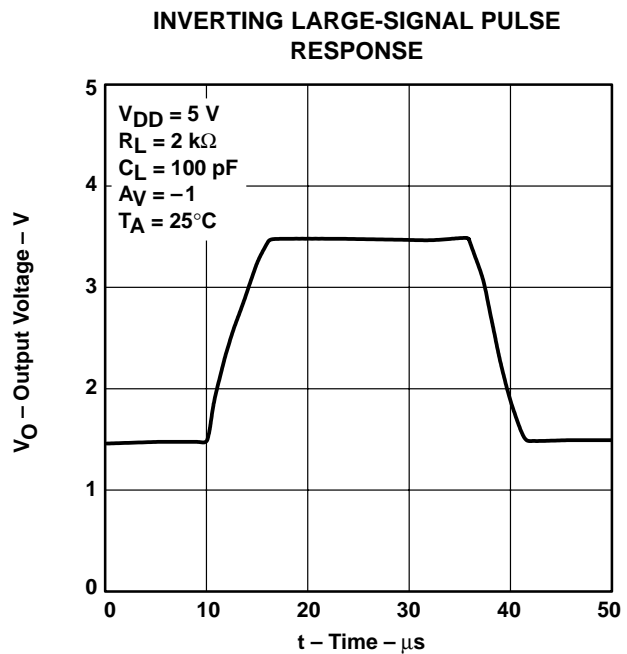


Figure 34

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

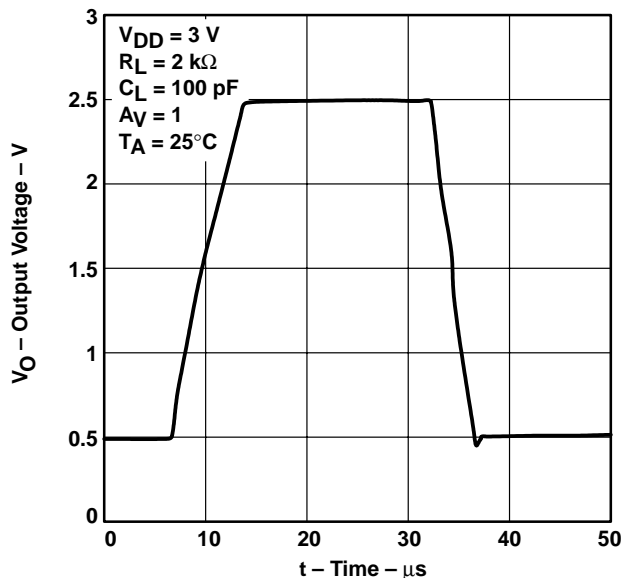


Figure 35

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

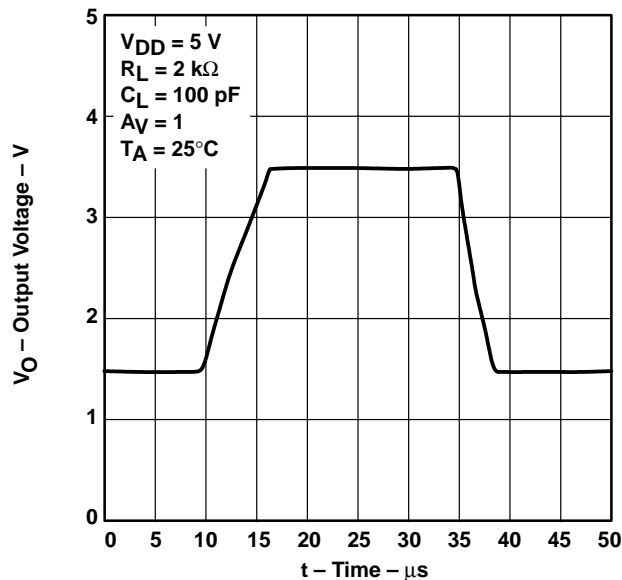


Figure 36

INVERTING SMALL-SIGNAL PULSE RESPONSE

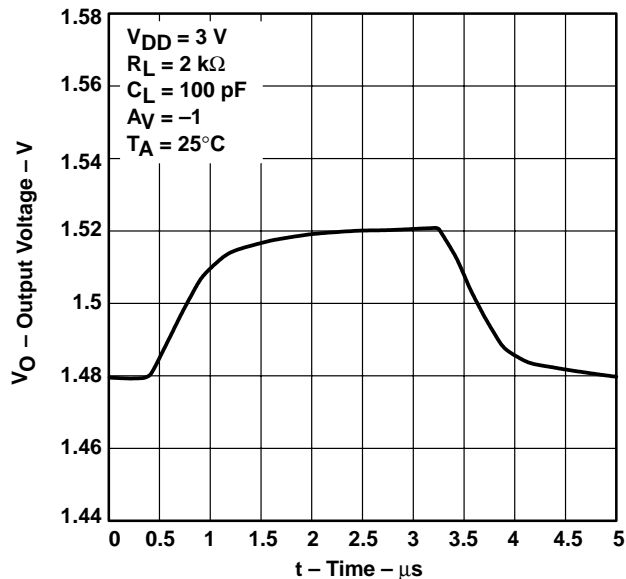


Figure 37

INVERTING SMALL-SIGNAL PULSE RESPONSE

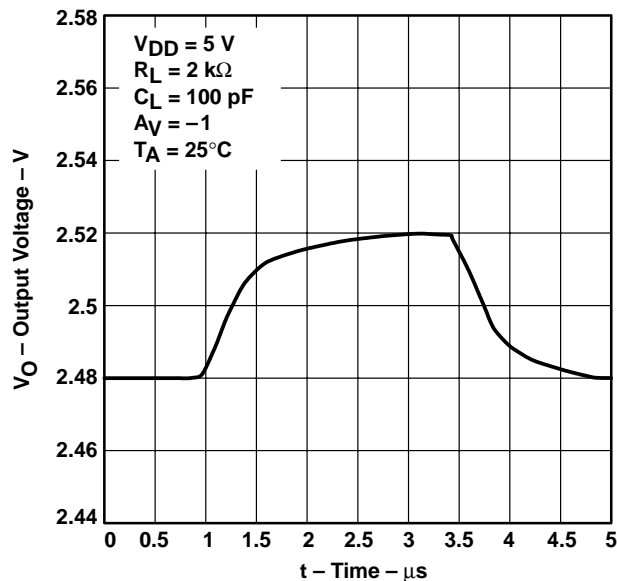


Figure 38

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WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

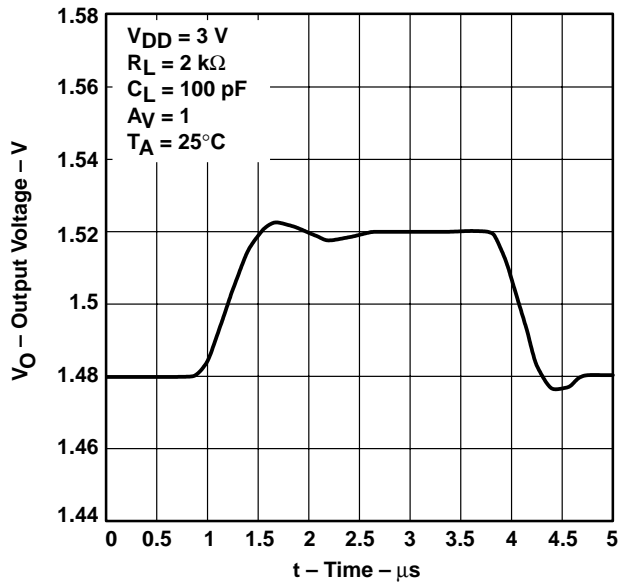


Figure 39

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

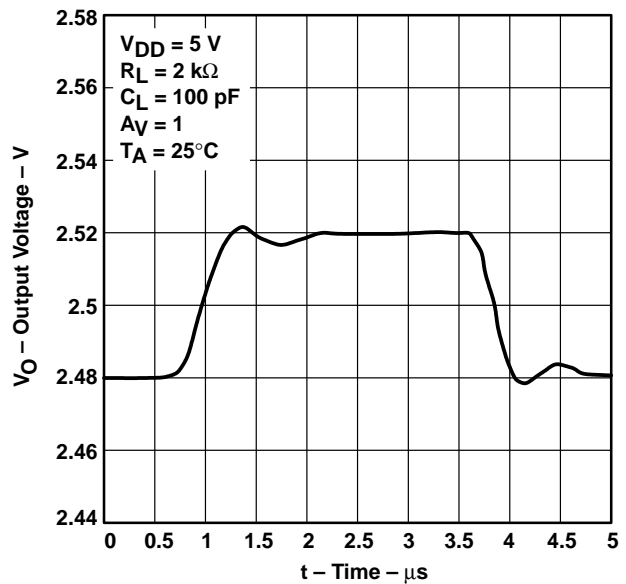


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY

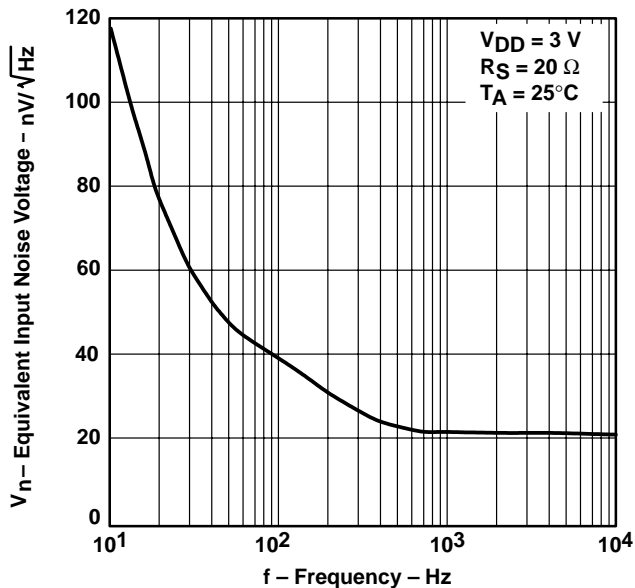


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY

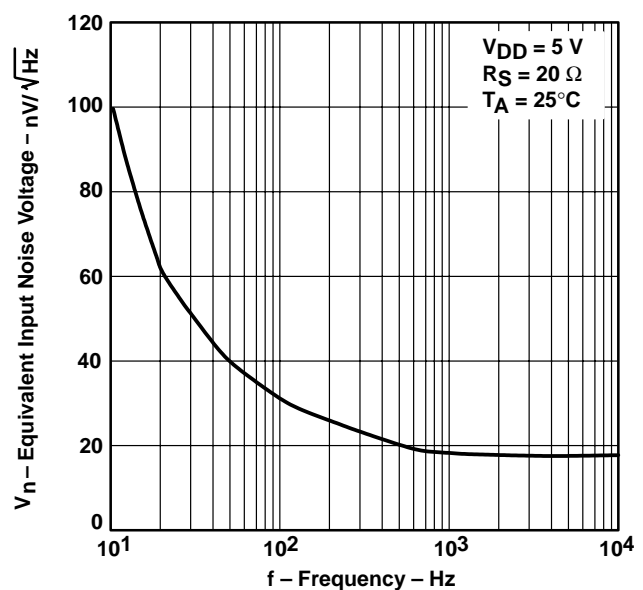


Figure 42



TYPICAL CHARACTERISTICS

NOISE VOLTAGE OVER A 10-SECOND PERIOD

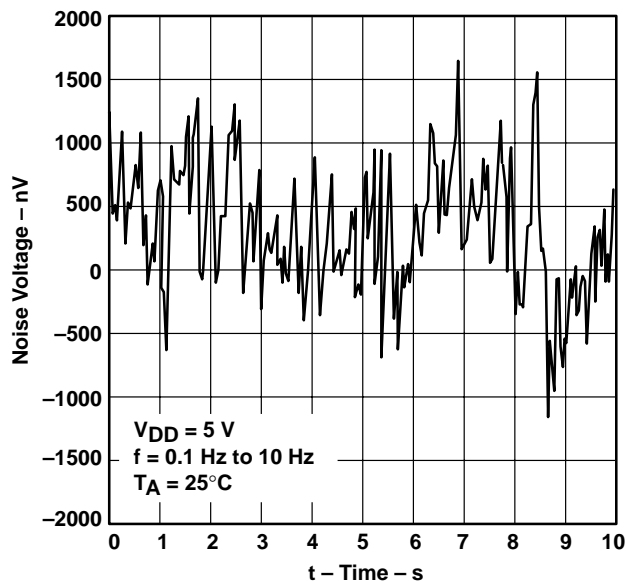


Figure 43

TOTAL HARMONIC DISTORTION PLUS NOISE
 VS
 FREQUENCY

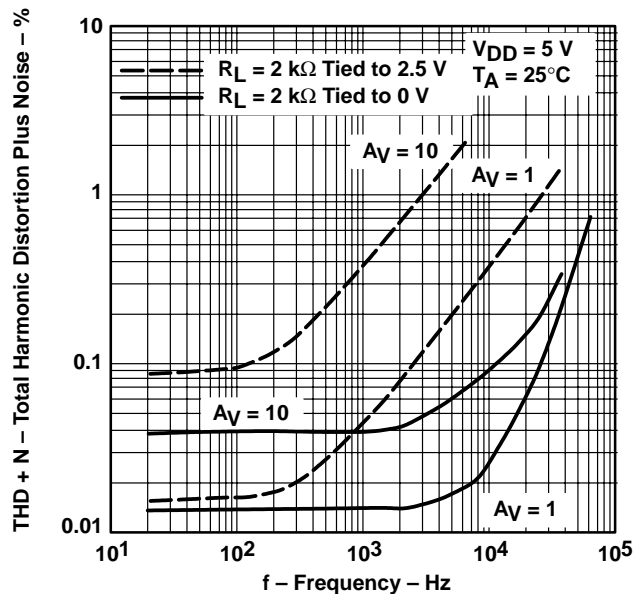


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
 VS
 FREQUENCY

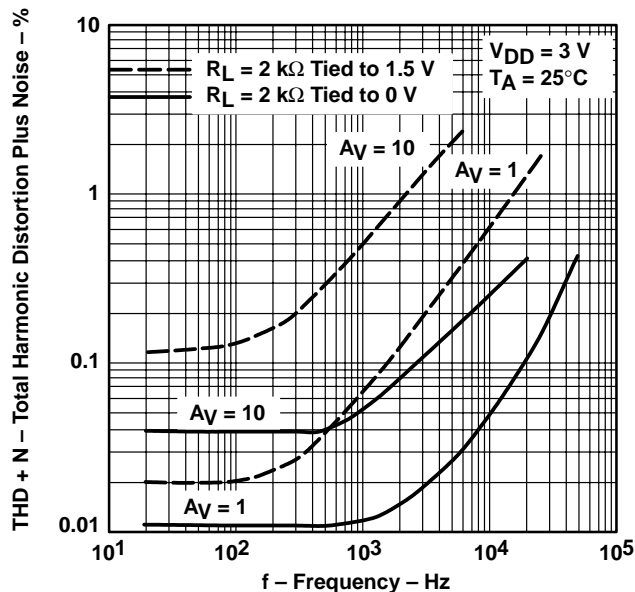


Figure 45

TLV2432, TLV2432A, TLV2434, TLV2434A
Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT
WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

SLOS168F – NOVEMBER 1996 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

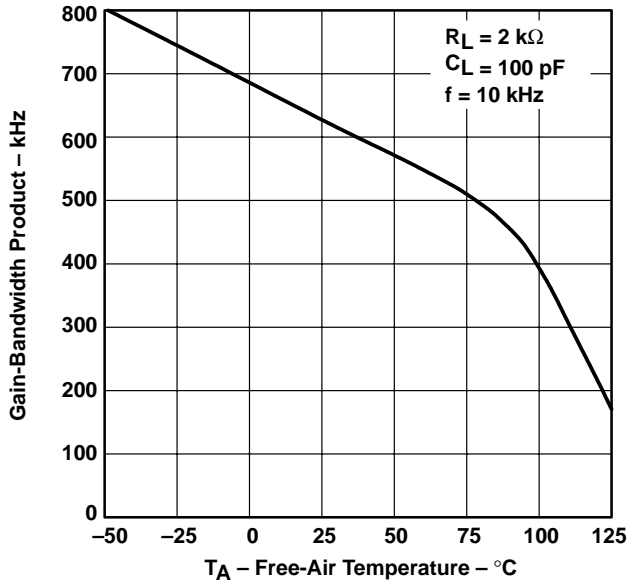


Figure 46

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

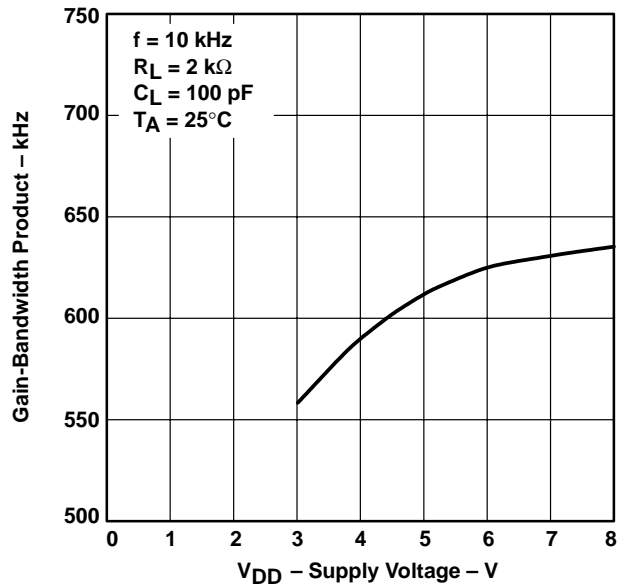


Figure 47

PHASE MARGIN
vs
LOAD CAPACITANCE

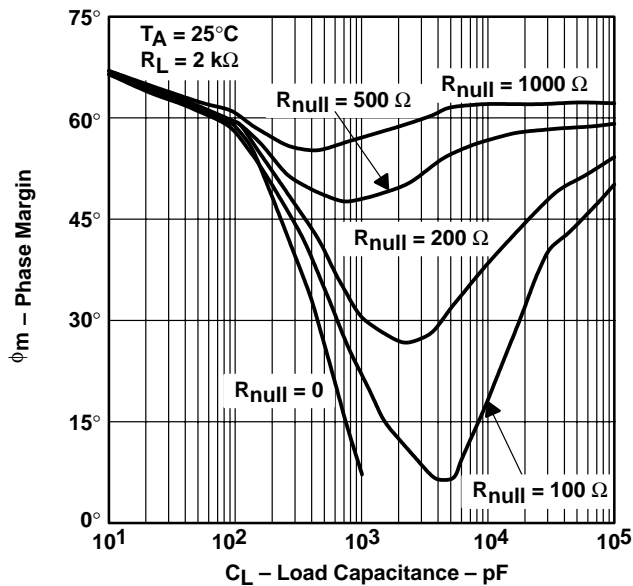


Figure 48

GAIN MARGIN
vs
LOAD CAPACITANCE

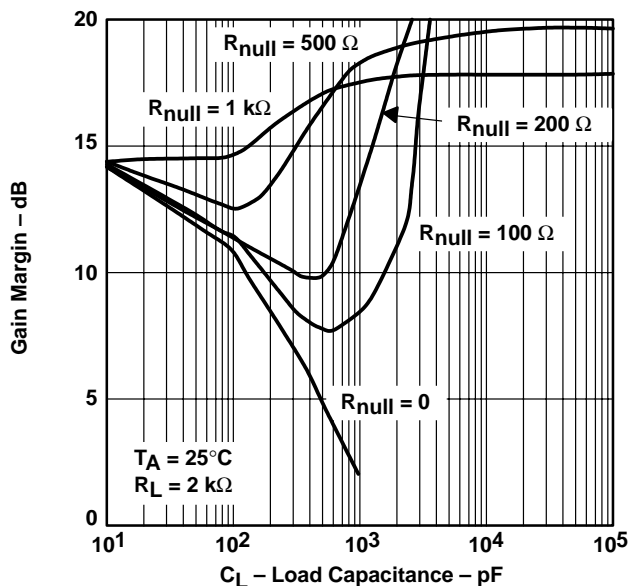


Figure 49



TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

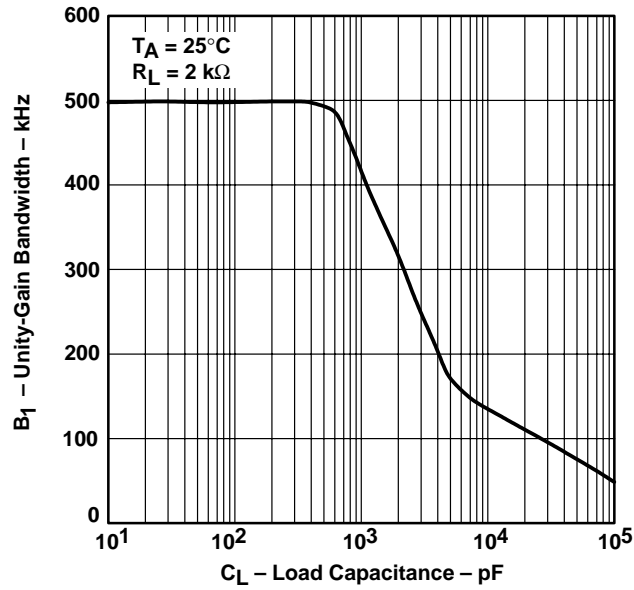


Figure 50

TLV2432, TLV2432A, TLV2434, TLV2434A Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

SLOS168F – NOVEMBER 1996 – REVISED MARCH 2001

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 51 are generated using the TLV243x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

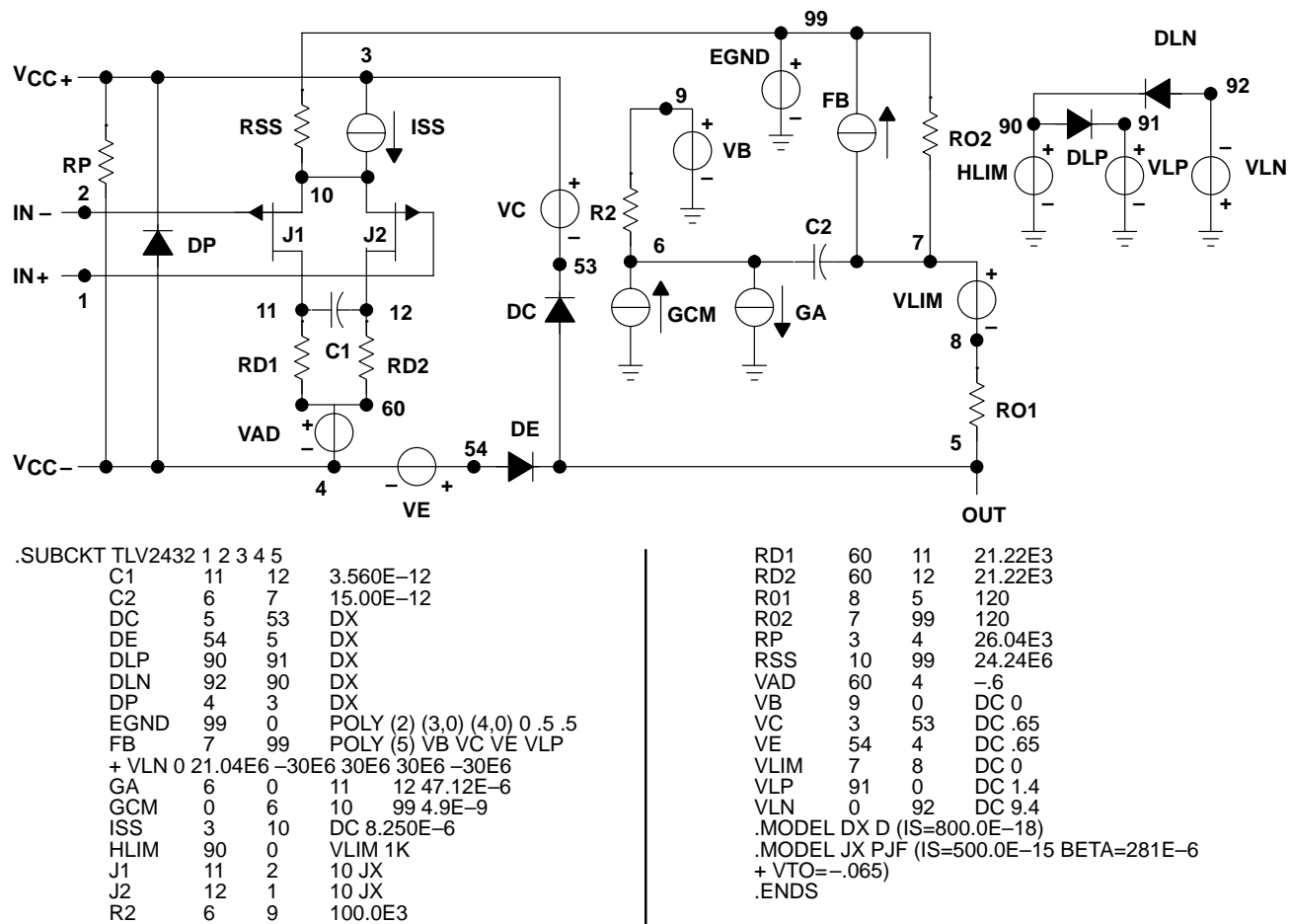


Figure 51. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9751001Q2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751001Q2A TLV2432 MFKB	
5962-9751001QHA	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751001QHA TLV2432M	
5962-9751001QPA	NRND	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751001QPA TLV2432M	
5962-9751002Q2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751002Q2A TLV2432 AMFKB	
5962-9751002QHA	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751002QHA TLV2432AM	
5962-9751002QPA	NRND	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751002QPA TLV2432AM	
TLV2432AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TV2432	Samples
TLV2432AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TV2432	Samples
TLV2432AIPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		
TLV2432AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AMFKB	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751002Q2A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										TLV2432 AMFKB	
TLV2432AMJGB	NRND	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751002QPA TLV2432AM	
TLV2432AMUB	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751002QHA TLV2432AM	
TLV2432AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A	Samples
TLV2432AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A	Samples
TLV2432AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLV2432AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A	Samples
TLV2432CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2432C	Samples
TLV2432CDG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70		Samples
TLV2432CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2432C	Samples
TLV2432CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2432C	Samples
TLV2432ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I	Samples
TLV2432IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I	Samples
TLV2432IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I	Samples
TLV2432IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I	Samples
TLV2432MFKB	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9751001Q2A TLV2432 MFKB	
TLV2432MJGB	NRND	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751001QPA TLV2432M	
TLV2432MUB	NRND	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9751001QHA TLV2432M	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2432QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432Q	Samples
TLV2432QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432Q	Samples
TLV2432QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLV2434AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI	Samples
TLV2434AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI	Samples
TLV2434AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI	Samples
TLV2434AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI	Samples
TLV2434CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C	Samples
TLV2434CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C	Samples
TLV2434CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C	Samples
TLV2434CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C	Samples
TLV2434ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2434IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2432, TLV2432A, TLV2432AM, TLV2432M, TLV2434A :

- Catalog: [TLV2432A](#), [TLV2432](#)
- Automotive: [TLV2432-Q1](#), [TLV2432A-Q1](#), [TLV2432A-Q1](#), [TLV2432-Q1](#), [TLV2434A-Q1](#)
- Military: [TLV2432M](#), [TLV2432AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2432AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2432CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2434AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

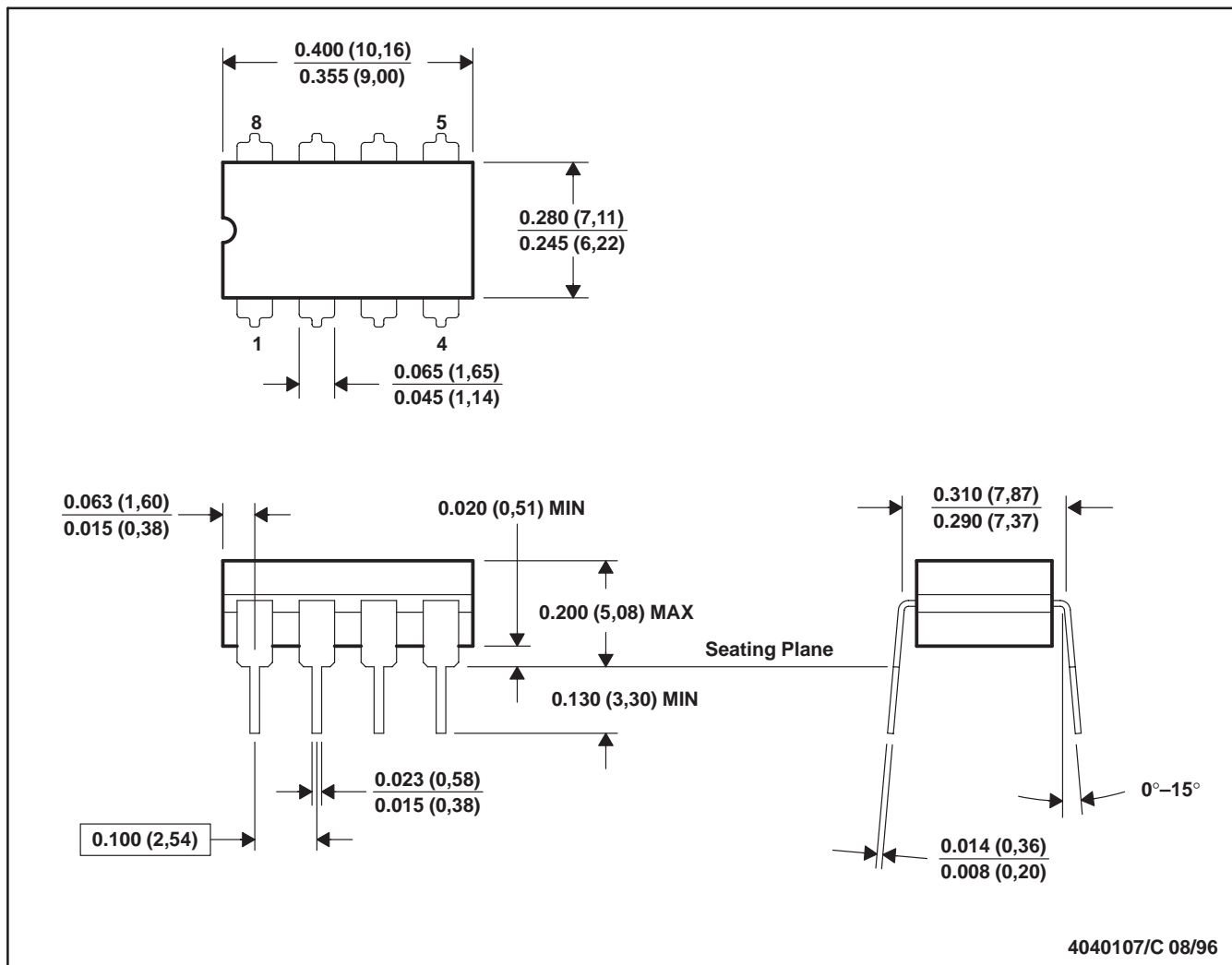
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2432AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2432AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2432CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2432IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2434AIDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2434AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2434CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2434CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2434IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2434IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

JG (R-GDIP-T8)

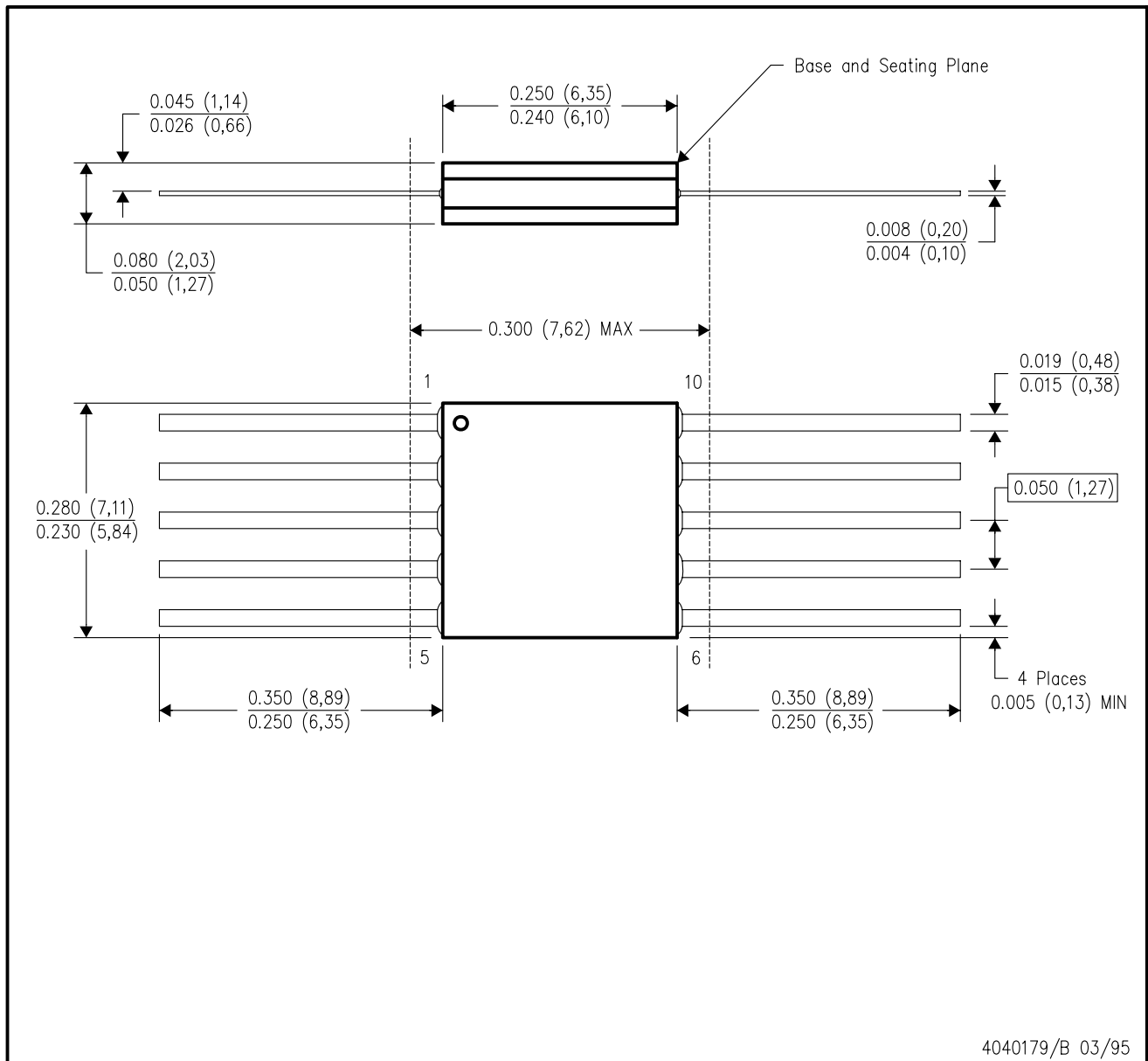
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - (D) Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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