LMZ22010

LMZ22010 10A SIMPLE SWITCHER® Power Module with 20V Maximum Input Voltage and Current Sharing

Texas Instruments

Literature Number: SNVS687D

National Semiconductor

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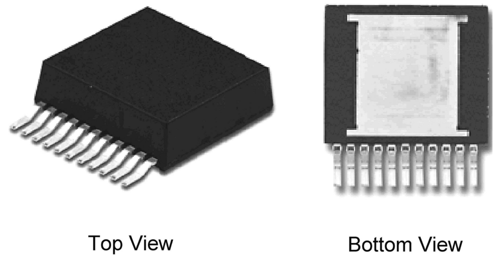
10A SIMPLE SWITCHER® Power Module with 20V Maximum Input Voltage and Current Sharing

Easy to use 11 pin package


Top View
Bottom View

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TO-PMOD 11 Pin Package
15 x 17.79 x 5.9 mm (0.59 x 0.7 x 0.232 in)
θ_{JA} = 9.9 °C/W, θ_{JC} = 1.0 °C/W (*Note 1*)
RoHS Compliant

Electrical Specifications

- 50W maximum total output power
- Up to 10A output current
- Input voltage range 6V to 20V
- Output voltage range 0.8V to 6V
- Efficiency up to 92%

Key Features

- Integrated shielded inductor
- Simple PCB layout
- Frequency synchronization input (350 kHz to 600 kHz)
- Current sharing capability
- Flexible startup sequencing using external soft-start, tracking and precision enable
- Protection against inrush currents and faults such as input UVLO and output short circuit
- – 40°C to 125°C junction temperature range
- Single exposed pad and standard pinout for easy mounting and manufacturing
- Fully enabled for Webench® Power Designer
- Pin compatible with LMZ22008/06, LMZ12010/08/06, LMZ23610/08/06, and LMZ13610/08/06

Applications

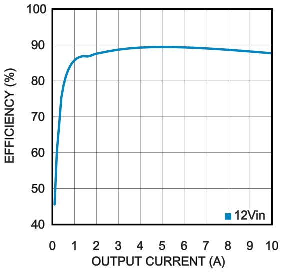
- Point of load conversions from 12V input rail
- Time critical projects
- Space constrained / high thermal requirement applications
- Negative output voltage applications See AN-2027

Performance Benefits

- High efficiency reduces system heat generation
- Low radiated emissions (EMI) complies with EN55022 (*Note 2*)
- Only 7 external components
- Low output voltage ripple
- No external heat sink required
- Simple current sharing for higher current applications

System Performance

Efficiency V_{IN} = 12V, V_{OUT} = 3.3V



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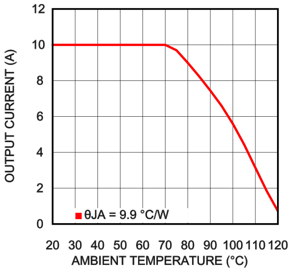
Thermal derating curve
V_{IN} = 12V, V_{OUT} = 3.3V



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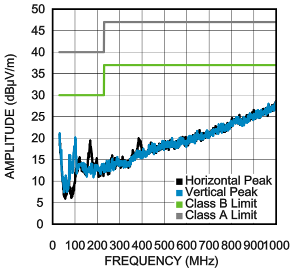
Radiated EMI (EN 55022)
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 10A



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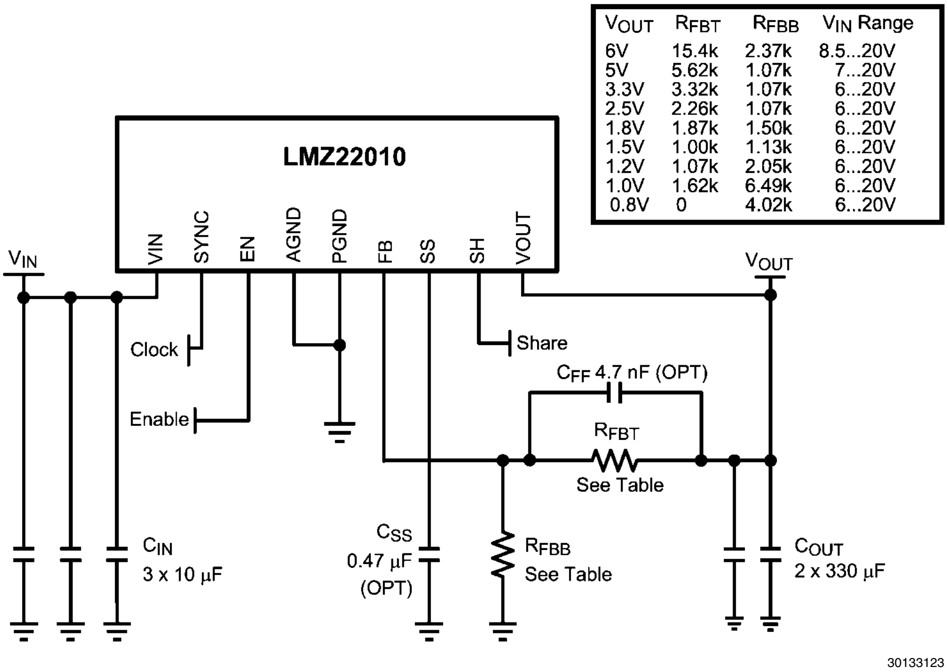
Note 1: θ_{JA} measured on a 75mm x 90 mm four-layer PCB

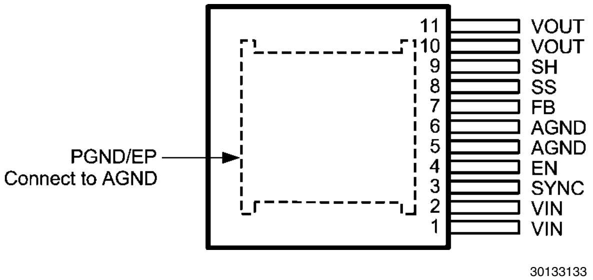
Note 2: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B, tested on Evaluation Board with EMI configuration

Simplified Application Schematic



V_{OUT}	R_{FBT}	R_{FBB}	V_{IN} Range
6V	15.4k	2.37k	8.5...20V
5V	5.62k	1.07k	7...20V
3.3V	3.32k	1.07k	6...20V
2.5V	2.26k	1.07k	6...20V
1.8V	1.87k	1.50k	6...20V
1.5V	1.00k	1.13k	6...20V
1.2V	1.07k	2.05k	6...20V
1.0V	1.62k	6.49k	6...20V
0.8V	0	4.02k	6...20V

Connection Diagram



Top View
11-Lead TO-PMOD

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LMZ22010TZ	TO-PMOD-11	TZA11A	32 Units in a Rail
LMZ22010TZE	TO-PMOD-11	TZA11A	250 Units on Tape and Reel

Pin Descriptions

Pin	Name	Description
1, 2	VIN	Input supply — Nominal operating range is 6V to 20V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and the exposed pad (PGND).
3	SYNC	Synchronization — Apply a CMOS logic level square wave whose frequency is between 314 kHz and 600 kHz to synchronize the PWM operating frequency to an external frequency source. When not using synchronization this pin must be tied to ground. The module free running PWM frequency is 359 kHz (Typ).
4	EN	Enable — Input to the precision enable comparator. Rising threshold is 1.274V typical. Once the module is enabled, a 13 uA source current is internally activated to facilitate programmable hysteresis.

Pin	Name	Description
5, 6	AGND	Analog Ground — Reference point for all stated voltages. Must be externally connected to PGND(EP).
7	FB	Feedback — Internally connected to the regulation amplifier and over-voltage comparator. The regulation reference point is 0.795V at this input pin. Connect the feedback resistor divider between VOUT and AGND to set the output voltage.
8	SS	Soft-Start/Track Input — To extend the 1.6 mSec internal soft-start connect an external soft start capacitor. For tracking connect to an external resistive divider connected to a higher priority supply rail. See applications section.
9	SH	Share — Connect this pin to the share pin of other LMZ22010 modules to share the load between the devices. One device should be configured as the master by connecting FB normally. All other devices should be configured as slaves by leaving their respective FB pins floating. Leave SH floating if current sharing is not used. Do Not Ground. See applications section.
10, 11	VOUT	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and exposed pad (PGND).
EP	PGND	Exposed Pad / Power Ground — Electrical path for the power circuits within the module. PGND is not internally connected to AGND (pin 5,6). Must be electrically connected to pins 5 and 6 external to the package. The exposed pad is also used to dissipate heat from the package during operation. Use one hundred 12 mil thermal vias from top to bottom copper for best thermal performance.

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN to PGND	-0.3V to 24V
EN, SYNC to AGND	-0.3V to 5.5V
SS, FB, SH to AGND	-0.3V to 2.5V
AGND to PGND	-0.3V to 0.3V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility (Note 4)	± 2 kV

For soldering specifications:
see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 3)

VIN	6V to 20V
EN, SYNC	0V to 5.0V
Operation Junction Temperature	−40°C to 125°C

Electrical Characteristics

Limits in standard type are for $T_J = 25°C$ only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, V_{OUT} = 3.3V

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
SYSTEM PARAMETERS						
Enable Control						
V_{EN}	EN threshold	V_{EN} rising	**1.096**	1.274	**1.452**	V
$I_{EN\text{-}HYS}$	EN hysteresis source current	V_{EN} > 1.274V		13		µA
Soft-Start						
I_{SS}	SS source current	V_{SS} = 0V	**40**	50	**60**	µA
t_{SS}	Internal soft-start interval			1.6		msec
Current Limit						
I_{CL}	Current limit threshold	d.c. average	12.5			A
Internal Switching Oscillator						
f_{osc}	Free-running oscillator frequency	Sync input connected to ground	314	359	404	kHz
f_{sync}	Synchronization range	V_{sync} = 3.3Vp-p	314		600	kHz
$V_{IL\text{-}sync}$	Synchronization logic zero amplitude	Relative to AGND			**0.4**	V
$V_{IH\text{-}sync}$	Synchronization logic one amplitude	Relative to AGND	**1.8**			V
Sync $_{d.c.}$	Synchronization duty cycle range		15	50	85	%
Regulation and Over-Voltage Comparator						
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V I_O = 10A	**0.775**	0.795	**0.815**	V
$V_{FB\text{-}OV}$	Feedback over-voltage protection threshold			0.86		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non Switching Quiescent Current	SYNC = 3.0V		3		mA
I_{SD}	Shut Down Quiescent Current	V_{EN} = 0V		32		µA
D_{max}	Maximum Duty Factor			85		%
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
$T_{SD\text{-}HYST}$	Thermal shutdown hysteresis	Falling		15		°C
θ_{JA}	Junction to Ambient (Note 7)	Natural Convection		9.9		°C/W
		225 LFPM		6.8		
		500 LFPM		5.2		
θ_{JC}	Junction to Case			1.0		°C/W

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
PERFORMANCE PARAMETERS(Note 8)						
ΔV_O	Output voltage ripple	BW@ 20 MHz		24		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line regulation	V_{IN} = 12V to 20V, I_{OUT}= 10A		±0.2		%
$\Delta V_O/\Delta I_{OUT}$	Load regulation	V_{IN} = 12V, I_{OUT}= 0.001A to 10A		1		mV/A
η	Peak efficiency	V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 5A		89.5		%
η	Full load efficiency	V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 10A		87.5		%

Note 3: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 4: The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

Note 5: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 6: Typical numbers are at 25°C and represent the most likely parametric norm.

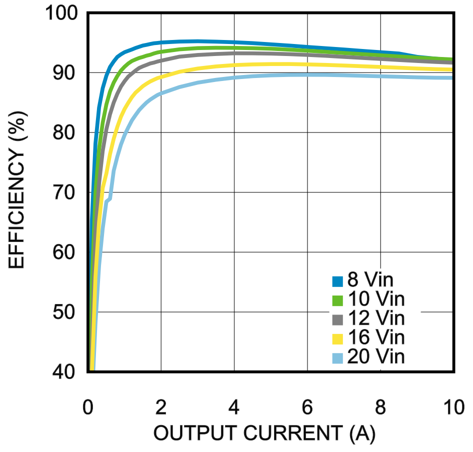
Note 7: Theta JA measured on a 3.0" x 3.5" four layer board, with two ounce copper on outer layers and one ounce copper on inner layers, two hundred and ten 12 mil thermal vias, and 2W power dissipation. Refer to evaluation board application note layout diagrams.

Note 8: Refer to BOM in *Typical Application Bill of Materials — Table 1*.

Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

Efficiency 5.0V output @ 25°C



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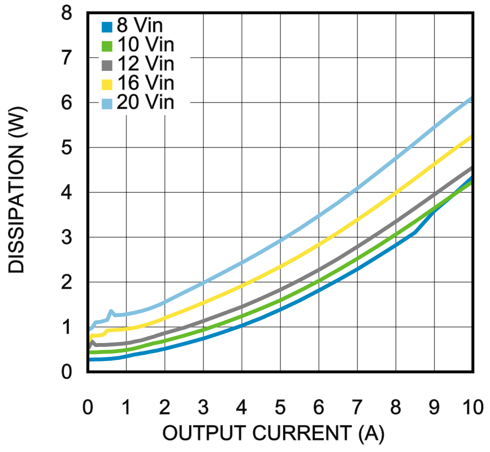
Dissipation 5.0V output @ 25°C



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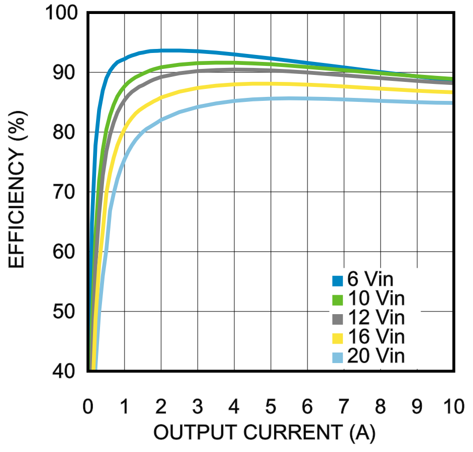
Efficiency 3.3V output @ 25°C



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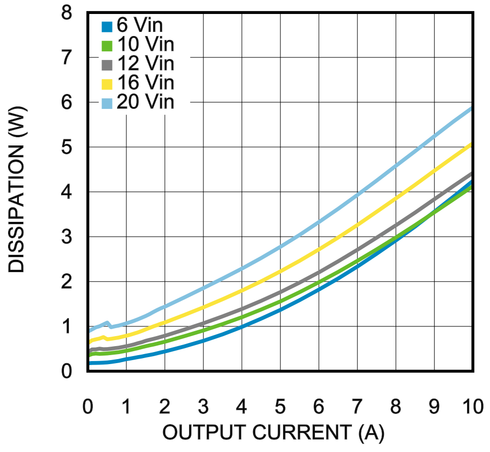
Dissipation 3.3V output @ 25°C



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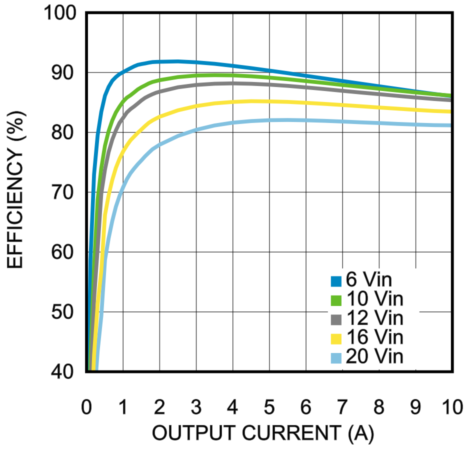
Efficiency 2.5V output @ 25°C



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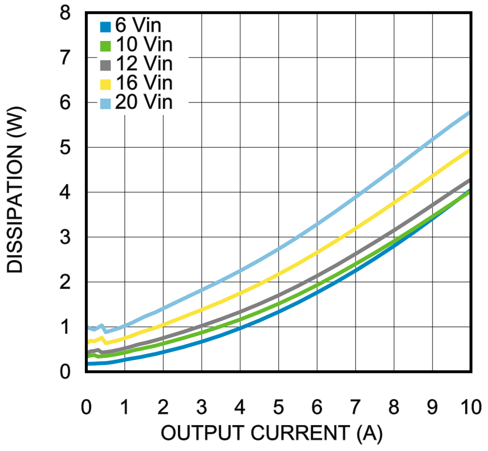
Dissipation 2.5V output @ 25°C



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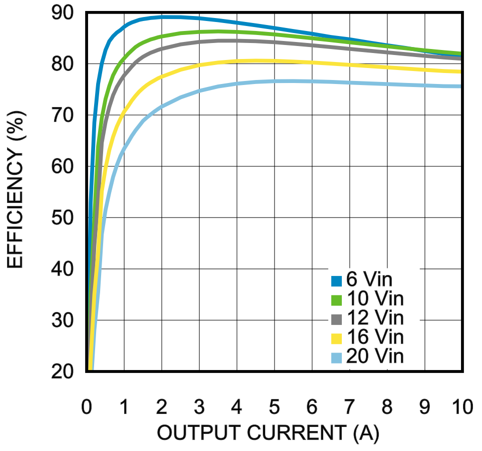
Efficiency 1.8V output @ 25°C



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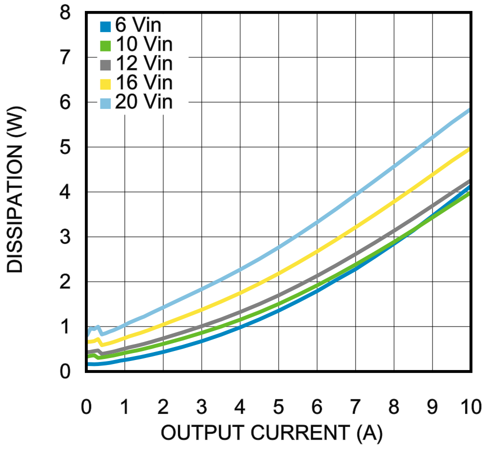
Dissipation 1.8V output @ 25°C



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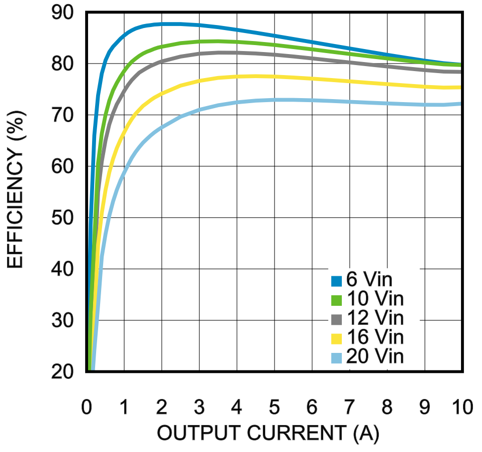
Efficiency 1.5V output @ 25°C



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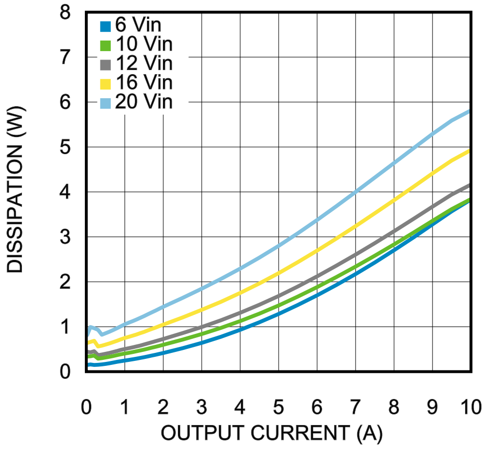
Dissipation 1.5V output @ 25°C



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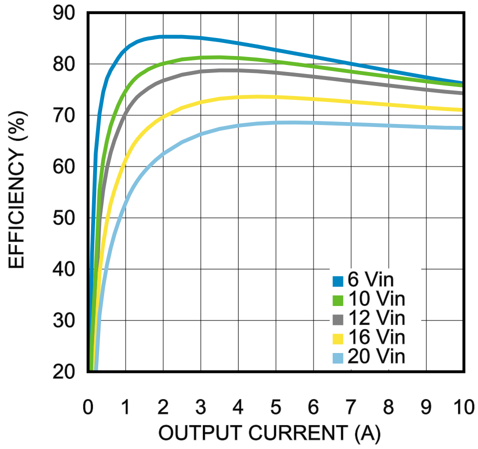
Efficiency 1.2V output @ 25°C



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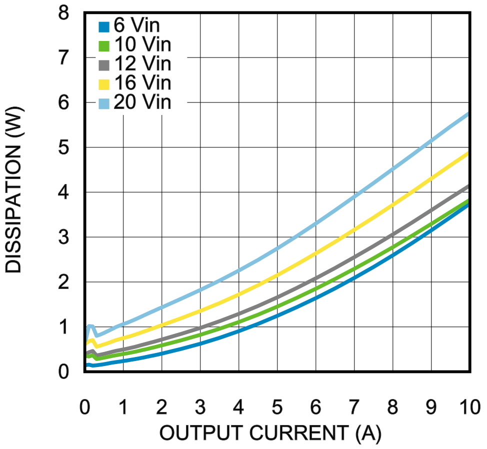
Dissipation 1.2V output @ 25°C



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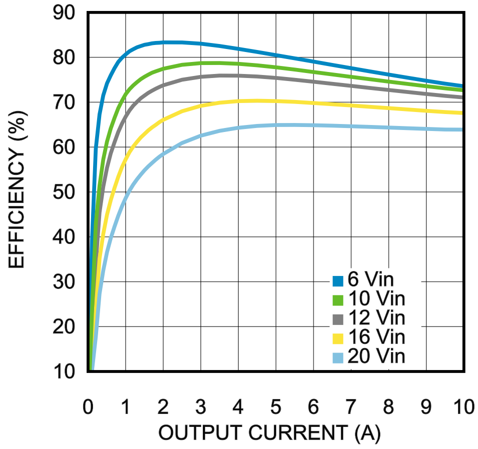
Efficiency 1.0V output @ 25°C



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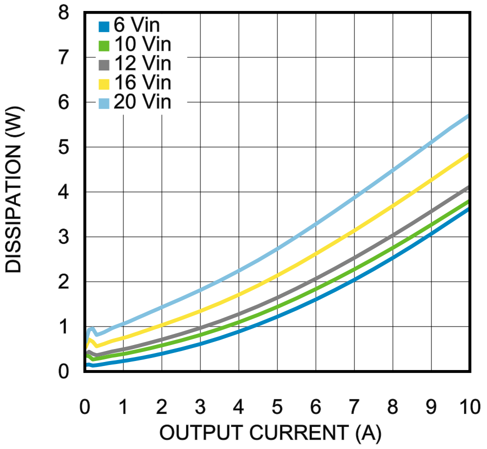
Dissipation 1.0V output @ 25°C



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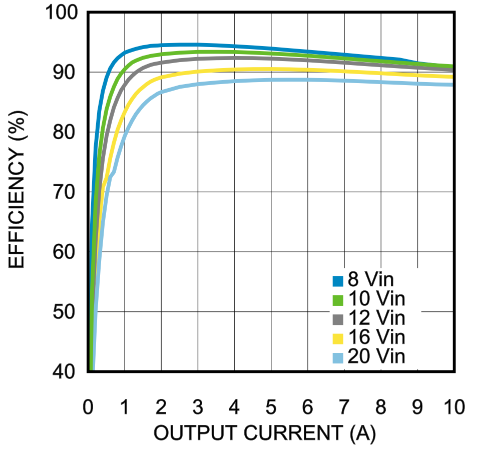
Efficiency 5.0V output @ 85°C



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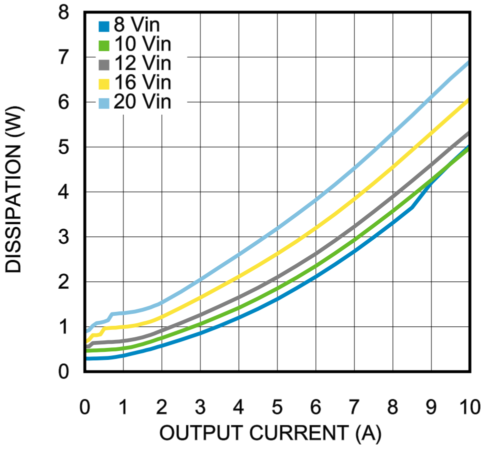
Dissipation 5.0V output @ 85°C



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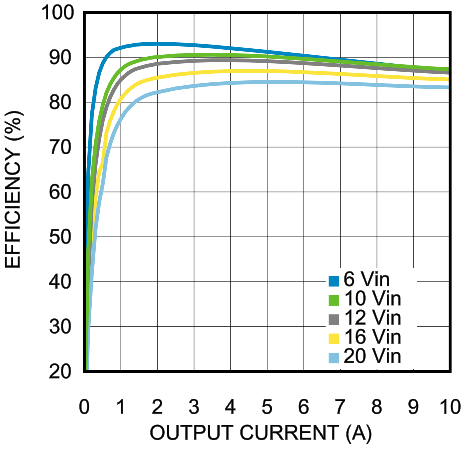

Efficiency 3.3V output @ 85°C

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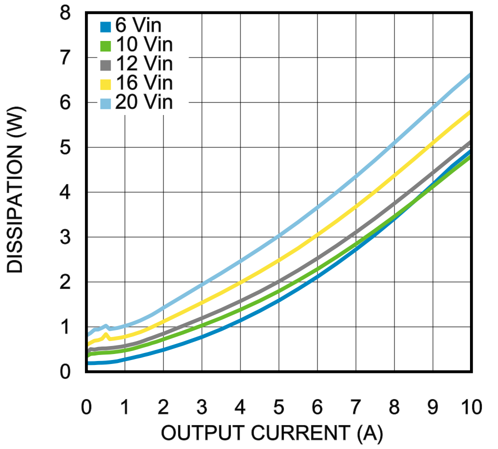

Dissipation 3.3V output @ 85°C

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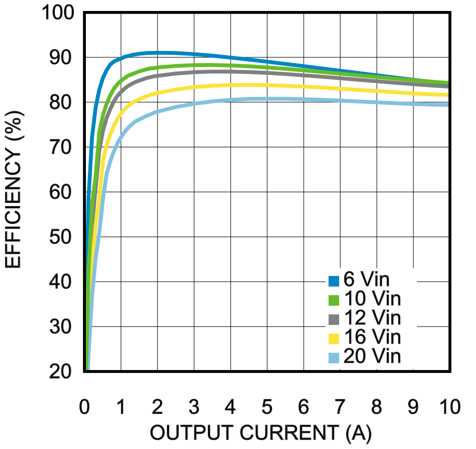

Efficiency 2.5V output @ 85°C

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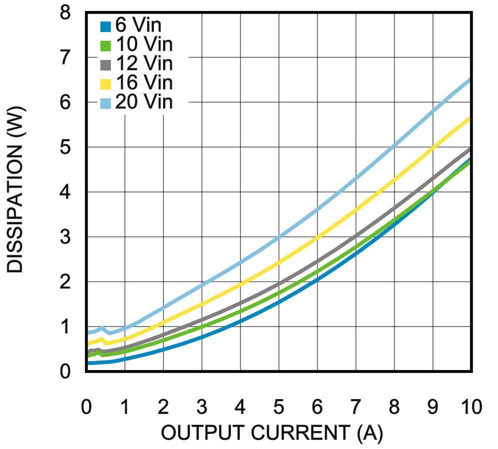

Dissipation 2.5V output @ 85°C

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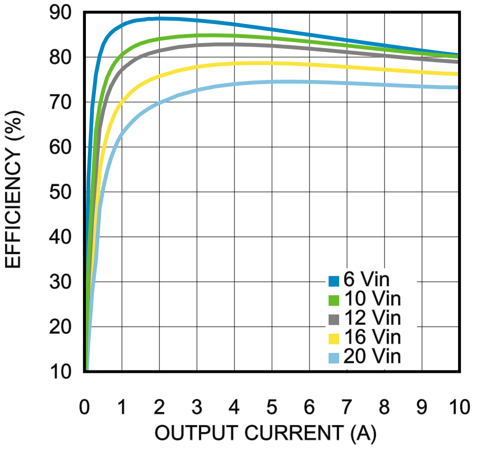

Efficiency 1.8V output @ 85°C

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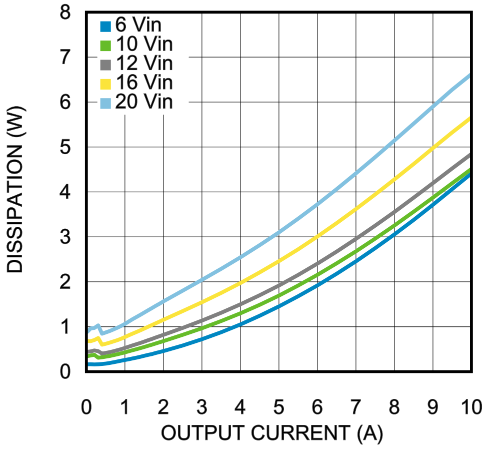

Dissipation 1.8V output @ 85°C

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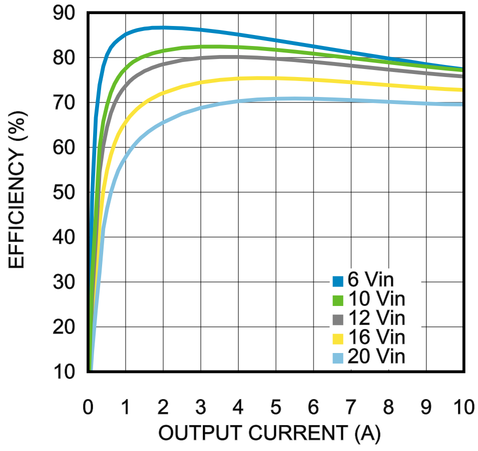
Efficiency 1.5V output @ 85°C



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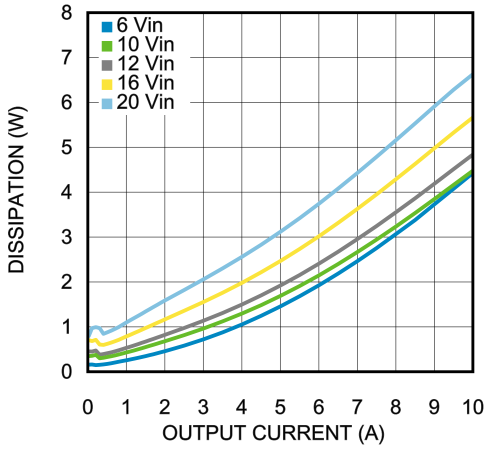
Dissipation 1.5V output @ 85°C



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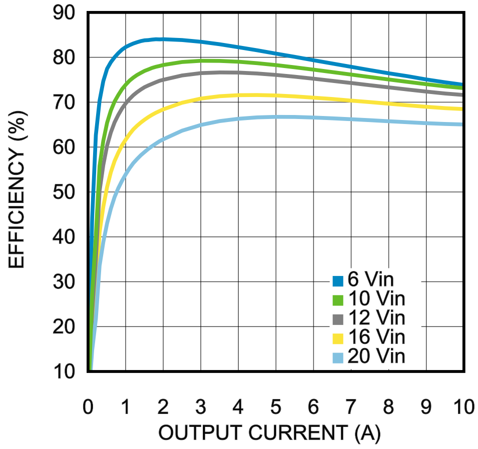
Efficiency 1.2V output @ 85°C



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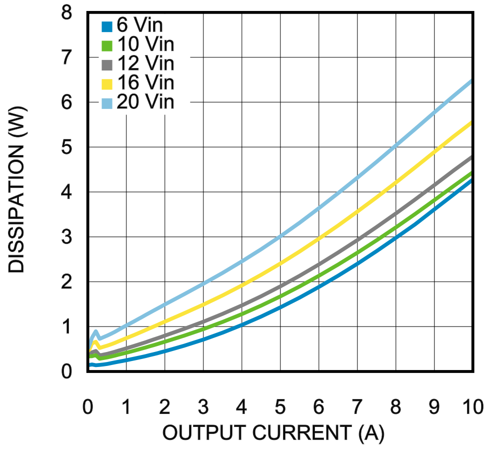
Dissipation 1.2V output @ 85°C



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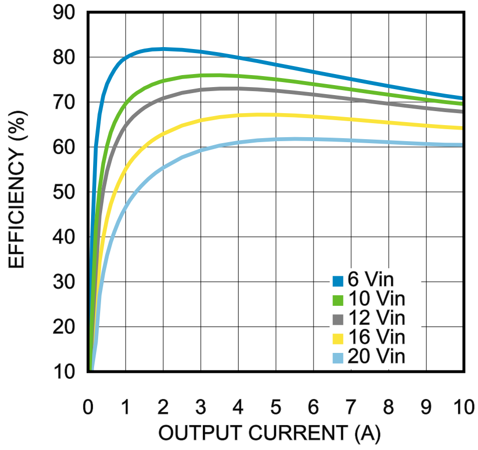
Efficiency 1.0V output @ 85°C



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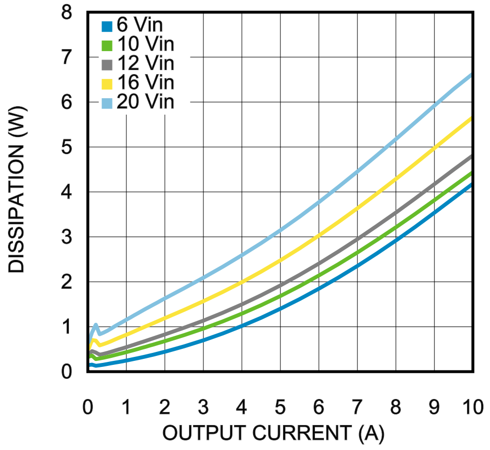
Dissipation 1.0V output @ 85°C



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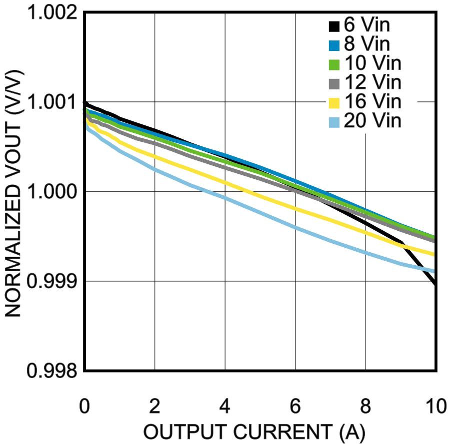
Normalized line and load regulation V_{OUT} = 3.3V



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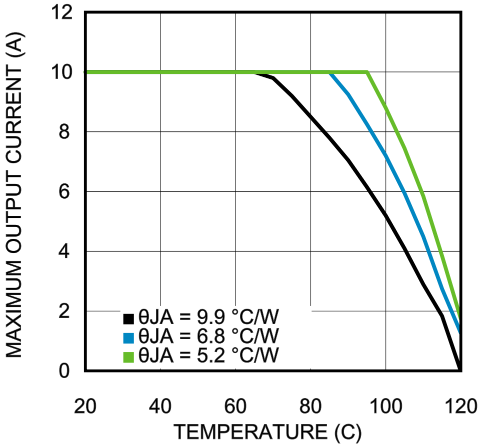
Thermal derating V_{IN} = 12V, V_{OUT} = 5.0V



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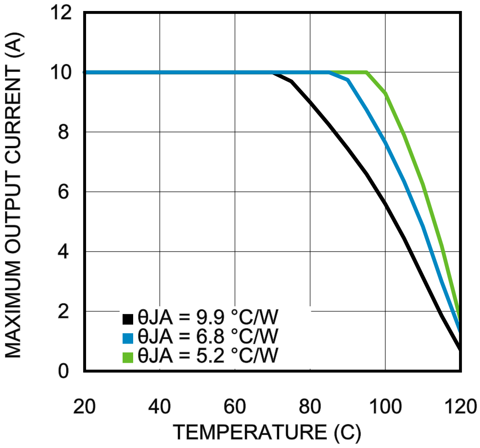
Thermal derating V_{IN} = 12V, V_{OUT} = 3.3V



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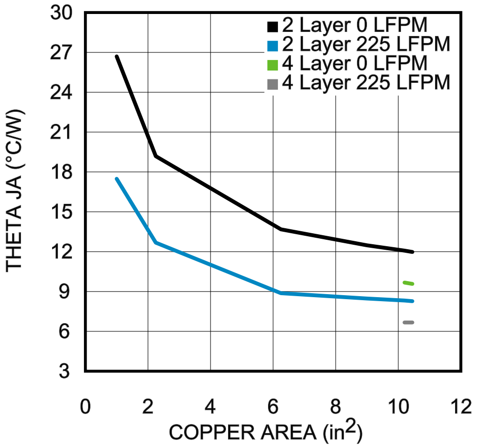
θ_{JA} vs copper heat sinking area



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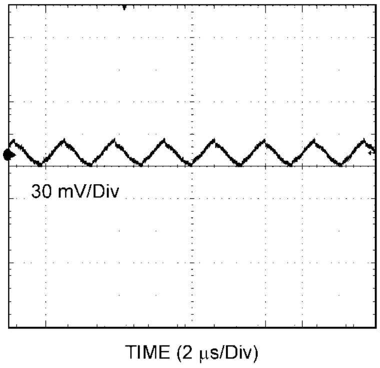
Output ripple
$12V_{IN}$, $5.0V_{OUT}$ @ Full Load, BW = 20 MHz



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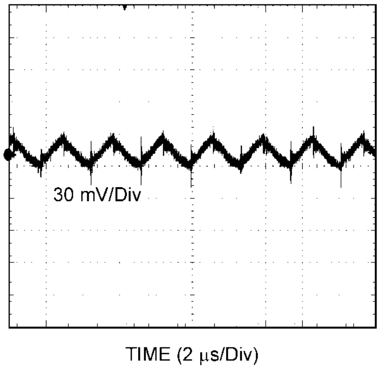
Output ripple
$12V_{IN}$, $5.0V_{OUT}$@ Full Load, BW = 250 MHz



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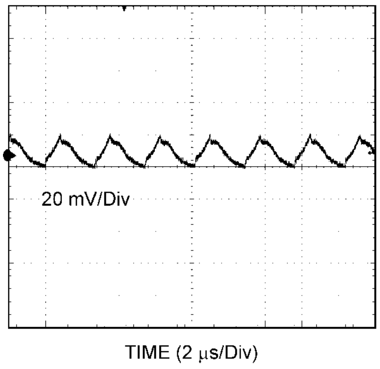
Output ripple
$12V_{IN}$, $3.3V_{OUT}$ @ Full Load, BW = 20 MHz

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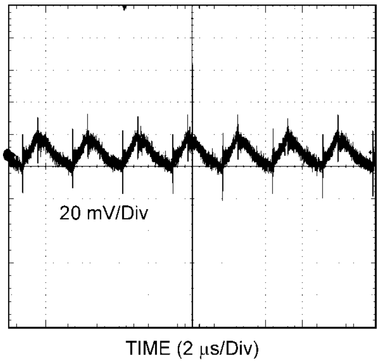
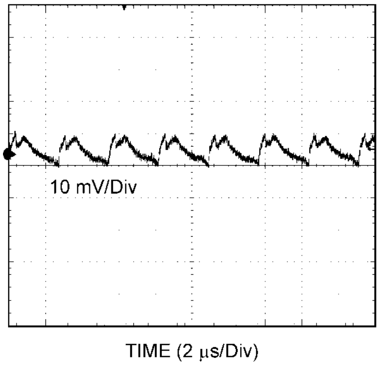

Output ripple
$12V_{IN}$, $3.3V_{OUT}$@ Full Load, BW = 250 MHz

30133170


Output ripple
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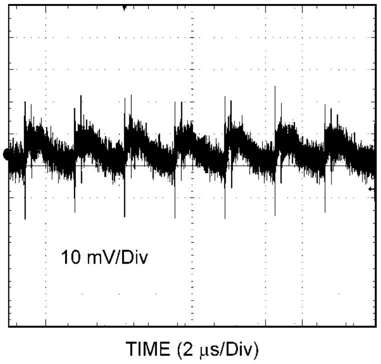
Output ripple
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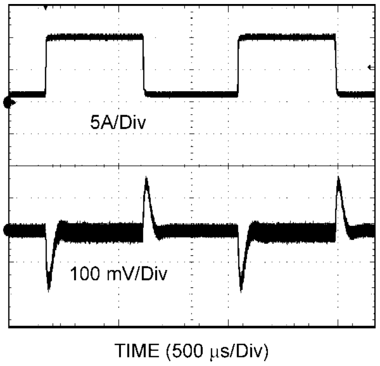
Transient response
$12V_{IN}$, $5.0V_{OUT}$ 1 to 10A Step

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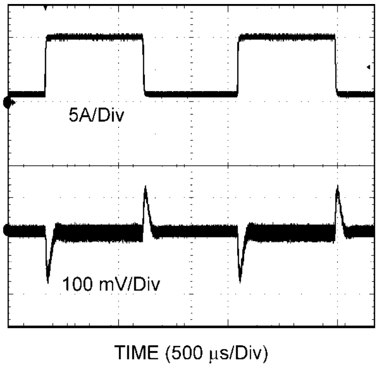
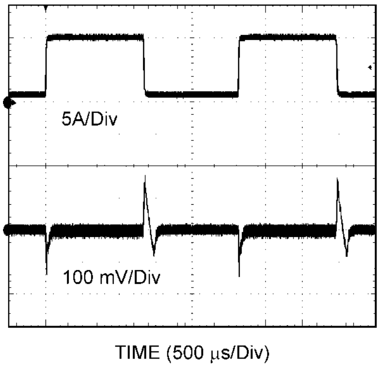

Transient response
$12V_{IN}$, $3.3V_{OUT}$ 1 to 10A Step

30133173

Transient response $12V_{IN}$, $1.2V_{OUT}$ 1 to 10A Step



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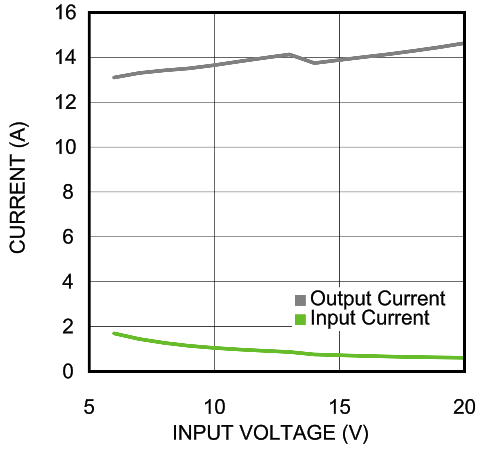
Short circuit current vs input voltage



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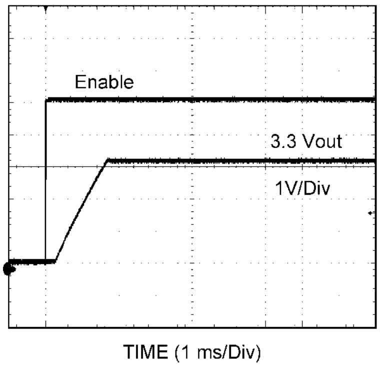
$3.3V_{OUT}$ Soft Start, no C_{SS}



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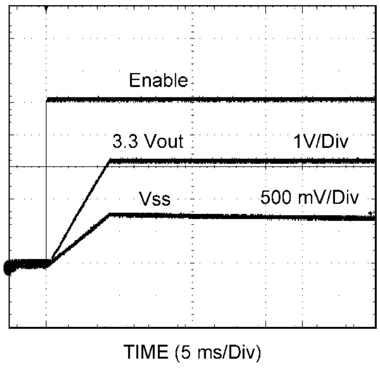
$3.3V_{OUT}$ Soft Start, C_{SS} = 0.47uF



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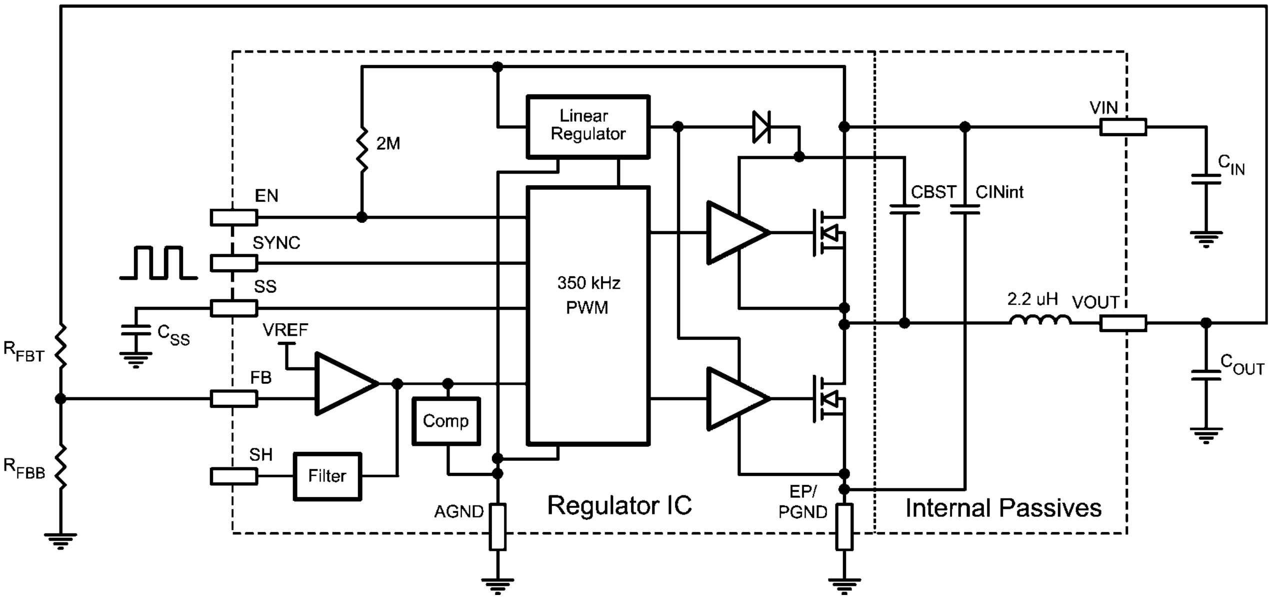
Block Diagram



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General Description

The LMZ22010 SIMPLE SWITCHER© power module is an easy-to-use step-down DC-DC solution capable of driving up to 10A load. The LMZ22010 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ22010 can accept an input voltage rail between 6V and 20V and deliver an adjustable and highly accurate output voltage as low as 0.8V. The LMZ22010 only requires two external resistors and external capacitors to complete the power solution. The LMZ22010 is a reliable and robust design with the following protection features: thermal shutdown, programmable input under-voltage lockout, output over-voltage protection, short-circuit protection, output current limit, and allows startup into a pre-biased output.

The sync input allows synchronization over the 314 to 600 kHz switching frequency range and up to 6 modules can be connected in parallel for higher load currents.

Design Steps for the LMZ22010 Application

The LMZ22010 is fully supported by Webench® which offers: component selection, electrical and thermal simulations. Additionally, there are both evaluation and demonstration boards that may be used as a starting point for design. The following list of steps can be used to manually design the LMZ22010 application.

All references to values refer to the typical applications schematic *Figure 5* .

- Select minimum operating V_{IN} with enable divider resistors
- Program V_{OUT} with FB resistor divider selection
- Select C_{OUT}
- Select C_{IN}
- Determine module power dissipation
- Layout PCB for required thermal performance

ENABLE DIVIDER, R_{ENT}, R_{ENB} AND R_{ENH}SELECTION

Internal to the module is a 2 mega ohm pull-up resistor connected from V_{IN} to Enable. For applications not requiring precision under voltage lock out (UVLO), the Enable input may be left open circuit and the internal resistor will always enable the module. In such case, the internal UVLO occurs typically at 4.3V (V_{IN} rising).

In applications with separate supervisory circuits Enable can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ22010 output rail.

Enable provides a precise 1.274V threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. Additionally there is 13 µA (typ) of switched offset current allowing programmable hysteresis. See *Figure 1*.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of a programmable UVLO. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.274\text{V}) - 1 \qquad (1)$$

The LMZ22010 typical application shows 12.7kΩ for R_{ENB} and 42.2kΩ for R_{ENT} resulting in a rising UVLO of 5.51V. Note that this divider presents 4.62V to the EN input when V_{IN} is raised to 20V. This upper voltage should always be checked, making sure that it never exceeds the Abs Max 5.5V limit for Enable. A 5.1V Zener clamp can be applied in cases where the upper voltage would exceed the EN input's range of operation. The zener clamp is not required if the target application prohibits the maximum Enable input voltage from being exceeded.

Additional enable voltage hysteresis can be added with the inclusion of R_{ENH}. It is possible to select values for R_{ENT} and R_{ENB} such that R_{ENH} is a value of zero allowing it to be omitted from the design.

Rising threshold can be calculated as follows:

$$V_{EN}(\text{rising}) = 1.274\ (\ 1 + (R_{ENT} || \ 2\ \text{meg}) / \ R_{ENB}) \qquad (2)$$

Whereas the falling threshold level can be calculated using:

$$V_{EN}(\text{falling}) = V_{EN}(\text{rising}) - 13\ \mu\text{A}\ (\ R_{ENT} || \ 2\ \text{meg}\ || \ R_{ENTB} + R_{ENH}\ ) \qquad (3)$$

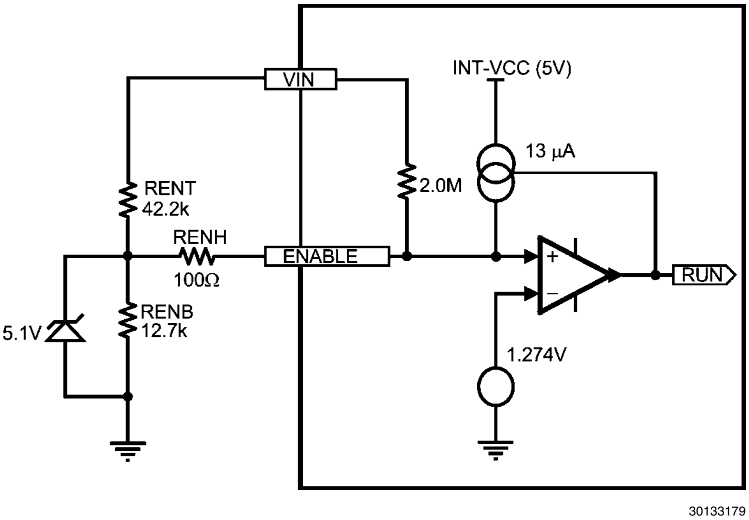

FIGURE 1. Enable input detail

OUTPUT VOLTAGE SELECTION

Output voltage is determined by a divider of two resistors connected between V_{OUT} and AGND. The midpoint of the divider is connected to the FB input.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_{OUT} = 0.795V * (1 + R_{FBT} / R_{FBB}) \quad (4)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_{OUT} / 0.795V) - 1 \quad (5)$$

These resistors should generally be chosen from values in the range of 1.0 kΩ to 10.0 kΩ.

For V_{OUT} = 0.8V the FB pin can be connected to the output directly and R_{FBB} can be set to 8.06kΩ to provide minimum output load.

A table of values for R_{FBT} , and R_{FBB}, is included in the simplified applications schematic on page 2.

SOFT-START CAPACITOR SELECTION

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time.

Upon turn-on, after all UVLO conditions have been passed, an internal 1.6msec circuit slowly ramps the SS input to implement internal soft start. If 1.6 msec is an adequate turn–on time then the Css capacitor can be left unpopulated. Longer soft-start periods are achieved by adding an external capacitor to this input.

Soft start duration is given by the formula:

$$t_{SS} = V_{REF} * C_{SS} / Iss = 0.795V * C_{SS} / 50uA \quad (6)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} * 50\mu A / 0.795V \quad (7)$$

Using a 0.22µF capacitor results in 3.5 msec typical soft-start duration; and 0.47µF results in 7.5 msec typical. 0.47 µF is a recommended initial value.

As the soft-start input exceeds 0.795V the output of the power stage will be in regulation and the 50 µA current is deactivated. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The Enable input being pulled low
- A thermal shutdown condition
- V_{IN} falling below 4.3V (TYP) and triggering the V_{CC} UVLO

TRACKING SUPPLY DIVIDER OPTION

The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3V system rail) where the slave module output voltage is lower than that of the master. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (i.e. <0.15V typ). The values for the tracking resistive divider should be selected such that the effect of the internal 50uA current source is minimized. In most cases the ratio of the tracking divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail be shorter than the master rail; a condition that is easy to satisfy since the C_{SS} cap is replaced by R_{TKB}. The tracking function is only supported for the power up interval of the master supply; once the SS/TRK rises past 0.795V the input is no longer enabled and the 50 uA internal current source is switched off.

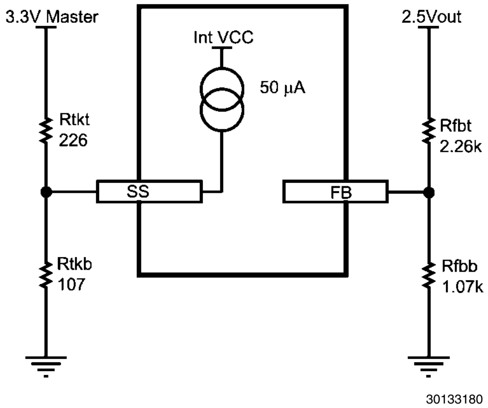

FIGURE 2. Tracking option input detail

C$_{OUT}$ SELECTION

None of the required C_{OUT} output capacitance is contained within the module. A minimum value ranging from 330 µF for $6V_{OUT}$ to 660 µF for $1.2V_{OUT}$ applications is required based on the values of internal compensation in the error amplifier. These minimum values can be decreased if the effective capacitor ESR is higher than 15 mOhms.

A Low ESR (15 mOhm) tantalum, organic semiconductor or specialty polymer capacitor types in parallel with a 47nF X7R ceramic capacitor for high frequency noise reduction is recommended for obtaining lowest ripple. The output capacitor C_{OUT} may consist of several capacitors in parallel placed in close proximity to the module. The output voltage ripple of the module depends on the equivalent series resistance (ESR) of the capacitor bank, and can be calculated by multiplying the ripple current of the module by the effective impedance of your chosen output capacitors (for ripple current calculation, see equation 18). Electrolytic capacitors will have large ESR and lead to larger output ripple than ceramic or polymer types. For this reason a combination of ceramic and polymer capacitors is recommended for low output ripple performance.

The output capacitor assembly must also meet the worst case ripple current rating of Δi_L, as calculated in equation ***(18)*** below. Loop response verification is also valuable to confirm closed loop behavior.

For applications with dynamic load steps; the following equation provides a good first pass approximation of C_{OUT} for load transient requirements.

$$C_{OUT} \geq \frac{I_{step}}{(\Delta V_{OUT} - I_{STEP} \text{ x } ESR) \text{ x } \left(\frac{f_{SW}}{V_{OUT}}\right)} \quad (8)$$

For $12V_{IN}$, $3.3V_{OUT}$, a transient voltage of 5% of V_{OUT} = 0.165V (ΔV_{OUT}), a 9A load step (I_{STEP}), an output capacitor effective ESR of 3 mOhms, and a switching frequency of 350kHz (f_{SW}):

$$C_{OUT} \geq \frac{9A}{(0.165V - 9A \text{ x } 0.003) \text{ x } \left(\frac{350e3}{3.3V}\right)}$$

$$\geq 615\ \mu F \quad (9)$$

Note that the stability requirement for minimum output capacitance must always be met.

One recommended output capacitor combination is two 330µF, 15 mOhm ESR tantalum polymer capacitors connected in parallel with a 47 uF 6.3V X5R ceramic. This combination provides excellent performance that may exceed the requirements of certain applications. Additionally some small 47nF ceramic capacitors can be used for high frequency EMI suppression.

C_{IN} SELECTION

The LMZ22010 module contains two internal ceramic input capacitors. Additional input capacitance is required external to the module to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. This input capacitance should be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I_{CIN\text{-}RMS} = I_{OUT} \times \sqrt{D(1\text{-}D)} \qquad (10)$$

where $D \cong V_{OUT} / V_{IN}$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_{OUT}$).

Recommended minimum input capacitance is 30 uF X7R (or X5R) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature derating of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this parameter.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) to be maintained then the following equation may be used.

$$C_{IN} \geq \frac{I_{OUT} \text{ x } D \text{ x } (1 - D)}{f_{SW} \text{ x } \Delta V_{IN}} \qquad (11)$$

If ΔV_{IN} is 200 mV or 1.66% of V_{IN} for a 12V input to 3.3V output application and f_{SW} = 350 kHz then:

$$C_{IN} \geq \frac{10\text{A x} \left(\frac{3.3\text{V}}{12\text{V}}\right) \text{x} \left(1 - \frac{3.3\text{V}}{12\text{V}}\right)}{350 \text{ kHz x } 200 \text{ mV}} \geq 28 \ \mu\text{F} \qquad (12)$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines. The LMZ22010 typical applications schematic and evaluation board include a 150 µF 50V aluminum capacitor for this function. There are many situations where this capacitor is not necessary.

POWER DISSIPATION AND BOARD THERMAL REQUIREMENTS

When calculating module dissipation use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in the characteristic curves such that less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

For the design case of V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 10A, and $T_{A\text{-}MAX}$ = 50°C, the module must see a thermal resistance from case to ambient (θ_{CA}) of less than:

$$\theta_{CA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC\_LOSS}} - \theta_{JC} \qquad (13)$$

Given the typical thermal resistance from junction to case (θ_{JC}) to be 1.0 °C/W. Use the 85°C power dissipation curves in the Typical Performance Characteristics section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 5.3W.

$$\theta_{CA} < \frac{125°\text{C} - 50°\text{C}}{5.3 \text{ W}} - 1.0 \ \frac{°\text{C}}{\text{W}} < 13.15 \ \frac{°\text{C}}{\text{W}} \qquad (14)$$

To reach θ_{CA} = 13.15, the PCB is required to dissipate heat effectively. With no airflow and no external heat-sink, a good estimate of the required board area covered by 2 oz. copper on both the top and bottom metal layers is:

$$\text{Board Area\_cm}^2 \geq \frac{500}{\theta_{CA}} \cdot \frac{°\text{C x cm}^2}{\text{W}} \qquad (15)$$

As a result, approximately 38.02 square cm of 2 oz copper on top and bottom layers is the minimum required area for the example PCB design. This is 6.16 x 6.16 cm (2.42 x 2.42 in) square. The PCB copper heat sink must be connected to the exposed pad. For best performance, use approximately 100, 12mil (305 µm) thermal vias spaced 59 mil (1.5 mm) apart connect the top copper to the bottom copper.

Another way to estimate the temperature rise of a design is using θ_{JA}. An estimate of θ_{JA} for varying heat sinking copper areas and airflows can be found in the typical applications curves. If our design required the same operating conditions as before but had 225 LFPM of airflow. We locate the required θ_{JA} of

$$\theta_{JA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC\_LOSS}}$$

$$\theta_{JA} < \frac{(125 - 50) \ °\text{C}}{5.3 \text{ W}} < 14.15 \ \frac{°\text{C}}{\text{W}} \qquad (16)$$

On the Theta JA vs copper heatsinking curve, the copper area required for this application is now only 2 square inches. The airflow reduced the required heat sinking area by a factor of three.

To reduce the heat sinking copper area further, this package is compatable with D3-PAK surface mount heat sinks.

For an example of a high thermal performance PCB layout for SIMPLE SWITCHER© power modules, refer to AN-2093, AN-2084, AN-2125, AN-2020 and AN-2026.

PC BOARD LAYOUT GUIDELINES

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules. A good layout example is shown in *Figure 6*

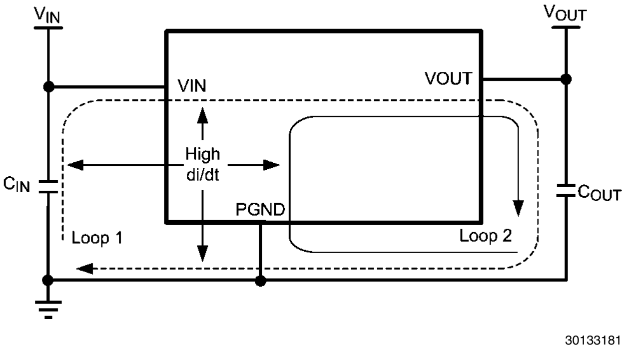

FIGURE 3. High Current Loops

1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout as shown in the figure above. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (C_{IN}) is placed at a distance away from the LMZ22010. Therefore place C_{IN} as close as possible to the LMZ22010 VIN and PGND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Additionally provide a single point ground connection from pin 4 (AGND) to EP/ PGND.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB} should be routed away from the body of the LMZ22010 to minimize possible noise pickup.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. For best results use a 10 x 10 via array or larger with a minimum via diameter of 12mil (305 µm) thermal vias spaced 46.8mil (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

Additional Features

SYNCHRONIZATION INPUT

The PWM switching frequency can be synchronized to an external frequency source. The PWM switching will be in phase with the external frequency source. If this feature is not used, connect this input either directly to ground, or connect to ground through a resistor of 1.5 kΩ ohm or less. The allowed synchronization frequency range is 314 kHz to 600 kHz. The typical input threshold is 1.4V. Ideally, the input clock should overdrive the threshold by a factor of 2, so direct drive from 3.3V logic via a 1.5kΩ or less Thevenin source resistance is recommended. Note that applying a sustained “logic 1” corresponds to zero Hz PWM frequency and will cause the module to stop switching.

CURRENT SHARING

When a load current higher than 10A is required by the application, the LMZ22010 can be configured to share the load between multiple devices. To share the load current between the devices, connect the SH pin of all current sharing LMZ22010 modules. One device should be configured as the master by connecting FB normally. All other devices should be configured as slaves by leaving their respective FB pins floating. The modules should be synchronized by a clock signal to avoid beat frequencies in the output voltage caused by small differences in the internal 359 kHz clock. If the modules are not synchronized, the magnitude of the ripple voltage will depend on the phase relationship of the internal clocks. The external synchronizing clocks can be in phase for all modules, or out of phase to reduce the current stress on the input and output capacitors. As an example, two modules can be run 180 degrees out of phase, and three modules can be run 120 degrees out of phase. The VIN, VOUT, PGND, and AGND pins should also be connected with low impedance paths. It is particularly important to pay close attention to the layout of AGND and SH, as offsets in grounding or noise picked up from other devices will be seen as a mismatch in current sharing and could cause noise issues.

Current sharing modules can be configured to share the same set of bulk input and output capacitors, while each having their own local input and output bypass capacitors. A C_{IN_BYP} >= 30uF is still recommended for each module that is connected in a current sharing configuration. A C_{OUT_BYP} consisting of 47nF X7R ceramic capacitor in parallel with a 22µF ceramic capacitor is recommended to locally bypass the output voltage for each module. These capacitors will provide local bypassing of high frequency switched currents.

In a current sharing system using two or more modules, the slaves have their error amp circuitry disconnected. The master over-rides the error amplifier outputs of the slaves. This signal is then compared to each module’s individual current sense circuitry. Due to this, the current sense gain of the entire system increases according to the number of modules slaved to the master. To compensate for this and ensure good stability, the total output capacitance has to be increased. For example, two modules configured to provide 1.2V_{OUT} and 20 amps have a required total bulk output capacitance of C_{OUT_BULK} = 2 x 450µF (ESR 25mOhms). This is a thirty six percent increase in the required output capacitance of a stand alone module. Up to 6 modules can be connected in parallel for loads up to 60A. For more information on current sharing refer to AN-2093 (Current sharing evaluation board).

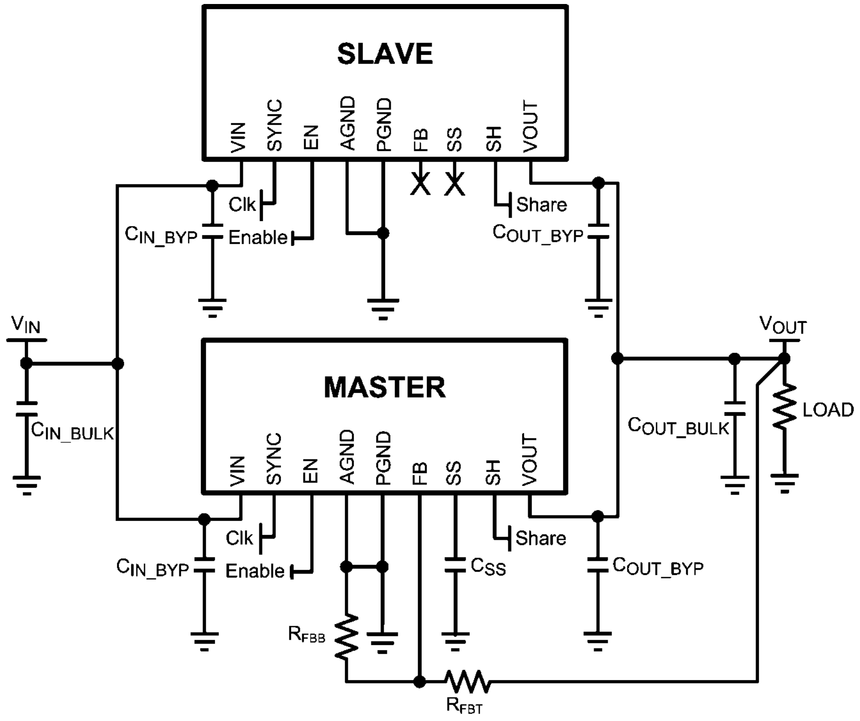

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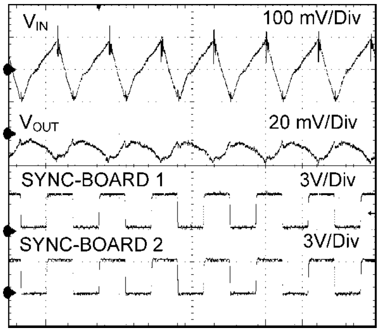
FIGURE 4. Current Sharing Example Schematic

Output voltage ripple of two modules with synchronization clocks in phase



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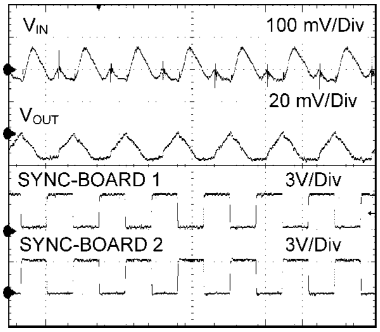
Output voltage ripple of two modules with synchronization clocks 180 degrees out of phase



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OUTPUT OVER-VOLTAGE PROTECTION

If the voltage at FB is greater than a 0.86V internal reference, the output of the error amplifier is pulled toward ground, causing V_{OUT} to fall.

CURRENT LIMIT

The LMZ22010 is protected by both low side (LS) and high side (HS) current limit circuitry. The LS current limit detection is carried out during the off-time by monitoring the current through the LS synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 13A (typical) the current limit comparator disables the start of the next switching period. Switching cycles are prohibited until current drops below the limit. It should also be noted that d.c. current limit is dependent on duty cycle as illustrated in the graph in the typical performance section. The HS current limit monitors the current of top side MOSFET. Once HS current limit is detected (16A typical) , the HS MOSFET is shutoff immediately, until the next cycle. Exceeding HS current limit causes V_{OUT} to fall. Typical behavior of exceeding LS current limit is that f_{SW} drops to 1/2 of the operating frequency.

THERMAL PROTECTION

The junction temperature of the LMZ22010 should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 150 °C (typ Hyst =

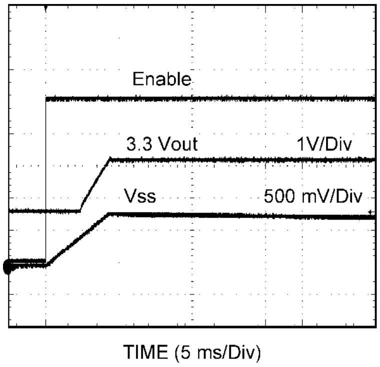
15°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

PRE-BIASED STARTUP

The LMZ22010 will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The following scope capture shows proper behavior in this mode. Trace one is Enable going high. Trace two is 1.8V pre-bias rising to 3.3V. Trace three is the SS voltage with a C_{SS}= 0.47uF. Risetime determined by C_{SS}.

Pre-Biased Startup



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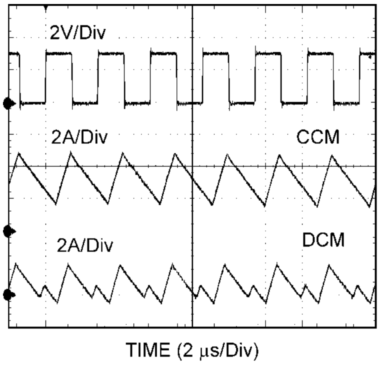
DISCONTINUOUS CONDUCTION AND CONTINUOUS CONDUCTION MODES

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM, inductor current is maintained to an average value equaling Iout . In DCM the low-side switch will turn off when the inductor current falls to zero, this causes the inductor current to resonate. Although it is in DCM, the current is allowed to go slightly negative to charge the bootstrap capacitor.

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time.

Following is a comparison pair of waveforms showing both the CCM (upper) and DCM operating modes.

CCM and DCM Operating Modes
V_{IN} = 12V, V_O = 3.3V, I_O = 3A/0.3A



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The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \qquad (17)$$

The inductor internal to the module is 2.2 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (Δi_L). Δi_L can be calculated with:

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \qquad (18)$$

Where V_{IN} is the maximum input voltage and f_{SW} is typically 359 kHz.

If the output current I_{OUT} is determined by assuming that $I_{OUT} = I_L$, the higher and lower peak of Δi_L can be determined.

Typical Application Schematic Diagram and BOM

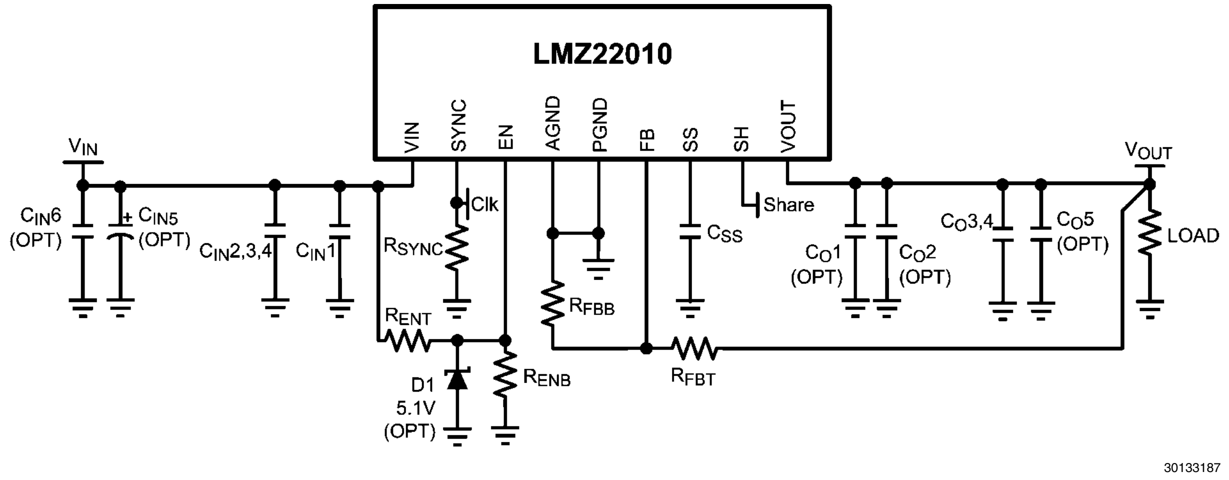
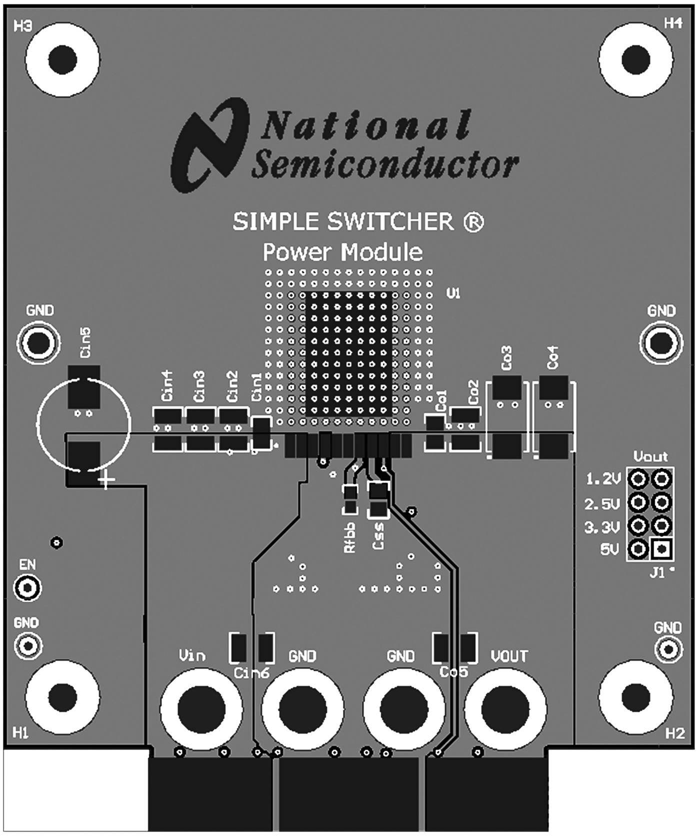


FIGURE 5.

Typical Application Bill of Materials — Table 1

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	SIMPLE SWITCHER ®	TO-PMOD-11	National Semiconductor	LMZ22010TZ
C_{IN}1,6 (OPT)	0.047 µF, 50V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_{IN}2,3,4	10 µF, 50V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{IN}5 (OPT)	CAP, AL, 150µF, 50V	Radial G	Panasonic	EEE-FK1H151P
C_O1,5 (OPT)	0.047 µF, 50V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_O2 (OPT)	47 µF, 10V, X7R	1210	Murata	GRM32ER61A476KE20L
C_O3,4	330 µF, 6.3V, 0.015 ohm	CAPSMT_6_UE	Kemet	T520D337M006ATE015
R_{FBT}	3.32 kΩ	0805	Panasonic	ERJ-6ENF3321V
R_{FBB}	1.07 kΩ	0805	Panasonic	ERJ-6ENF1071V
R_{SYNC}	1.50 kΩ	0805	Vishay Dale	CRCW08051K50FKEA
R_{ENT}	42.2 kΩ	0805	Panasonic	ERJ-6ENF4222V
R_{ENB}	12.7 kΩ	0805	Panasonic	ERJ-6ENF1272V
C_{SS}	0.47 µF, ±10%, X7R, 16V	0805	AVX	0805YC474KAT2A
D1 (OPT)	5.1V, 0.5W	SOD-123	Diodes Inc.	MMSZ5231BS-7-F



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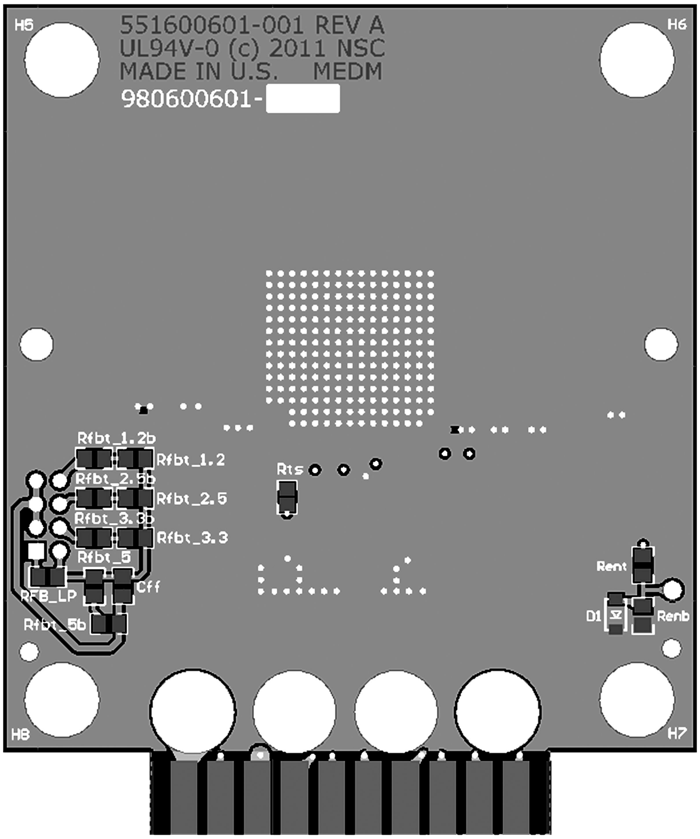

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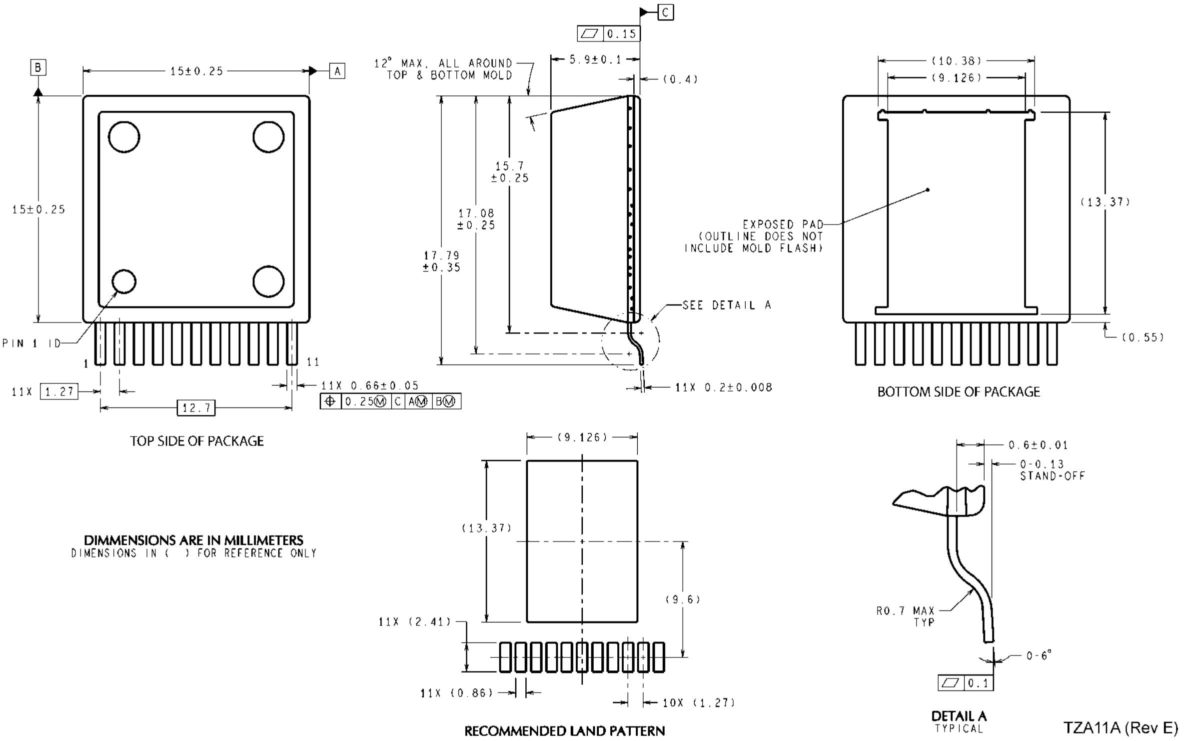
FIGURE 6. Layout example

Physical Dimensions inches (millimeters) unless otherwise noted



11-Lead TZA Package
NS Package Number TZA11A

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