LM4854 Boomer® Audio Power Amplifier Series 1.9W Monaural, 85mW Stereo Headphone Audio Amplifier

Check for Samples: LM4854

FEATURES

- **Fast 0.1ms (typ) and 1.0ms (max) turn-on and turn-off time**
- **Eliminates SE amplifier output coupling capacitors**
- **Advanced "click and pop" suppression circuitry**
- **Stereo headphone amplifier mode**
- **Low-power standby and ultra-low current micropower shutdown modes**
- **Thermal shutdown protection circuitry**
- **2.4V to 5.5V operation**
- **Unity-gain stable**
- **Gain set with external resistors**
- **Space-saving micro SMD package, exposed-DAP LLP, and TSSOP**

APPLICATIONS

- **PDAs**
- **Notebook computers**
- **Cellular phones**
- **Handheld portable electronic devices**

DESCRIPTION

The unity-gain stable LM4854 is both a mono differential output (for bridge-tied loads, or BTL) audio power amplifier and a single-ended (SE) stereo headphone amplifier. Operating on a single 5V supply, the mono BTL mode delivers 1.1W (typ) to an 8Ω load, 1.7W (typ) to a 4Ω load (Note 1) at 1% THD+N. In SE stereo mode, the amplifier will deliver 85mW to 32Ω loads. The LM4854 features a new circuit topology that suppresses output transients ('click and pops') and eliminates SE-mode output coupling capacitors, saving both component and board space costs. The LM4854 has three inputs: one pair for a two-channel stereo signal and the third for a single-channel mono input.

The LM4854 is designed for PDA, cellular telephone, notebook, and other handheld portable applications. It delivers high quality output power from a surface-mount package and requires few external components. Other features include an active-low micropower shutdown mode, an "instant-on" low power standby mode, and thermal shutdown protection.

The LM4854 is available in the very space-efficient 12-lead micro SMD, exposed-DAP LLP for higher power applications, and TSSOP packages.

NOTE

An LM4854LD that has been properly mounted to a circuit board will deliver 1.7W (typ) into a 4Ω load.

Table 1. Key Specifications

		VALUE	UNIT
LLP BTL output power (R_L = 3.2Ω and THD+N = 1%)	V_{DD} = 3.0V	1.0	W (typ)
	V_{DD} = 5.0V	1.9	W (typ)
LLP BTL output power (R_L = 4Ω and THD+N = 1%)	V_{DD} = 3.0V	900	mW (typ)
	V_{DD} = 5.0V	1.7	W (typ)
LLP BTL output power (R_L = 8Ω and THD+N = 1%)	V_{DD} = 3.0V	380	mW (typ)
	V_{DD} = 5.0V	1.1	W (typ)
SE output power (R_L = 32Ω and THD+N = 1.0%)	V_{DD} = 3.0V	32	mW (typ)
	V_{DD} = 5.0V	93	mW (typ)

Table 1. Key Specifications (continued)

		VALUE	UNIT
Micropower shutdown supply current	V_{DD} = 3.0V	0.005	µA (typ)
	V_{DD} = 5.0V	0.05	µA (typ)
Standby supply current	V_{DD} = 3.0V	16	µA (typ)
	V_{DD} = 5.0V	27	µA (typ)
PSRR (f = 1kHz, 3.0V ≤ V_{DD} ≤ 5.0V, Figure 1)	BTL	60	dB (typ)
	SE	66	dB (typ)

Typical Application

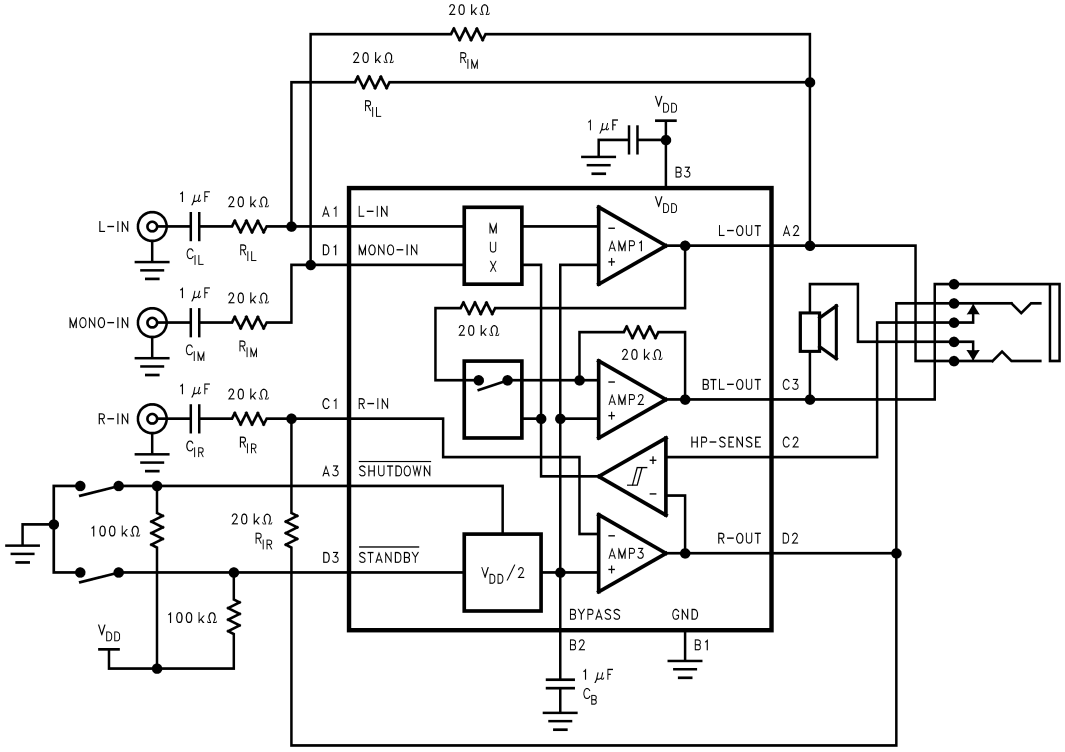

Figure 1. Typical Audio Amplifier Application Circuit

(Pin out shown for the 12-pin large bump micro SMD IBL package. Consult the "Connection Diagrams" for the LLP or MT package pin out.)

Connection Diagram

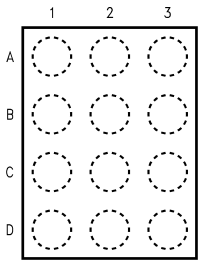

Figure 2. Top View (Bump-side down)

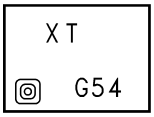

Figure 3. Micro SMD Marking (Top View)
X - Date Code
T - Die Traceability
G - Boomer Family
54 - LM4854IBL

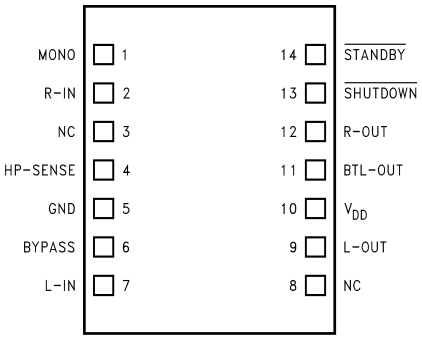

Figure 4. Top View

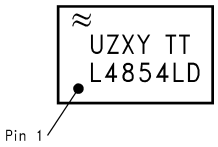

Figure 5. Top View
U - Fab Code
Z - Plant Code
XY - Date Code
TT - Die Tracebility
Bottom Line - Part Number

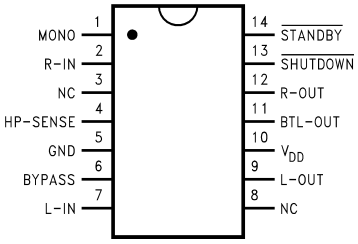

Figure 6. Top View

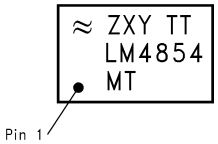

Figure 7. Top View
Z - Plant Code
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number

Table 2. LM4854IBL Pin Designation

Pin (Bump) Number	Pin Function
A1	L-IN
B1	GND
C1	R-IN
D1	MONO-IN
A2	L-OUT
B2	BYPASS
C2	HP-SENSE
D2	R-OUT
A3	$\overline{\text{SHUTDOWN}}$
B3	V_{DD}
C3	BTL-OUT
D3	$\overline{\text{STANDBY}}$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (3)	Internally Limited
ESD Susceptibility (4)	
All pins except Pin C3 (IBL), Pin11 (LD/MT)	2000V
Pin C3 (IBL), Pin 11 (LD/MT)	8000V
ESD Susceptibility (5)	200V
Junction Temperature (T_J)	150°C
Solder Information	
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
See AN-540 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface-mount devices.	
Thermal Resistance	
θ_{JA} (typ)—BLA12BAB	121°C/W
θ_{JC} (typ)—LDA14A	3°C/W
θ_{JA} (typ)—LDA14A	42°C/W (6)
θ_{JC} (typ)—MTC14	40°C/W
θ_{JA} (typ)—MTC14	109°C/W

(1) All voltages are measured with respect to the GND pin unless other wise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4854, see power derating currents for more information.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF-240pF discharged through all pins.
(6) The given θ_{JA} is for an LM4854 packaged in an LDA14A with the Exposed-DAP soldered to an exposed 2in2 area of 1oz printed circuit board copper.

Operating Ratings (1)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	$2.4V \le V_{DD} \le 5.5V$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Electrical Characteristics for Entire Amplifier (V_{DD} = 5V)

The following specifications apply for circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4854		Units (Limits)
			Typical (1)	Limit (2) (3)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V; I_O = 0A, No Load	5.0	12	mA max)
		V_{IN} = 0V; I_O = 0A, 8Ω Load	6.5	15	mA (max)
I_{STBY}	Standby Quiescent Power Supply Current	$V_{STANDBY}$ = GND	27	35	µA (max)
I_{SD}	Shutdown Quiescent Power Supply Current	$V_{SHUTDOWN}$ = GND	0.05	0.2	µA (max)
V_{OS}	Output Offset Voltage	8Ω Load	2.0	40	mV (max)
PSRR	Power Supply Rejection Ratio	C_{BYPASS} = 1.0µF, R_{SOURCE} = 10Ω V_{RIPPLE} = 200mV_{p-p} sinewave BTL, R_L = 8Ω, R_{IN} = 10Ω f_{IN} = 217Hz f_{IN} = 1kHz	 61 63		 dB dB
		SE, R_L = 32Ω, R_{IN} = 10Ω f_{IN} = 217Hz f_{IN} = 1kHz	 68 71		 dB dB
t_{RSH}	Return-from-Shutdown Time	C_{BYPASS} = 1.0µF	200		ms
t_{RST}	Return-from-Standby Time		0.1	1.0	ms(max)
V_{IH}	Shutdown or Standby Logic High Treshold			1.4	V (min)
V_{IL}	Shutdown or Standby Logic Low Treshold			0.4	V (max)

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) Datasheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.

Electrical Characteristics Bridged-Mode Operation (V_{DD} = 5V)

The following specifications apply for for the circuit shown in Figure 1 and a measurement bandwith of 20Hz to 80kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4854		Units (Limits)
			Typical (1)	Limit (2) (3)	
P_O	Output Power (Note 11)	THD = 1% (max); f = 1kHz (Note12)			
		R_L = 3.2Ω (LM4854LD)	1.9		W
		R_L = 4Ω (LM4854LD)	1.7		W
		R_L = 8Ω	1.1	1.0	W (min)
		THD = 10% (max); f = 1kHz (Note12)			
		R_L = 3.2Ω (LM4854LD)	2.3		W
		R_L = 4Ω (LM4854LD)	2.1		W
		R_L = 8Ω	1.3		W
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f_{IN} ≤ 20kHz			
		R_L = 4Ω, P_O = 1.0W (LM4854LD)	0.3		%
		R_L = 8Ω, P_O = 400mW	0.18		%
		f_{IN} = 1kHz			
		R_L = 4Ω, P_O = 1.5W (LM4854LD)	0.1		%
		R_L = 8Ω, P_O = 50mW	0.08		%
S/N	Signal-to-Noise Ratio	f_{IN} = 1kHz, C_{BYPASS} = 1.0µF			
		P_O = 900mW, R_L = 8Ω	90		dB

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) Datasheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.

Electrical Characteristics : SE Operation (V_{DD} = 5V)

The following specifications apply for for the circuit shown in Figure 1 and a measurement bandwith of 20Hz to 80kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4854		Units (Limits)
			Typical (1)	Limit (2) (3)	
P_O	Output Power (Note 11)	THD+N = 1.0%, f = 1kHz, R_L = 32Ω THD+N = 10%, f = 1kHz, R_L = 32Ω THD+N = 1.0%, f = 1kHz, R_L = 16Ω THD+N = 10%, f = 1kHz, R_L = 16Ω	93 105 170 200	85 140 	mW(min) mW mW(min) mW
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f_{IN} ≤ 20kHz R_L = 32Ω, P_O = 50mW	0.3		%
VOUT	Output Voltage Swing	THD = 1.0%, R_L = 5kΩ	4.0		V_{P-P}
XTALK	Channel Separation	f_{IN} = 1kHz, C_{BYPASS} = 1.0µF, R_L = 32Ω	55		dB
S/N	Signal-to-Noise Ratio	f_{IN} = 1kHz, C_{BYPASS} = 1.0µF P_O = 50mW, R_L = 32Ω	90		dB

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) Datasheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.

Electrical Characteristics for Entire Amplifier (V_{DD} = 3.0V)

The following specifications apply for circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4854		Units (Limits)
			Typical (1)	Limit (2) (3)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, 8Ω Load	4.0	10	mA (max)
I_{STBY}	Standby Quiescent Power Supply Current	$V_{STANDBY}$ = GND	16.0	20.0	µA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.005	0.02	µA (max)
V_{OS}	Output Offset Voltage	8 Ω Load	2.0	40	mV (max)
PSRR	Power Supply Rejection Ratio	C_{BYPASS} = 1.0µF, R_{SOURCE} = 10Ω V_{RIPPLE} = 200mV_{p-p} sinewave BTL, R_L = 8Ω, R_{IN} = 10Ω f_{IN} = 217Hz f_{IN} = 1kHz SE, R_L = 32Ω, R_{IN} = 10Ω f_{IN} = 217Hz f_{IN} = 1kHz	 62 62 68 72		 dB dB dB dB
t_{RSH}	Return-from-Shutdown Time	C_{BYPASS} = 1.0µF	200		ms
t_{RST}	Return-from-Standby Time		0.1	1.0	ms(max)
V_{IH}	Shutdown or Standby Logic High Treshold			1.4	V (min)
V_{IL}	Shutdown or Standby Logic Low Treshold			0.4	V (max)

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) Datasheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.

Electrical Characteristics : Bridged-Mode Operation (V_{DD} = 3.0V) (1) (2)

The following specifications apply for for the circuit shown in Figure 1 and a measurement bandwith of 20Hz to 80kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4854		Units (Limits)
			Typical (3)	Limit (2) (4)	
P_O	Output Power (Note11)	THD = 1% (max); f = 1kHz (Note11) R_L = 4Ω (LM4854LD) R_L = 8Ω	 1.0 380	 350	 W mW (min)
		THD = 10% (max); f = 1kHz (Note11) R_L = 4Ω (LM4854LD) R_L = 8Ω	 1.1 530		 W mW
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f_{IN} ≤ 20kHz R_L = 4Ω, P_O = 800mW (LM4854LD) R_L = 8Ω, P_O = 150mW	 0.3 0.21		 % %
		f_{IN} = 1kHz R_L = 4Ω, P_O = 500mW (LM4854LD) R_L = 8Ω, P_O = 150mW	 0.1 0.075		 % %
S/N	Signal-to-Noise Ratio	f_{IN} = 1kHz, C_{BYPASS} = 1.0µF P_O = 900mW, R_L = 8Ω	 90		 dB

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4854, see power derating currents for more information.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.

Electrical Characteristics : SE Operation (V_{DD} = 3.0V) (1) (2)

The following specifications apply for for the circuit shown in Figure 1 and a measurement bandwith of 20Hz to 80kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4854		Units (Limits)
			Typical (3)	Limit (2) (4)	
P_O	Output Power (Note 11)	THD+N = 1.0%, f = 1kHz, R_L = 32Ω THD+N = 10%, f = 1kHz, R_L = 32Ω THD+N = 1.0%, f = 1kHz, R_L = 16Ω THD+N = 10%, f = 1kHz, R_L = 16Ω	32 60 57 100	27 38 	mW(min) mW mW (min) mW
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f_{IN} = ≤ 20kHz R_L = 32Ω, P_O = 30mW	0.3		%
VOUT	Output Voltage Swing	THD = 0.5%, R_L = 5kΩ	2.4		V_{P-P}
XTALK	Channel Separation	f_{IN} = 1kHz, C_{BYPASS} = 1.0µF, R_L = 32Ω	55		dB
S/N	Signal-to-Noise Ratio	f_{IN} = 1kHz, C_{BYPASS} = 1.0µF P_O = 30mW, R_L = 32Ω	TBD		dB

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4854, see power derating currents for more information.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.

External Components Description

See Figure 1.

Components		Functional Description
1.	R_i	This is the inverting input resistance that, along with R_f, sets the closed-loop gain. Input resistance R_i and input capacitance C_i form a high pass filter. The filter's cutoff frequency is $f_c = 1/2\pi R_i C_i$.
2.	C_i	This is the input coupling capacitor. It blocks DC voltage at the amplifier's inverting input. C_i and R_i create a highpass filter. The filter's cutoff frequency is $f_c = 1/2\pi R_i C_i$. Refer to the Application Information section, **SELECTING EXTERNAL COMPONENTS**, for an explanation of determining C_i's value.
3.	R_f	This is the feedback resistance that, along with R_i, sets the closed-loop gain.
4.	C_s	The supply bypass capacitor. Refer to the **POWER SUPPLY BYPASSING** section for information about properly placing, and selecting the value of, this capacitor.
5.	C_B	This capacitor filters the half-supply voltage present on the BYPASS pin. Refer to the Application Information section, **SELECTING EXTERNAL COMPONENTS**, for information about properly placing, and selecting the value of, this capacitor..

Typical Performance Characteristics

THD+N vs Frequency

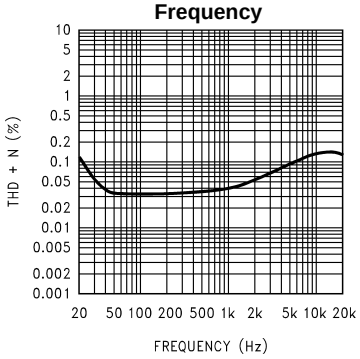

Figure 8. LM4854LD V_{DD} = 5V, R_L = 4Ω (BTL), P_{OUT} = 1000mW

THD+N vs Frequency

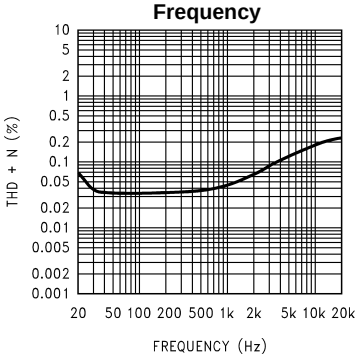

Figure 9. LM4854LD V_{DD} = 5V, R_L = 4Ω (BTL), P_{OUT} = 400mW

THD+N vs Frequency

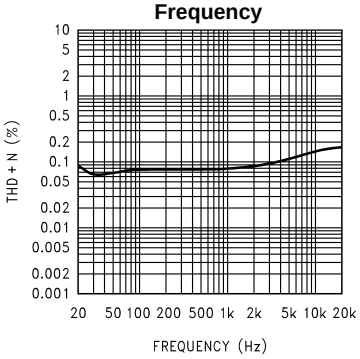

Figure 10. V_{DD} = 5V, R_L = 8Ω (BTL), P_{OUT} = 400mW

THD+N vs Frequency

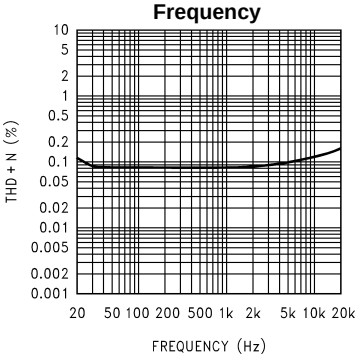

Figure 11. V_{DD} = 5V, R_L = 16Ω (SE), P_{OUT} = 50mW

THD+N vs Frequency

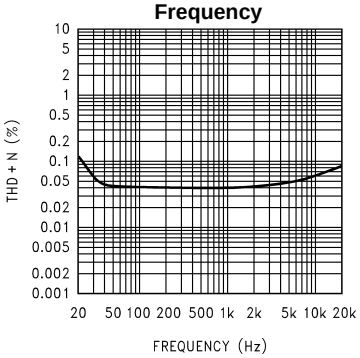

Figure 12. V_{DD} = 5V, R_L = 32Ω (SE), P_{OUT} = 50mW

THD+N vs Frequency

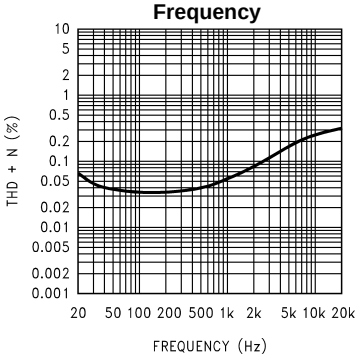

Figure 13. LM4854LD V_{DD} = 3V, R_L = 4Ω (BTL), P_{OUT} = 150mW

Typical Performance Characteristics (continued)

THD+N vs Frequency

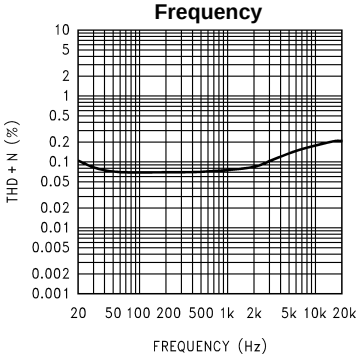

Figure 14. V_{DD} = 3V, R_L = 8Ω (BTL), P_{OUT} = 150mW

THD+N vs Frequency

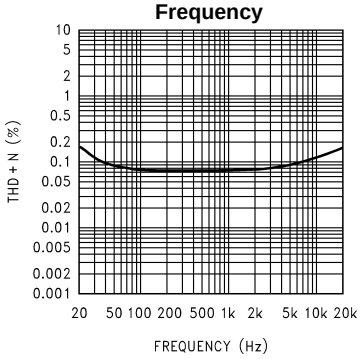

Figure 15. V_{DD} = 3V, R_L = 16Ω (SE), P_{OUT} = 30mW

THD+N vs Frequency

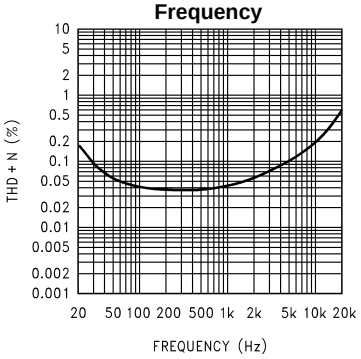

Figure 16. V_{DD} = 3V, R_L = 32Ω (SE), P_{OUT} = 30mW

THD+N vs Output Power

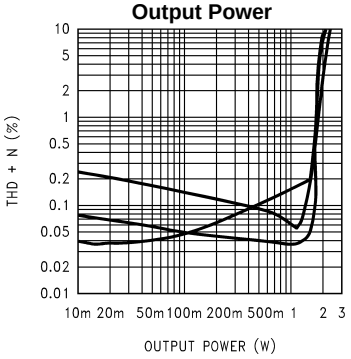

Figure 17. LM4854LD V_{DD} = 5V, R_L = 4Ω (BTL), at (from top to bottom at 200mW) 20kHZ, 20Hz, 1kHz

THD+N vs Output Power

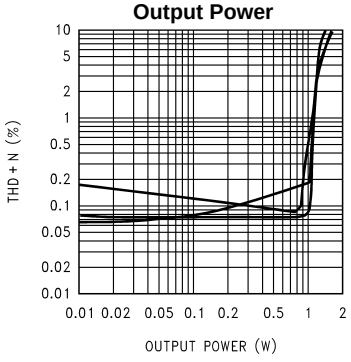

Figure 18. V_{DD} = 5V, R_L = 8Ω (BTL), at (from top to bottom at 0.2W) 20kHz, 20Hz, 1kHz

THD+N vs Output Power

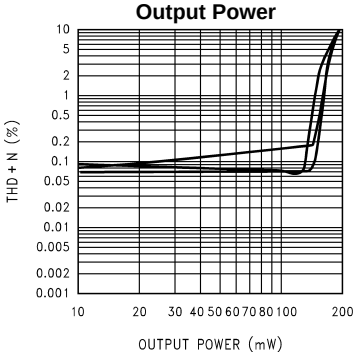

Figure 19. V_{DD} = 5V, R_L = 16Ω (SE), at (from top to bottom at 30mW) 20kHz, 20Hz, 1kHz

Typical Performance Characteristics (continued)

THD+N vs Output Power

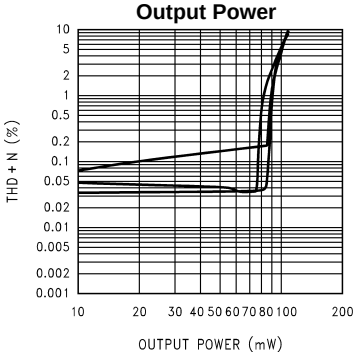

Figure 20.
V_{DD} = 5V, R_L = 32Ω (SE),
at (from top to bottom at 20mW)
20kHz, 20Hz, 1kHz

THD+N vs Output Power

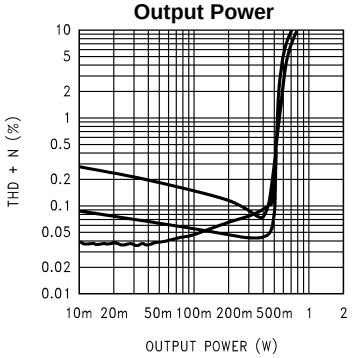

Figure 21. LM4854LD
V_{DD} = 3V, R_L = 4Ω (BTL),
at (from top to bottom at 200mW)
20kHz, 20Hz, 1kHz

THD+N vs Output Power

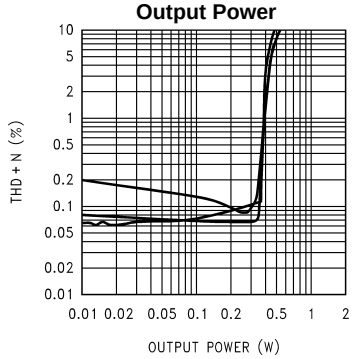

Figure 22.
V_{DD} = 3V, R_L = 8Ω (BTL),
at (from top to bottom at 0.02W)
20kHz, 20Hz, 1kHz

THD+N vs Output Power

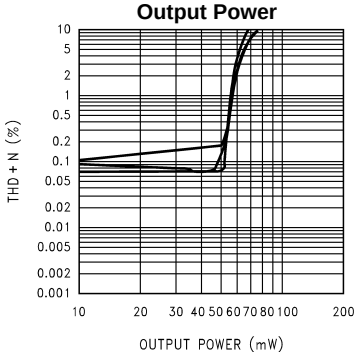

Figure 23. V_{DD} = 3V, R_L = 16Ω (SE),
at (from top to bottom at 20mW)
20kHz, 20Hz, 1kHz

THD+N vs Output Power

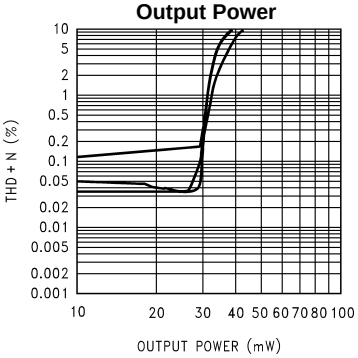

Figure 24. V_{DD} = 3V, R_L = 32Ω (SE),
at (from top to bottom at 20mW)
20kHz, 20Hz, 1kHz

Output Power vs Power Supply Voltage

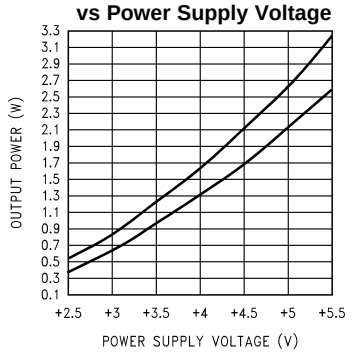

Figure 25. R_L = 8Ω (BTL), f_{IN} = 1kHz,
at (from top to bottom at 4V)
10% THD+N, 1% THD+N

Typical Performance Characteristics (continued)

Output Power vs Power Supply Voltage

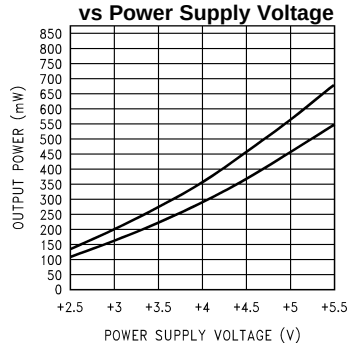

Figure 26. R_L = 16Ω (BTL), f_{IN} = 1kHz, at (from top to bottom at 4V): 10% THD+N, 1% THD+N

PSRR vs Frequency

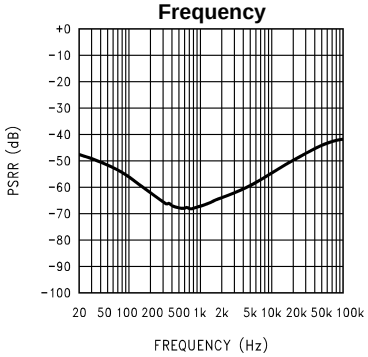

Figure 27. LM4854LD V_{DD} = 5V, R_L = 4Ω (BTL), R_{SOURCE} = 10Ω

PSRR vs Frequency

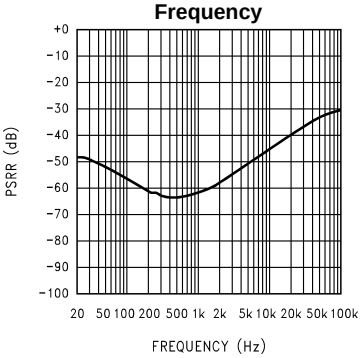

Figure 28. V_{DD} = 5V, R_L = 8Ω (BTL), R_{SOURCE} = 10Ω

PSRR vs Frequency

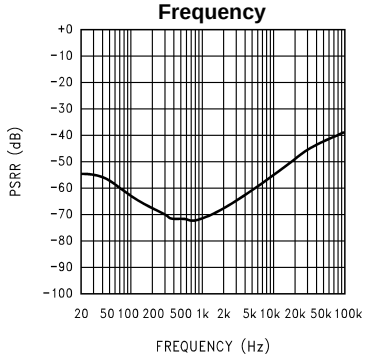

Figure 29. V_{DD} = 5V, R_L = 16Ω (SE), R_{SOURCE} = 10Ω

PSRR vs Frequency

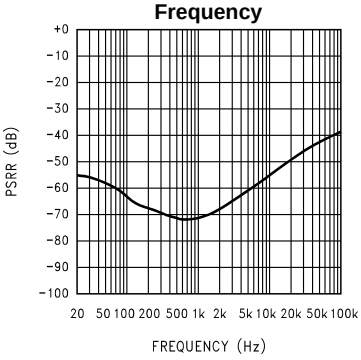

Figure 30. V_{DD} = 5V, R_L = 32Ω (SE), R_{SOURCE} = 10Ω

PSRR vs Frequency

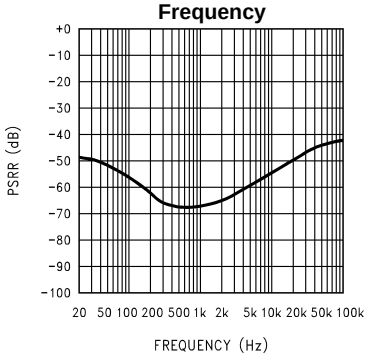

Figure 31. LM4854LD V_{DD} = 3V, R_L = 4Ω (BTL), R_{SOURCE} = 10Ω

Typical Performance Characteristics (continued)

PSRR vs Frequency

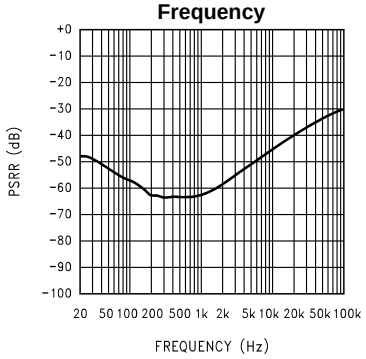

Figure 32. V_{DD} = 3V, R_L = 8Ω (BTL), R_{SOURCE} = 10Ω

PSRR vs Frequency

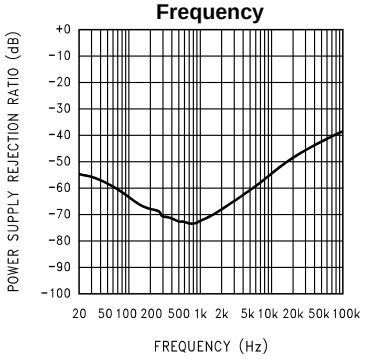

Figure 33. V_{DD} = 3V, R_L = 16Ω (SE), R_{SOURCE} = 10Ω

PSRR vs Frequency

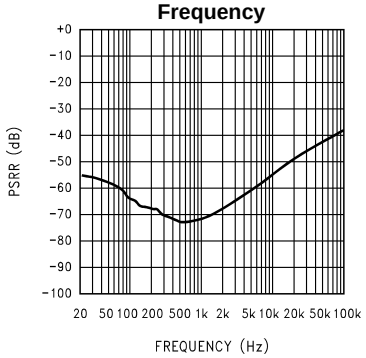

Figure 34. V_{DD} = 3V, R_L = 32Ω (SE), R_{SOURCE} = 10Ω

Amplifier Power Dissipation vs Load Power Dissipation

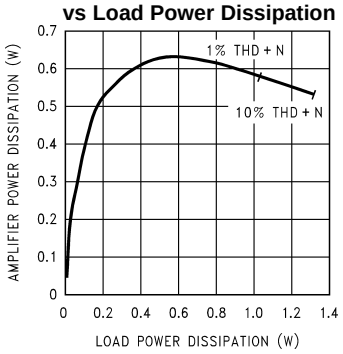

Figure 35. LM4854IBL/MT, V_{DD} = 5V, R_L = 8Ω (BTL), f_{IN} = 1kHz

Amplifier Power Dissipation vs Load Power Dissipation

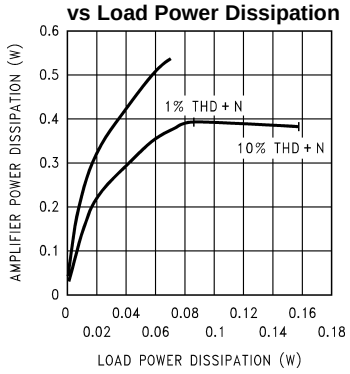

Figure 36. LM4854IBL/MT, V_{DD} = 5V, (from top to bottom at 0.04W): R_L = 16Ω (SE), R_L = 32Ω (SE), f_{IN} = 1kHz, both channels driven and loaded

Amplifier Power Dissipation vs Load Power Dissipation

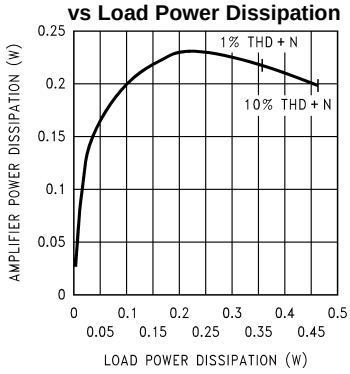

Figure 37. LM4854IBL/MT, V_{DD} = 3V, R_L = 8Ω (BTL), f_{IN} = 1kHz

Typical Performance Characteristics (continued)

Power Dissipation Derating Curves

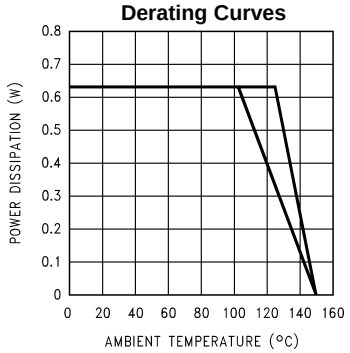

Figure 38. LM4854LD, V_{DD} = 5V, R_L = 8Ω (BTL), f_{IN} = 1kHz, (from top to bottom at 120°C): 4in² copper plane heatsink area 1in² copper plane heatsink area

Power Dissipation Derating Curve

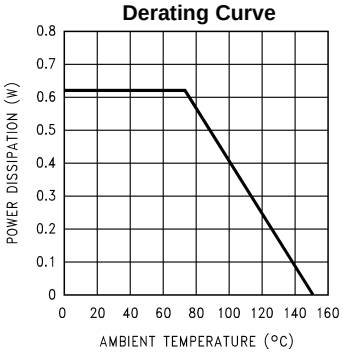

Figure 39. LM4854IBL, V_{DD} = 5V, R_L = 8Ω (BTL), f_{IN} = 1kHz

Power Dissipation Derating Curve

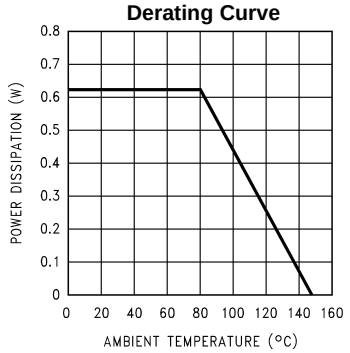

Figure 40. LM4854MT, V_{DD} = 5V, R_L = 8Ω (BTL), f_{IN} = 1kHz

Amplifier Power Dissipation vs Load Power Dissipation

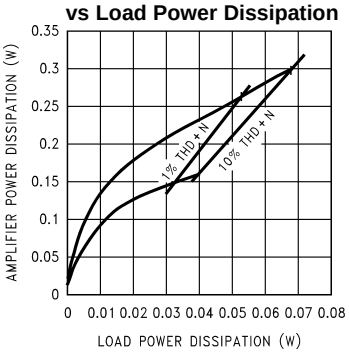

Figure 41. LM4854IBL/MT, V_{DD} = 3V, (from top to bottom at 0.02W): R_L = 16Ω (SE), R_L = 32Ω (SE), f_{IN} = 1kHz, both channels driven and loaded

Output Power vs Load Resistance

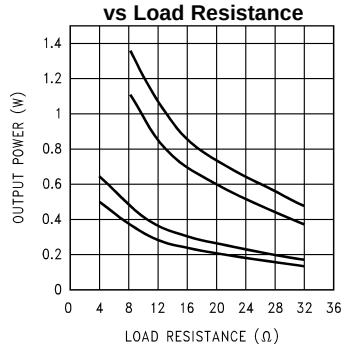

Figure 42. LM4854IBL/MT, BTL Load, (from top to bottom at 12Ω): V_{DD} = 5V, THD+N = 10%; V_{DD} = 5V, THD+N = 1% V_{DD} = 3V, THD+N = 10% V_{DD} = 3V, THD+N = 1%

Output Power vs Load Resistance

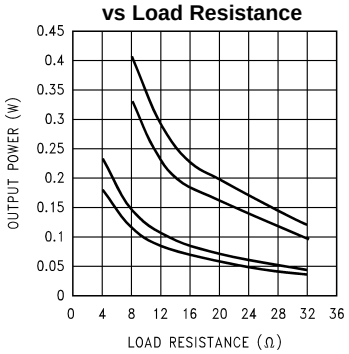

Figure 43. LM4854IBL/MT, SE Load (both channels driven and loaded), f_{IN} = 1kHz, (from top to bottom at 12Ω): V_{DD} = 5V, THD+N = 10%; V_{DD} = 5V, THD+N = 1% V_{DD} = 3V, THD+N = 10% V_{DD} = 3V, THD+N = 1%

Typical Performance Characteristics (continued)

Channel-to-Channel Crosstalk vs Frequency

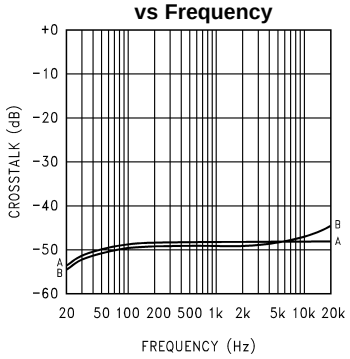

Figure 44. V_{DD} = 5V, R_L = 16Ω (SE)
A = Left channel driven, right channel measured
B = Right channel driven, left channel measured

Channel-to-Channel Crosstalk vs Frequency

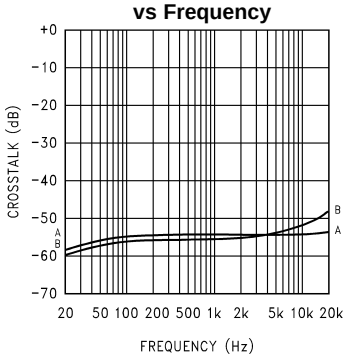

Figure 45. V_{DD} = 5V, R_L = 32Ω (SE)
A = Left channel driven, right channel measured
B = Right channel driven, left channel measured

Channel-to-Channel Crosstalk vs Frequency

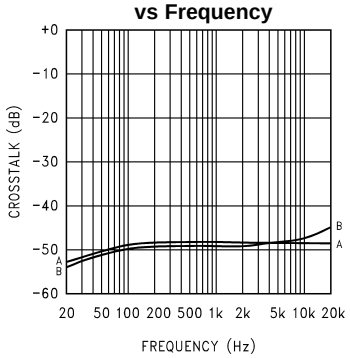

Figure 46. V_{DD} = 3V, R_L = 16Ω (SE)
A = Left channel driven, right channel measured
B = Right channel driven, left channel measured

Channel-to-Channel Crosstalk vs Frequency

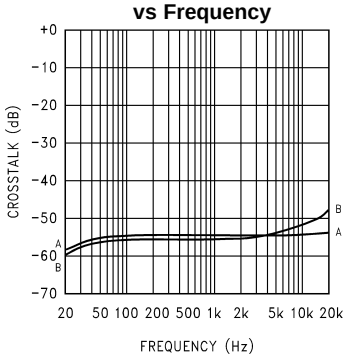

Figure 47. V_{DD} = 3V, R_L = 32Ω (SE)
A = Left channel driven, right channel measured
B = Right channel driven, left channel measured

Application Information

ELIMINATING OUTPUT COUPLING CAPACITORS

Typical single-supply audio amplifiers that can switch between driving bridge-tied-load (BTL) speakers and single-ended (SE) headphones use a coupling capacitor on each SE output. This capacitor blocks the half-supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones. The signal returns to circuit ground through the headphone jack's sleeve.

The LM4854 eliminates these coupling capacitors. When the LM4854 is configured to drive SE loads, AMP2 is internally configured to apply $V_{DD}/2$ to a stereo headphone jack's sleeve. This voltage equals the quiescent voltage present on the Amp1 and Amp3 outputs that drive the headphones. Headphones driven by the LM4854 operate in a manner very similar to a BTL load. The same DC voltage is applied to each input terminal on a headphone speaker. This results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on one of the speaker's terminal.

When operating as a headphone amplifier, the headphone jack sleeve is not connected to circuit ground, but to $V_{DD}/2$. Using the headphone output jack as a line-level output will place the LM4854's one-half supply voltage on a plug's sleeve connection. Driving a portable notebook computer or audio-visual display equipment is possible. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC-coupled, the LM4854 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds 500mA$_{PK}$, the amplifier is shutdown, protecting the LM4854 and the external equipment. For more information, see the section titled **'Single-Ended Output Power Performance and Measurement Considerations'**.

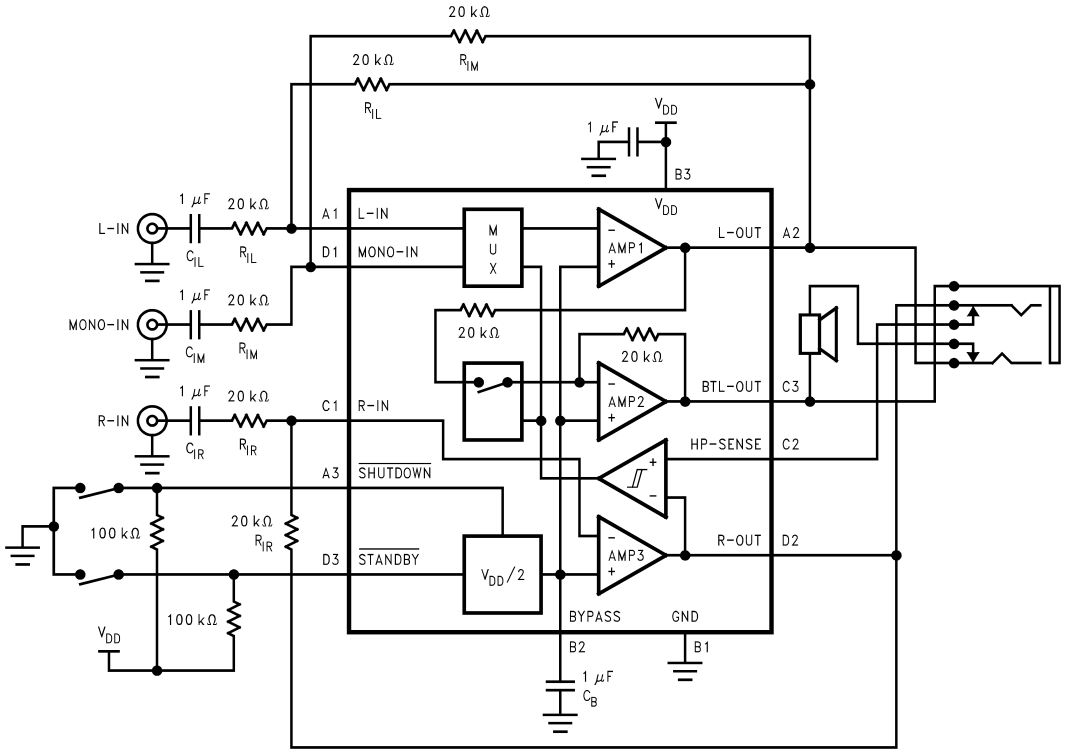

Figure 48. Typical Audio Amplifier Application Circuit

EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4854's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.7W dissipation in a 4Ω load at ≤ 1% THD+N and over 1.9W in a 3Ω load at 10% THD+N. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4854's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The LD package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 6 (3 X 2) (LD) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4854 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In all circumstances and under all conditions, the junction temperature must be held below 150°C to prevent activating the LM4854's thermal shutdown protection. The LM4854's power de-rating curve in the **Typical Performance Characteristics** shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP and LD packages are shown in the **Demonstration Board Layout** section. Further detailed and specific information concerning PCB layout and fabrication and mounting an LD (LLP) is found in National Semiconductor's AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 1.7W to 1.6W. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 2, the LM4854 consists of three operational amplifiers. In mono mode, AMP1 and AMP2 operate in series to drive a speaker connected between their outputs. In stereo mode, AMP1 and AMP3 are used to drive stereo headphones or other SE load.

In mono mode, external resistors R_{fL} and R_{iL} set the closed-loop gain of AMP1, whereas two internal 20kΩ resistors set AMP2's gain at -1. The LM4854 drives a load, such as a speaker, connected between the two amplifier outputs, L-OUT and BTL-OUT.

Figure 2 shows that AMP1's output serves as AMP2's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between L-OUT and BTL-OUT and driven differentially (commonly referred to as "bridge mode"). This results in a differential,or BTL, gain of:

$$A_{VD} = 2(R_f/R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the Audio Power Amplifier Design section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing AMP1's and AMP2's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX\text{-}SE} = (V_{DD})^2/(2\pi^2 R_L)\text{: Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions. The LM4854 has two operational amplifiers driving a mono bridge load. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum BTL-mode power dissipation is 317mW.

$$P_{DMAX-MONOBTL} = 4(V_{DD})^2/(2\pi^2 R_L)\text{: Bridge Mode} \quad (3)$$

The maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A)/ \theta_{JA} \quad (4)$$

The LM4854's TJMAX = 150°C. In the IBL package, the LM4854's θ_{JA} is 121°C/W. The LM4854's T_{JMAX} = 150°C. In the LD package soldered to a DAP pad that expands to a copper area of 2.0in^2 on a PCB, the LM4854's θ_{JA} is 42°C/W. In the MT package, the LM4854's θ_{JA} is 109°C/W. At any given ambient temperature T_A, use Equation 4to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting P_{DMAX} for P_{DMAX}' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4854's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-MONOBTL}\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 73°C for the IBL package.

$$T_{JMAX} = P_{DMAX-MONOBTL}\theta_{JA} + T_A \quad (6)$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4854's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 3 is greater than that of Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4854's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4854's power supply pin and ground as short as possible. Connecting a 1µF capacitor, CB, between the BYPASS pin and

ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially CB, depends on desired PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

STANDBY

The LM4854 features a low-power, fast turn-on standby mode. Applying a logic-low to the $\overline{\text{STANDBY}}$ pin act actives the standby mode. When this mode is active, the power supply current decreases to a nominal value of 30µA and the amplifier outputs are muted. Fast turn-on is assured because all bias points remain at the same voltage as when the part is in fully active operation. The LM4854 returns to fully active operation in 100µs (typ) after the input voltage on the $\overline{\text{STANDBY}}$ pin switches from a logic low to a logic high.

MICRO-POWER SHUTDOWN

The LM4854 features an active-low micro-power shutdown mode. When active, the LM4854's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.1µA typical shutdown current is achieved by applying a voltage to the $\overline{\text{SHUTDOWN}}$ pin that is as near to GND as possible. A voltage that is greater than GND may increase the shutdown current.

CONTROLLING STANDBY AND MICROPOWER SHUTDOWN

There are a few methods to control standby or micro-power shutdown. These include using a single-pole, single-throw switch (SPST), a microprocessor, or a microcontroller. When using a switch, connect a 100kΩ pull-up resistor between the $\overline{\text{STANDBY}}$ or $\overline{\text{SHUTDOWN}}$ pin and V_{DD} and the SPST switch between the $\overline{\text{STANDBY}}$ or $\overline{\text{SHUTDOWN}}$ pin and GND. Select normal amplifier operation by opening the switch. Closing the switch applies GND to the $\overline{\text{STANDBY}}$ or $\overline{\text{SHUTDOWN}}$ pins, activating micro-power shutdown. The switch and resistor guarantee that the $\overline{\text{STANDBY}}$ or $\overline{\text{SHUTDOWN}}$ pins will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the active-state voltage to the $\overline{\text{STANDBY}}$ or $\overline{\text{SHUTDOWN}}$ pin.

HEADPHONE (SINGLE-ENDED) AMPLIFIER OPERATION

Previous single-supply amplifiers that were designed to drive both BTL and SE loads used a SE (or headphone) "sense" input. This input typically required two external resistors to bias the sense input to a preset voltage that selected BTL operation.

The LM4854 has a unique headphone sense circuit that eliminates the external resistors. The amplifier has an internal comparator that monitors the voltage present on the R-OUT pin. It compares this voltage against the voltage on the HP-SENSE pin. When these voltages are equal, BTL mode is selected and AMP3 is shutdown and its output has a very high impedance. When the comparator's input signals are different, (a typical ΔV of 200mV), the comparator's output switches and activates the SE (headphone) mode. AMP3 changes from shutdown state to an active state and, along with AMP1, drives a stereo load. AMP2 drives the headphone jack sleeve.

Figure 3 shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip should carry a stereo signal's left-channel information. The ring adjacent to the tip should each carry the right-channel signal and the ring furthest from the tip provides the return to AMP2. A switch can replace the headphone jack contact pin. When the switch shorts the HP-SENSE pin to R-OUT, the bridge-connected speaker is driven by AMP1 and AMP2. AMP3 is shutdown, its output in a high-impedance state. When the switch opens, the LM4854 operates in SE stereo mode. If headphone drive is not needed, short the HP-SENSE pin to the R-OUT pin.

The LM4854's unique headphone sense circuit requires a dual switch headphone jack. A five-terminal headphone jack, such as the Switchcraft 35RAPC4BH3, is shown in Figure 2. For applications that require an SPDIF interface in the stereo headphone jack, use a Foxconn 2F1138-TJ-TR.

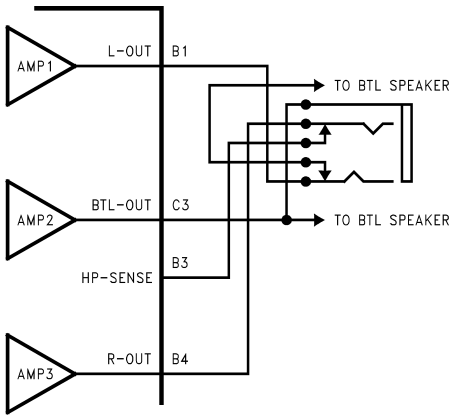

Figure 49. Headphone Circuit

Figure 4 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that supressed power supply hum. This hum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100Ω value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100Ω resistor and a 5V supply).

Single-Ended Output Power Performance and Measurement Considerations

The LM4854 delivers clean, low distortion SE output power into loads that are greater than 10Ω. As an example, output power for 16Ω and 32Ω loads are shown in the Typical Performance Characteristic curves. For loads less than 10Ω, the LM4854 can typically supply 180mW of low distortion power. However, when higher dissipation is desired in loads less than 10Ω, a dramatic increase in THD+N may occur. This is normal operation and does not indicate that proper functionality has ceased. When a jump from moderate to excessively high distortion is seen, simply reducing the output voltage swing will restore the clean, low distortion SE operation.

The dramatic jump in distortion for loads less than 10Ω occurs when current limiting circuitry activates. During SE operation, AMP2 (refer to Figure 2) drives the headphone sleeve. An on-board circuit monitors this amplifier's output current. The sudden increase in THD+N is caused by the current limit circuitry forcing AMP2 into a high-impedance output mode. When this occurs, the output waveform has discontinuities that produce large amounts of distortion. It has been observed that as the output power is steadily increased, the distortion may jump from 5% to greater than 35%. Indeed, 10% THD+N may not actually be achievable.

ESD Protection

As stated in the Absolute Maximum Ratings, the AMP2 output pin has a maximum ESD susceptibility rating of 8000V. For higher ESD voltages, the addition of a PCDN042 dual transil (from California Micro Devices), as shown in Figure 4, will provide additional protection.

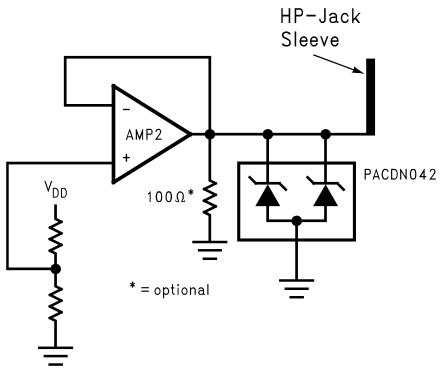

Figure 50. The PCDN042 provides additional ESD protection beyond the 8000V shown in the Absolute Maximum Ratings for the AMP2 output

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (Ci in Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The LM4854's advanced output transient suppression circuitry has eliminated the need to select the input capacitor's value in relation to the BYPASS capacitor's value as was necessary in some previous Boomer amplifiers. The value of CI is now strictly determined by the desired low frequency response.

As shown in Figure 2, the input resistor (R_i) and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation 7.

$$f_c = 1 / (2\pi R_i C_i) \quad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 7 is 0.063µF. The 1.0µF C_i shown in Figure 2 allows the LM4854 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of CB, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4854 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4854's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of Ci (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. CB's value should be in the range of 5 times to 7 times the value of C_i. This ensures that output transients are eliminated when power is first applied or the LM4854 resumes operation after shutdown.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4854 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops") and transients that could occur when switching between BTL speakers and single-ended headphones. For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the $V_{DD}/2$ voltage present at the BYPASS pin ramps to its final value, the LM4854's internal amplifiers are configured as unity gain buffers and are disconnected from the L-OUT, BTL-OUT, and R-OUT pins. An internal current source charges the capacitor connected between the BYPASS pin and GND in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $V_{DD}/2$. Once the voltage on the bypass pin is stable and after a fixed nominal delay of 120ms, the device becomes fully operational and the amplifier outputs are reconnected to their respective output pins. Although the BYPASS pin current cannot be modified, changing the size of CB alters the device's turn-on time. There is a linear relationship between the size of CB and the turn-on time. Here are some typical turn-on times for various values of CB:

C_B (µF)	T_{ON} (ms)
0.01	120
0.1	130
0.22	140
0.47	160
1.0	200
2.2	300

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

- Power Output: $1W_{RMS}$
- Load Impedance 8Ω
- Input Level: $1V_{RMS}$
- Input Impedance: 20kΩ
- Bandwidth: 100Hz - 20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation 8, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation 8. The result is Equation 9.

$$V_{outpeak} = \sqrt{2 R_L P_O} \quad (8)$$

$$V_{DD} = V_{OUTPEAK} + V_{ODTOP} + V_{ODBOT} \quad (9)$$

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. The commonly used 5V supply voltage easily meets this. The additional voltage creates the benefit of headroom, allowing the LM4854 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the Power Dissipation section. After satisfying the LM4854's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation 10.

$$A_{VD} \geq \frac{\sqrt{P_O R_L}}{V_{IN}} = \frac{V_{ORMS}}{V_{INRMS}} \quad (10)$$

Thus, a minimum gain of 2.83 allows the LM4854's to reach full output swing and maintain low noise and THD+N performance. For this example, let AVD = 3. The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_f / R_i = A_{VD} / 2 \quad (11)$$

The value of R_f is 30kΩ. The nominal output power is 1.13W.

TThe last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB-desired limit. The results are an

$$f_L = 100Hz / 5 = 20Hz \quad (12)$$

and an

$$f_L = 20kHz \times 5 = 100kHz \quad (13)$$

As mentioned in the SELECTING EXTERNAL COMPONENTS section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (14).

$$C_i = 1 / (2\pi R_i f_L) \quad (14)$$

The result is

$$1 / (2\pi \times 20k\Omega \times 20Hz) = 0.397\mu F \quad (15)$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain AVD, determines the upper passband response limit. With AVD = 3 and fH = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4854's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 51 through Figure 54 show the recommended four-layer PC board layout that is optimized for the micro SMD-packaged LM4854 and associated external components. Figure 56 through Figure 55 show the recommended two-layer PC board layout that is optimized for the TSSOP-packaged LM4854 and associated external components.Figure 60 through Figure 63 show the recommended four-layer PC board layout that is optimized for the LLP-packaged LM4854 and associate external components.

These circuits are designed for use with an external 5V supply and 8Ω(min) speakers. These circuit boards are easy to use. Apply 5V and ground to the board's V_{DD} and GND pads, respectively. Connect a speaker between the board's L-OUT and BTL-OUT or headphones to the headphone jack (L-OUT and R-OUT outputs).

Demonstration Board Layout

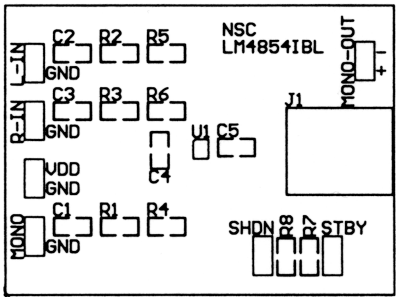

Figure 51. Recommended microSMD PC Board Layout: Component-Side SilkScreen

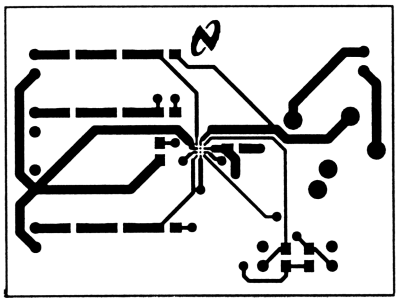

Figure 52. Recommended microSMD PC Board Layout: Component-Side Layout

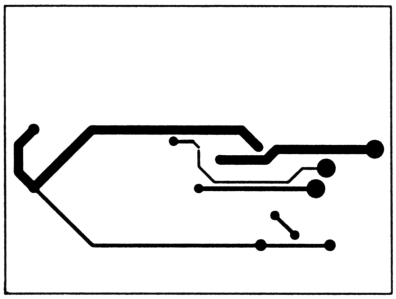

Figure 53. Recommended microSMD PC Board Layout: Upper Inner-Layer Layout

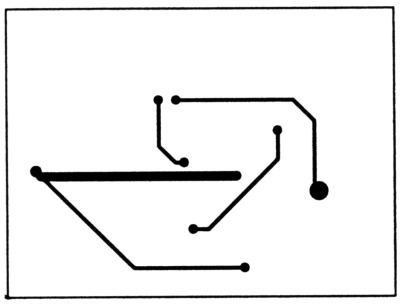

Figure 54. Recommended microSMD PC Board Layout: Lower Inner-Layout Layer

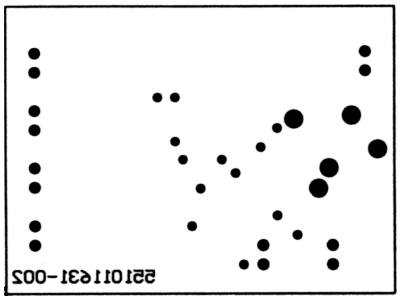

Figure 55. Recommended MM PC Board Layout: Bottom_Side Layout

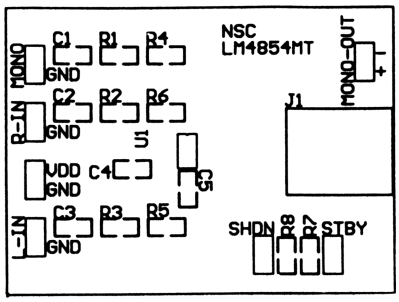

Figure 56. Recommended MT PC Board Layout: Component-Side SilkScreen

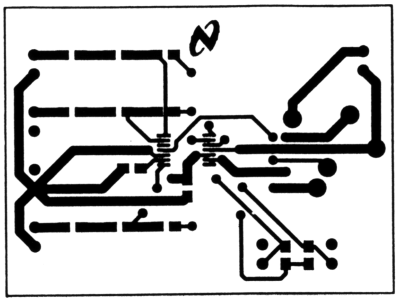

Figure 57. Recommended MT PC Board Layout: Component-Side Layout

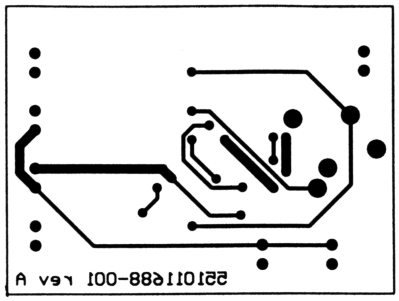

Figure 58. Recommended MT PC Board Layout: Bottom-Side Layout

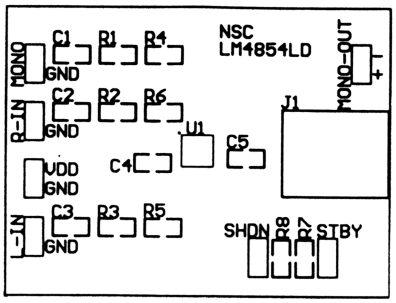

Figure 59. Recommended LD PC Board Layout: Component-Side SilkScreen

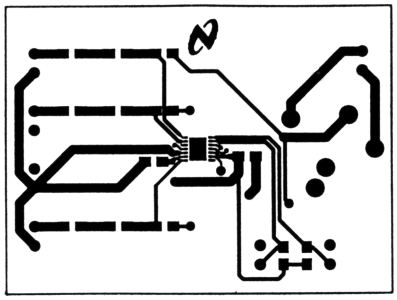

Figure 60. Recommended LD PC Board Layout: Component-Side Layout

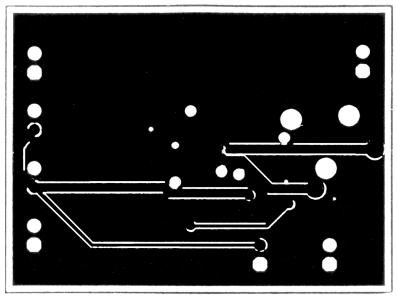

Figure 61. Recommended LD PC Board Layout: Upper Inner-Layer Layout

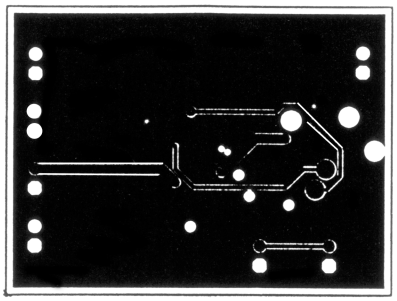

Figure 62. Recommended LD PC Board Layout: Lower Inner-Layer Layout

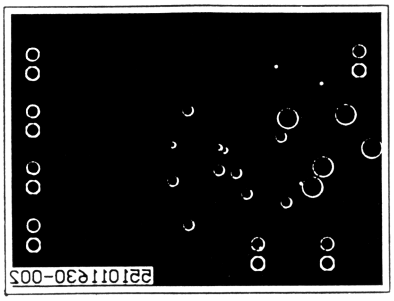

Figure 63. Recommended LD PC Board Layout: Bottom-Side Layout

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