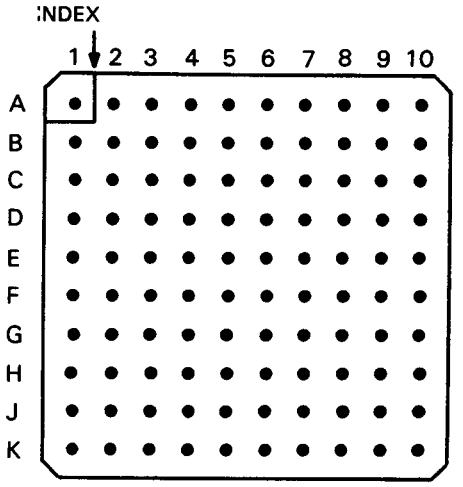
SEPTEMBER 1985 - REVISED MAY 1986

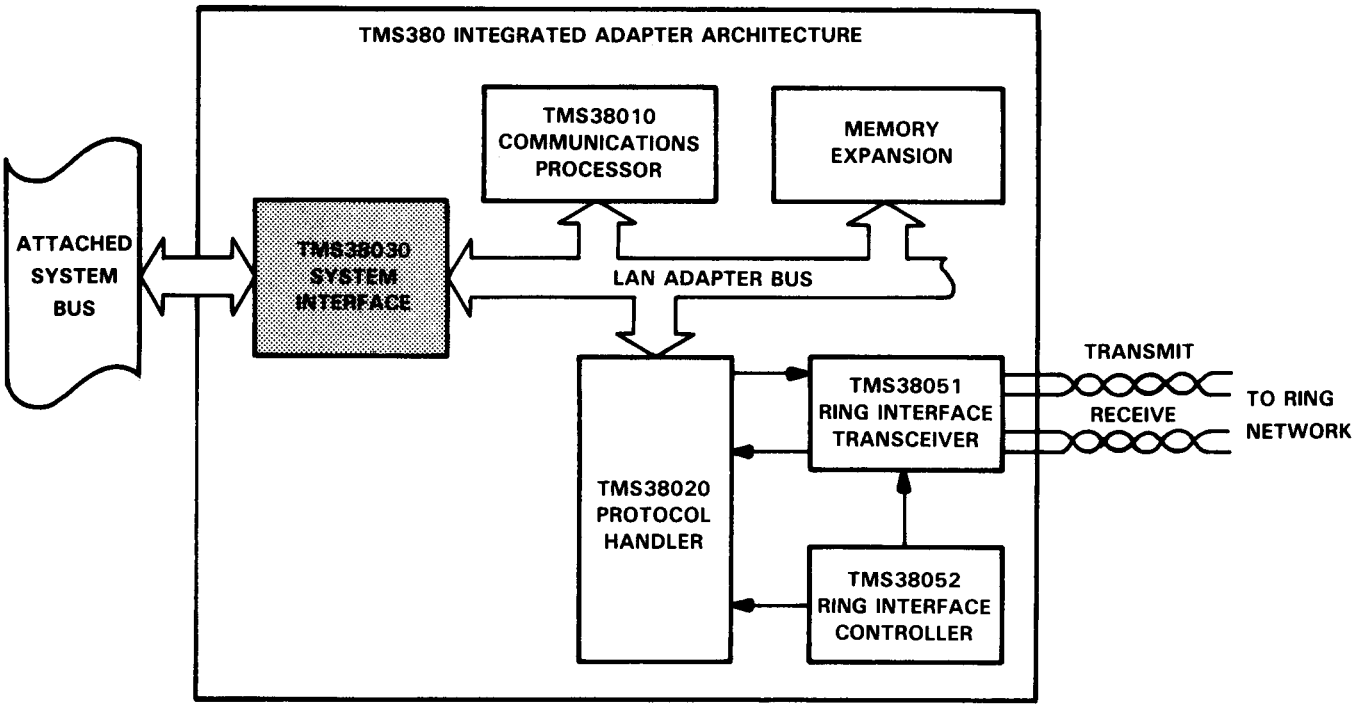
- **Connects Two High-Speed Asynchronous Buses**
  - **—Up to 5M Bytes/Second DMA on Host System Bus**
  - **—6M Bytes/Second DMA on LAN Adapter Bus**
- **Provides Dual-Port DMA and Direct I/O Transfer Between Buses**
- **Selectable Host System Bus Options**
  - **—808X- or 680XX-Type Bus and Memory Organization**
  - **—8- or 16-Bit Data Bus for 808X-Type Buses**
  - **—Optional Parity Checking**
- **Provides Direct Control of Latches and Drivers on Host System Bus Interface**
- **Test Pin for Hi-Z, Module-In-Place Testing**
- **Single 5-V Supply**
- **100-Pin Ceramic Grid Array Package**
- **Low-Power Scaled-NMOS Technology**

GB PACKAGE†
(TOP VIEW)



†See pin description table (Page 2) for location and description of all pins.

token ring LAN application diagram



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pin descriptions

NAME	PIN	I/O	DESCRIPTION
SYSTEM BUS ADDRESS/DATA PINS			
SADH0	H7	I/O	System address/Data bus — High Byte. SADH0 is the most-significant bit
SADH1	K10	I/O	and SADH7 is the least-significant bit.
SADH2	J8	I/O	
SADH3	J7	I/O	
SADH4	K6	I/O	
SADH5	J6	I/O	
SADH6	K9	I/O	
SADH7	K8	I/O	
SADL0	J5	I/O	System Address/Data bus — Low Byte. SADL0 is the most-significant bit and SADL7
SADL1	H5	I/O	is the least-significant bit.
SADL2	G5	I/O	
SADL3	K4	I/O	
SADL4	F5	I/O	
SADL5	J4	I/O	
SADL6	H4	I/O	
SADL7	K3	I/O	
SPH	K7	I/O	System Parity High Byte
SPL	K5	I/O	System Parity Low Byte
SYSTEM BUS CONTROL PINS			
SI/$\overline{M}$	H8	I	808X/680XX Mode Select
S8/$\overline{16}$	H9	I	8/16-Bit Data Bus Select
$\overline{SRESET}$	H10	I	System Reset
$\overline{SCS}$	J2	I	Chip Select
SRS0	K2	I	Register Select 0 (MSB)
SRS1	H3	I	Register Select 1
SRS2	G4	I	Register Select 2 (LSB)
$\overline{SBHE}$/SRNW	K1	I/O	Byte High Enable (808X mode)/Read Not Write (680XX mode)
$\overline{SWR}$/$\overline{SLDS}$	H1	I/O	Write Strobe (808X mode)/Lower Data Strobe (680XX mode)
$\overline{SRD}$/$\overline{SUDS}$	G1	I/O	Read Strobe (808X mode)/Upper Data Strobe (680XX mode)
SRAS/$\overline{SAS}$	G3	I/O	Register Address Strobe (808X mode)/Memory Address Strobe (680XX mode)
$\overline{SRDY}$/$\overline{SDTACK}$	J1	I/O	Bus Ready (808X mode)/Data Transfer Acknowledge (680XX mode)
SALE	D3	O	Address Latch Enable
SXAL	D2	O	Extended Address Latch Enable
SBCLK	E2	I	System Bus Clock
SYSTEM BUS DRIVER/RECEIVER CONTROL PINS			
SDDIR	C2	O	Data Direction
$\overline{SDBEN}$	C1	O	Data Bus Enable
$\overline{SOWN}$	E5	O	System Bus Owned

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pin descriptions (continued)

NAME	PIN	I/O	DESCRIPTION
			SYSTEM BUS ARBITRATION/DMA CONTROL PINS
SHRQ/$\overline{\text{SBRQ}}$	H2	O	Hold Request (808X mode)/Bus Request (680XX mode)
SHLDA/$\overline{\text{SBGR}}$	F1	I	Hold Acknowledge (808X mode)/Bus Grant (680XX mode)
$\overline{\text{SBBSY}}$	G2	I	Bus Busy
$\overline{\text{SBRLS}}$	B2	I	Bus Release
$\overline{\text{SBERR}}$	F2	I	Bus Error
			SYSTEM BUS INTERRUPT CONTROL PINS
SINTR/$\overline{\text{SIRQ}}$	D4	O	Interrupt Request (808X mode)/Interrupt Request (680XX mode)
$\overline{\text{SIACK}}$	D1	I	Interrupt Acknowledge
			LAN ADAPTER BUS ADDRESS/DATA PINS
LAD0	B8	I/O	LAN Adapter Bus Address/Data Bus. LAD0 is the most-significant bit and LAD15 is the least-significant bit.
LAD1	A8	I/O	
LAD2	C7	I/O	
LAD3	B7	I/O	
LAD4	A7	I/O	
LAD5	D6	I/O	
LAD6	C6	I/O	
LAD7	B6	I/O	
LAD8	A3	I/O	
LAD9	A2	I/O	
LAD10	B5	I/O	
LAD11	A5	I/O	
LAD12	B4	I/O	
LAD13	B3	I/O	
LAD14	A1	I/O	
LAD15	C4	I/O	
LPH	A6	I/O	LAN Adapter Bus Parity High Byte
LPL	A4	I/O	LAN Adapter Bus Parity Low Byte
			LAN ADAPTER BUS CONTROL PINS
LBCLK1	B10	I	LAN Adapter Bus Clock 1
LBCLK2	C10	I	LAN Adapter Bus Clock 2
LAL	D9	I/O	LAN Adapter Bus Address Latch Enable
LI/$\overline{\text{D}}$	D8	I	LAN Adapter Bus Instruction/Data Bus Status Code
$\overline{\text{LEN}}$	C9	I/O	LAN Adapter Bus Data Enable
LR/$\overline{\text{W}}$	E7	I/O	LAN Adapter Bus Read/Not Write
LBRDY	A9	I	LAN Adapter Bus Ready

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pin descriptions (concluded)

NAME	PIN	I/O	DESCRIPTION
			LAN ADAPTER BUS INTERRUPT PINS
LIRQIN0	G10	I	LAN Adapter Bus Interrupt Request 0 Input
LIRQIN1	F7	I	LAN Adapter Bus Interrupt Request 1 Input
LIRQIN2	F8	I	LAN Adapter Bus Interrupt Request 2 Input
LIRQOUT0	F6	O	LAN Adapter Bus Interrupt Request Output 0
LIRQOUT1	F10	O	LAN Adapter Bus Interrupt Request Output 1
LIRQOUT2	F9	O	LAN Adapter Bus Interrupt Request Output 2
$\overline{\text{LRESET}}$	G9	O	LAN Adapter Bus Reset
			LAN ADAPTER BUS ARBITRATION PINS
$\overline{\text{LBRQS}}$	A10	O	LAN Adapter Bus Request
$\overline{\text{LBGRS}}$	C8	I	LAN Adapter Bus Grant
			MISCELLANEOUS PINS
$\overline{\text{CHPTST}}$	J10	I	This pin is reserved and should be left unconnected.
$\overline{\text{TEST}}$	G8	I	Module-in-Place Test Mode Select
V_{BB}	D10		This pin is reserved and should be left unconnected.
NC	E6		This pin is reserved and should be left unconnected.
			POWER PINS
V_{CC}	J3		5-V power supply (All pins must be connected.)
V_{CC}	J9		
V_{CC}	E9		
V_{CC}	D7		
V_{CC}	D5		
V_{CC}	E3		
V_{SS}	C3		Ground pins (All pins must be connected.)
V_{SS}	E4		
V_{SS}	E1		
V_{SS}	F3		
V_{SS}	F4		
V_{SS}	H6		
V_{SS}	G6		
V_{SS}	G7		
V_{SS}	E8		
V_{SS}	E10		
V_{SS}	B9		
V_{SS}	C5		
V_{SS}	B1		

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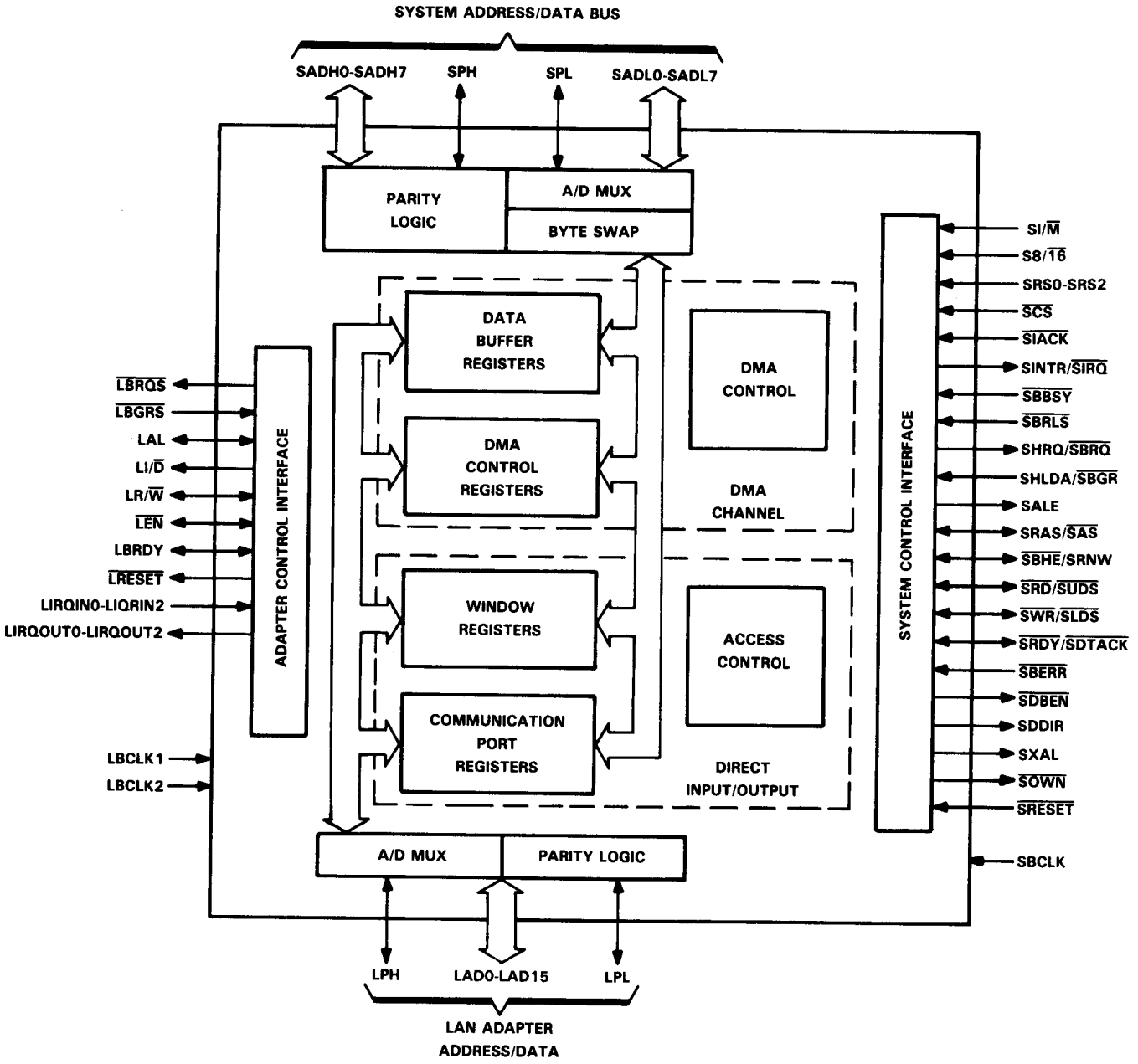
functional block diagram†



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†For signal names separated by a slash (/), the first signal name given is for the 808X mode and the second signal name is for the 680XX mode.

description

The TMS38030 System Interface (SIF) connects two high-speed buses and provides DMA and direct I/O (DIO) transfer between these buses. The TMS38030 features a dual-port DMA channel and DIO registers that connect a host system bus transferring data up to 5 megabytes per second to the LAN Adapter bus operating at a 6 megabyte per second transfer rate. For added flexibility the host system bus can be pin-strap selected to either an 808X-type or 680XX-type bus allowing the designer to choose the bus configuration which best meets his application. When in 808X mode, the TMS38030 automatically handles byte swapping to meet the requirements of the 808X processor memory conventions. Four DIO registers on the host system bus are available for handshaking between the host system CPU and the LAN Adapter CPU. Full control of the TMS38030 is provided by nine 16-bit registers accessible from the LAN Adapter bus interface. Control lines on the host system bus interface reduce interface logic requirements by providing direct control of latches and drivers.

The TMS38030, when coupled with the TMS38010 Communications Processor, the TMS38020 Protocol Handler, and the TMS38051 and TMS38052 Ring Interface Circuits, forms a complete integrated Token Ring local area network adapter fully compatible with IEEE Std 802.5-1985 Token Ring Access and Physical Layer Specifications for Token Ring Networks.

architecture

The TMS38030 may be conceptually viewed as shown in Figure 1. The DMA controller differs from conventional DMA controllers in that DMA transfers occur from the memory of one bus to the memory of another bus versus DMA transfers on the same bus. The two buses are independent of each other in that timing of one bus may be asynchronous to the timing of the other. A direct I/O (DIO) (or memory-mapped I/O) interface on the host system bus may be used as a low-level handshake between the two CPUs as well as for posting interrupts from one CPU to the other.

The TMS38030 also contains an interrupt priority encoder for prioritizing up to seven interrupt levels for presentation to the LAN Adapter bus CPU (TMS38010 Communications Processor).

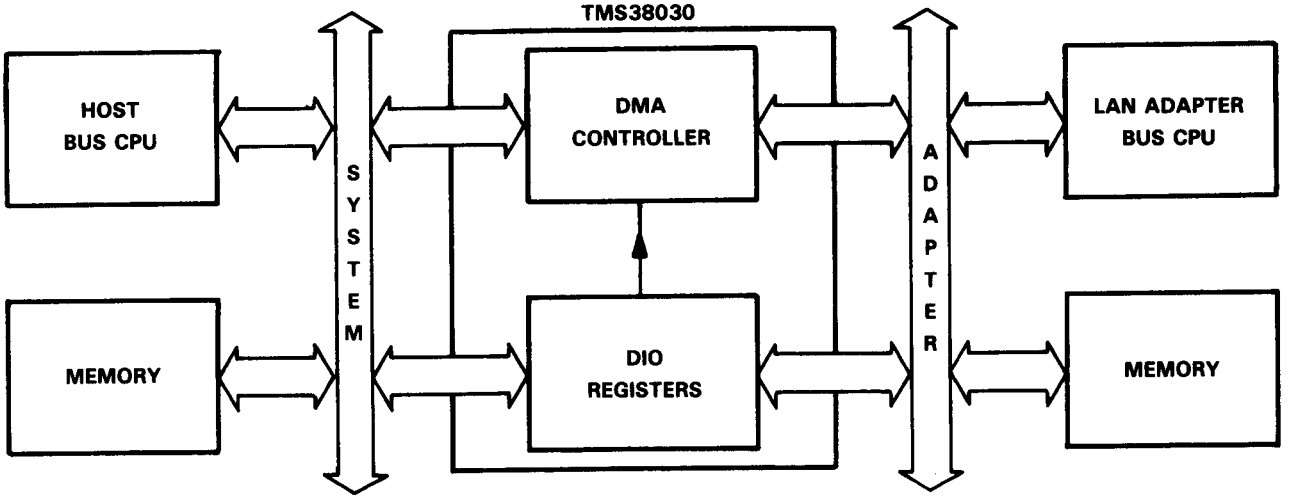

FIGURE 1. TMS38030 DMA CONTROL—CONCEPTUAL REPRESENTATION

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system bus interface

interface modes

The TMS38030 system-side interface may be pin strap selected, via the SI/$\overline{M}$ pin, to provide pin personalities compatible with 808X-type and 680XX-type processor buses. When the SI/$\overline{M}$ pin is tied high, the system interface pins assume 808X-type personalities. When the SI/$\overline{M}$ pin is tied low, the system interface pins assume 680XX-type personalities. The system designer has the option to choose the bus type which best supports his intended hardware environment.

The S8/$\overline{16}$ pin may be used to select either an 8-bit or 16-bit wide system data bus when the SI/$\overline{M}$ pin is strapped high (808X mode). When 8-bit mode is selected, the SI/$\overline{M}$ pin must not be strapped low (680XX mode). When in 8-bit mode, the data is transferred on the SADL0-SADL7 pins while the SADH0-SADH7 pins are either ignored during data read or high impedance during data write.

direct I/O registers

Located on the system bus are four 16-bit registers. One register, called the Interrupt Register, is dedicated to bit-level status and control information handshaking between the host system processor and the LAN Adapter bus processor (the TMS38010 Communications Processor). The remaining three registers are used by the host system processor to access memory locations within the LAN Adapter bus address space. These registers are the Address Register, Data Register, and Data Register with Autoincrement (of the Address Register). These registers are selected by the SRS0-SRS2 register select pins as shown in Table 1.

TABLE 1. TMS38030 SYSTEM BUS REGISTERS

SRS0	SRS1	SRS2	REGISTER
L	L	Note 1	Data Register
L	H	Note 1	Data Register with Autoincrement
H	L	Note 1	Address Register
H	H	Note 1	Interrupt Register

NOTE 1: SRS2 is used to address the upper/lower byte of the register when in 8-bit mode (S8/$\overline{16}$ high).

interrupt register

The Interrupt Register is used to pass bit-level control and status information between the host system processor and the LAN Adapter processor (TMS38010). The Interrupt Register is also used to clear the TMS38030-to-host interrupt (SINTR/$\overline{SIRQ}$) and to post interrupts to the LAN Adapter bus CPU through the TMS38030 interrupt prioritizer. The bit functions of the Interrupt Register are shown in Table 2.

TABLE 2. INTERRUPT REGISTER BIT FUNCTIONS — SYSTEM SIDE

BITS	READ/WRITE	FUNCTION
0 (MSB)	Write	1 = set bit and interrupt LAN Adapter Bus CPU. 0 = no effect.
	Read	Read value of bit.
1-7	Write	1 = sets bit value to 1. 0 = no effect.
	Read	Read value of bit.
8	Write	1 = no effect. 0 = reset. SINTR/$\overline{SIRQ}$ to inactive high.
9-15	Write	No effect. These bits cannot be set/reset by the host processor.
	Read	Read value of bits.

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address register

The Address Register provides a pointer into LAN Adapter bus memory address space with which the host system processor may access data through either the Data Register or the Data Register with Autoincrement. Bits 5 through 14 may be set to any value by the host processor by writing the appropriate value to this register. Bits 0-4 and bit 15 may only be set/reset by the LAN Adapter bus CPU. This allows the LAN Adapter bus CPU to control host access to the LAN Adapter bus memory space within a 2K-byte window as defined by the setting of bits 0 through 4. Bit 15 is always set to zero as all data transfers on the LAN Adapter bus are 16-bit transfers (even addresses).

data registers

Two data registers provide read/write capability to the LAN Adapter bus memory address location pointed to by the Address Register. The host processor does not access these locations directly however, the TMS38030 performs LAN Adapter bus DMA operations to read or write the memory location as necessary.

When read, the Data Register returns the value found in the memory location pointed to by the Address Register. The TMS38030 will perform a DMA read of this location when this occurs. Writing to the Data Register will cause the data to be written to the LAN Adapter bus memory location as pointed to by the Address Register when the IOWEN bit of the SIF Control (SIFCTL) Register is set to one. The TMS38030 will perform a DMA write to this location when this occurs.

The Data Register with Autoincrement behaves identically to the Data Register; however, the Address Register is automatically incremented by two following each access (post increment). This feature is useful for the passing of parameter tables to sequential memory locations within the LAN Adapter bus memory space.

direct input/output

Read and write cycles to the direct I/O registers cannot occur simultaneously with DMA operation on the system bus because they share the same physical interface pins. However, a DIO access occurring between two successive bus cycles of a DMA cycle will not disrupt any DMA conditions existing within the TMS38030.

direct memory access

The direct memory access (DMA) channel of the system bus interface provides a full 24 bits of address with which to access up to 16 megabytes of system memory. The throughput capability of the DMA channel is matched to that of the host system through a host system supplied bus clock (SBCLK). The maximum DMA transfer rate corresponds to one word per four user system clock periods. DMA on the system bus may occur concurrently and asynchronously to DMA on the LAN Adapter bus.

When configured in 808X mode, the TMS38030 performs automatic byte swapping on data passed between the LAN Adapter bus and the host system bus. This is to compensate for the differing byte ordering conventions between the 808X-type processor and the LAN Adapter bus CPU. The LAN Adapter bus memory organization defines byte 0 of a 16-bit memory word to be the most-significant byte and byte 1 to be the least-significant. The 808X-type processor defines byte 0 of a 16-bit memory word to be the least-significant byte and byte 1 to be the most-significant. Byte swapping automatically corrects for this difference in convention. Byte swapping is not performed on DIO accesses.

The system bus DMA is controlled by the LAN Adapter bus CPU through the registers resident on the Adapter bus. The system bus DMA may be configured for system bus starting address, DMA length, burst or cycle-steal mode of operation and parity checking on DMA reads.

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Since only 16 bits of address can be output at any instant on the 16 address/data pins, the 8 most-significant address bits must be multiplexed onto the address/data pins. These are called the extended address bits. Two separate latch enable signals (SALE and SXAL) are provided for the demultiplexing of the address. The extended address portion is updated only when the TMS38030 increments an address such that a carry out from the low-order 8 bits is generated. The updating of the extended address is done during an extra phase of the system bus memory transfer cycle. This extra phase is termed the TX cycle. For systems only requiring 16-bits of address, the extended address latches are not required. The TMS38030 performs a TX cycle every time it acquires the system bus. In cycle steal mode, then, the TMS38030 will always perform a TX cycle; in burst mode, the TMS38030 will perform a TX cycle on the first memory cycle and thereafter only when the most-significant 16 bits of address are changed due to a carry propagated from the lower 8 bits. Detailed timing of system DMA operations for both 808X mode and 680XX mode may be found in the Electrical Specifications.

LAN adapter bus interface

The LAN Adapter bus interface provides the ability of the TMS38030 to transfer data between the LAN Adapter bus environment and the system bus. This high-speed bus is used by the TMS380 family to connect the TMS38010 Communications Processor and TMS38020 Protocol Handler. In expanded configurations, the LAN Adapter bus can interface to expansion memory. The timing of LAN Adapter bus memory mapped I/O and direct memory access cycles is provided in the Electrical Specifications.

LAN Adapter bus registers

The TMS38030 contains nine registers accessible from the LAN Adapter bus side. These registers are used to control the DMA operation on the system bus side, the DMA operation on the LAN Adapter bus side, direct I/O for the system bus side, and the system interrupt vector driven onto the system bus side during an interrupt acknowledge cycle. These registers, their function and LAN Adapter bus memory location are shown in Figure 2.

ADDRESS	BITS 0	7	8	15	DESCRIPTION
>0080	SIFCTL				SYSTEM INTERFACE CONTROL
>0082	SIFACT				SYSTEM INTERFACE ACTIVITY
>0084	SIFINT				INTERRUPT REGISTER
>0086	SIFADR				SYSTEM DIO ADAPTER BUS ADDRESS
>0088	SDMALEN				SYSTEM DMA LENGTH
>008A	00		SDMAX		SYSTEM ADDRESS EXTENDED BYTE
>008C	SDMAH		SDMAL		SYSTEM ADDRESS HIGH/LOW BYTES
>008E	LDMAADR				ADAPTER BUS DMA ADDRESS
>0090	00		SIFVEC		SYSTEM INTERRUPT VECTOR

FIGURE 2. TMS38030 LAN ADAPTER BUS REGISTERS

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SIFCTL register

The SIFCTL register controls all TMS38030 peripheral functions. Certain values are loaded to the bits of SIFCTL when the LAN Adapter bus CPU writes to address >0080. The current value of the bits are returned by reading the word at this location. Changes made to DMADIR, DMABURST, SPIEN, and SLPIEN bits have no effect on DMA operations already in progress. Such changes affect subsequent DMA operation. All bits of SIFCTL are set to zero when $\overline{\text{SRESET}}$ is activated. The bits of SIFCTL are summarized in Table 3.

TABLE 3. SIFCTL REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	DMADIR	System DMA Direction
1	DMAENB	System DMA Enable
2	DMABURST	System DMA Burst Mode
3	DMAHALT	System DMA Halt
4	DMAIEN	System DMA Interrupt Enable
5	SPIEN	System Parity Interrupt Enable
6	SPTST	System Parity Test
7	SLPIEN	System Local Parity Enable
8	IOWEN	DIO Write Enable
9-15		Reserved

SIFACT register

The SIFACT register contains the system bus error flag, LAN Adapter bus and system bus parity error flags, and the DMA halt interrupt request bit. All bits of SIFACT are reset to zero at system reset. Table 4 summarizes the bit functions of the SIFACT register.

TABLE 4. SIFACT REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0		Reserved
1		Reserved
2	DIRQ	System DMA Halt Interrupt Request
3	SPE	System Parity Error - DIO
4	SDPE	System Parity Error - DMA
5	SDBE	System DMA Bus Error
6	LPEXM	LAN Adapter Bus Parity Error - External Master
7	LPESM	LAN Adapter Bus Parity Error - TMS38030 Master
8-15		Reserved

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SIFINT register

The SIFINT register is the Interrupt register which is accessible from both the host system bus side and the LAN Adapter bus side. However, the restrictions on setting/clearing these bits is different than when accessed from the LAN Adapter bus side. These are illustrated in Table 5. Table 2 illustrates the function of these bits as viewed from the host system bus side.

TABLE 5. INTERRUPT REGISTER BIT FUNCTIONS - LAN ADAPTER BUS SIDE

BITS	READ/WRITE	FUNCTION
0 (MSB)	Write	1 = no effect. 0 = clear interrupt.
	Read	Read value of bit.
1-7	Write	1 = no effect. 0 = reset bit to zero.
	Read	Read value of bit.
8	Write	1 = set SINT/$\overline{\text{SIRQ}}$ active. 0 = no effect.
9-15	Write	Modify current contents.
	Read	Read value of bits.

SIFADR Register

The SIFADR (SIF Address) register is the Address register which is accessible from both the host system bus and the LAN Adapter bus. Bits 0-4 and bit 15 can only be set/reset from the LAN Adapter bus side of the TMS38030. The remaining bits (5-14) can only be set/reset from the host system side of the TMS38030.

SDMALEN Register

The SDMALEN (System DMA length) register contains the byte count length of a DMA transfer. A maximum length transfer can be 65,535 bytes. A zero loaded into SDMALEN will limit DMA to transferring zero bytes.

SDMAX, SDMAH, and SDMAL Registers

These three register fields contain the 24-bit system address where DMA is to begin. SDMAX contains the most-significant eight bits, SDMAH the middle eight bits, and SDMAL the least-significant eight bits.

LDMAADR Register

The LDMAADR (LAN Adapter bus DMA address) register contains the 16-bits of LAN Adapter bus address location where DMA is to begin. This address space is always in the data space of the LAN Adapter bus (the TMS38030 always drives LI/$\overline{\text{D}}$ low). The DMA length is controlled by SDMALEN.

SIFVEC Register

The SIFVEC (SIF vector) register contains the 8-bit interrupt vector which is output onto the system data bus during an interrupt acknowledge cycle.

interrupts

The TMS38030 contains an interrupt prioritizer for other devices on the LAN Adapter bus for presentation of interrupts to the TMS38010 Communications Processor. Other devices assert an interrupt on the TMS38030's LIRQIN0 through LIRQIN2 (LAN Adapter Bus Request In) inputs. The TMS38030 prioritizes the requests and presents an interrupt priority code to the TMS38010 on output pins LIRQOUT0 through LIRQOUT2. The relation between the levels on LIRQIN0 through LIRQIN2 and priority level is given in Table 6.

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TABLE 6. INTERRUPT REQUEST CODES

LIRQIN0	LIRQIN1	LIRQIN2	MEANING
0	0	0	Level-1 Interupt Request
0	0	1	Level-2 Interrupt Request
0	1	0	Level-3 Interrupt Request
0	1	1	Level-4 Interrupt Request
1	0	0	Level-5 Interrupt Request
1	0	1	Level-6 Interrupt Request
1	1	0	Level-7 Interrupt Request
1	1	1	No request

TMS38030 Generated Interrupts

The TMS38030 will assert an interrupt on the LIRQOUT0 through LIRQOUT2 pins as follows:

1. LAN Adapter bus or system bus parity errors are asserted on level 2.
2. The system DMA complete interrupt is asserted on level 6.
3. The interrupt request from the system bus (MSB of the interrupt register is set to one) is asserted on level 7.

test mode

The TMS38030 features a module-in-place test mode for board level testing with the TMS38030 in circuit. This facilitates testing by bed-of-nails testers. This test mode is enabled by tying the $\overline{\text{TEST}}$ pin to ground. This has the effect of driving all outputs of the TMS38030 to a high-impedance state. When not used for testing purposes, this pin should be left unconnected. An internal pullup drives the $\overline{\text{TEST}}$ pin high when not externally connected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range (see Note 3) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. Voltage values are with respect to V_{SS}.
3. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 85°C.

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage	$\overline{TEST}$	V_{CC}			V
		LBCLK1, LBCLK2	3.8			V
		All other inputs	2			V
V_{IL}	Low-level input voltage	$\overline{TEST}$			V_{SS}	V
		LBCLK1, LBCLK2			0.6	V
		All other inputs			0.8	V
I_{OH}	High-level output current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, SADH0-SADH7, SADL0-SADL7, SPH, SPL SHRQ/$\overline{SBRQ}$, SINTR/$\overline{SIRQ}$, $\overline{SDBEN}$, SDDIR, SALE, SXAL, $\overline{SOWN}$			0.4	mA
		$\overline{LBRQS}$, $\overline{LRESET}$, LIRQOUT0-LIRQOUT2, LAL $\overline{LEN}$, LI/$\overline{D}$, LR/$\overline{W}$, LAD0-LAD15, LPH, LPL			0.15	mA
I_{OL}	Low-level output current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, SHRQ/$\overline{SBRQ}$, SINTR/$\overline{SIRQ}$			−2	mA
		SADH0-SADH7, SADL0-SADL7, SPH, SPL, SDDIR			−2.5	mA
		SALE, SXAL			−3.5	mA
		$\overline{SDBEN}$			−5	mA
		$\overline{SOWN}$			−5.5	mA
		$\overline{LBRQS}$, $\overline{LRESET}$, LIRQOUT0-LIRQOUT2, LAL $\overline{LEN}$, LI/$\overline{D}$, LR/$\overline{W}$, LAD0-LAD15, LPH, LPL			−1.7	mA
C_L	Load capacitance	All outputs			100	pF
T_A	Operating free-air temperature (Note 3)		0		70	°C

NOTE 3: Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 85°C.

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electrical characteristics over full range of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.5 V, I_{OH} = max	2.4			V
V_{OL}	Low-level output voltage	All outputs	V_{CC} = 4.5 V, I_{OL} = max			0.45	V
I_{OH}	High-level output current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, SADH0-SADH7, SADL0-SADL7, SPH, SPL, SHRQ/$\overline{SBRQ}$ SINTR/$\overline{SIRQ}$, $\overline{SDBEN}$, SDDIR, SALE, SXAL, $\overline{SOWN}$	V_{CC} = 4.5 V, V_{OH} = 2.4 V			400	μA
		$\overline{LBRQS}$, $\overline{LRESET}$, LIRQOUT0-LIRQOUT2, LAL, $\overline{LEN}$, LI/$\overline{D}$, LR/$\overline{W}$, LAD0-LAD15, LPH, LPL				150	μA
I_{OL}	Low-level output current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, SHRQ/$\overline{SBRQ}$, SINTR/$\overline{SIRQ}$	V_{CC} = 4.5 V, V_{OL} = 0.45 V			−2	mA
		SADH0-SADH7, SADL0-SADL7, SPH, SPL, SDDIR				−2.5	mA
		SALE, SXAL				−3.5	mA
		$\overline{SDBEN}$				−5	mA
		$\overline{SOWN}$				−5.5	mA
		$\overline{LBRQS}$, $\overline{LRESET}$, LIRQOUT0-LIRQOUT2, LAL, $\overline{LEN}$, LI/$\overline{D}$, LR/$\overline{W}$, LAD0-LAD15, LPH, LPL				−1.7	mA

Continued next page.

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electrical characteristics over full range of recommended operating conditions (concluded)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OZL}	Off-state (high-impedance state) output current with low-level voltage applied (outputs only)		V_O = 0.45 V			−20	μA
I_{OZH}	Off-state (high-impedance state) output current with high-level voltage applied (outputs only)		V_O = 2.4 V			20	μA
I_{IL}	Low-level input current	$\overline{TEST}$, LIRQIN0-LIRQIN2	V_I = 0.45 V			−700	μA
		$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, $\overline{SBSSY}$				−450	μA
		All other inputs and I/O's				−20	μA
I_{IH}	High-level input current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/SLDS, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, $\overline{SBBSY}$	V_I = 2.4 V	−100			μA
		All other inputs and I/O's	V_I = V_{CC}			20	μA
I_{CC}	Supply current		V_{CC} = 5 V, T_A = 25°C		190		mA
			V_{CC} = 5.5 V, T_A = 0°C			240	mA
			V_{CC} = 5.5 V, T_C = 85°C			200	mA
C_I	Input capacitance	SBCLK	f = 1 MHz, All other inputs at 0			25	pF
		LBCLK1, LBCLK2 (Note 4)				20	pF
		All other inputs				15	pF

NOTE 4: Input capacitance difference between LBCLK1 and LBCLK2 will not exceed 3 pF.

LAN ADAPTER BUS CLOCK PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
$t_{c(LA)}$	LAN adapter bus cycle time (Note 5)	333	333.7	ns
t_{d1}	Delay time, LBCLK2 low to LBCLK2 no longer low in next cycle	4Q−2	4Q+2	
t_{d2}	Delay time, LBCLK2 rise to LBCLK2 high in next cycle		4Q+9	
t_{d3}	Delay time, LBCLK2 no longer low to LBCLK1 no longer low	Q−3	Q+3	
t_{d4}	Delay time, LBCLK2 rise to LBCLK1 high		Q+9	
t_{d5}	Delay time, LBCLK2 no longer low to LBCLK2 no longer high	2Q−2	2Q+7	
t_{d6}	Delay time, LBCLK2 rise to LBCLK2 low		2Q+12	
t_{d7}	Delay time, LBCLK2 no longer low to LBCLK1 no longer high	3Q−15	3Q−1	
t_{d8}	Delay time, LBCLK2 rise to LBCLK1 low		3Q	
t_{d9}	Delay time, LBCLK1 low to LBCLK2 high	Q		
t_{d10}	Delay time, LBCLK2 high to LBCLK1 high	Q−4		
t_{d11}	Delay time, LBCLK1 high to LBCLK2 low	Q−4		
t_{d12}	Delay time, LBCLK2 low to LBCLK1 low	Q−16		

NOTES: 5. The LAN Adapter bus cycle time is 333.3 ns ±0.1%. This value shall be used for calculations requiring the time between successive rising edges of LBCLK2.
6. Q = 0.25 $t_{c\ (LA)}$.

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LAN ADAPTER BUS READ AND WRITE PARAMETERS

switching characteristics/timing requirements over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q-50		
t_{d17}	Delay time, address valid to LAL no longer high	Q-50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q+74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q+84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q+47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q+47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q−12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q−70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q−4		
t_{su1}	Setup time, Read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q−41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q−21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master (DMA). The values given are valid for both modes.

NOTE 6: Q = 0.25 $t_{c(LA)}$.

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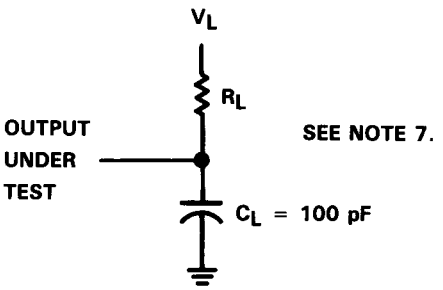
PARAMETER MEASUREMENT INFORMATION



NOTE 7: R_L and V_L are chosen as follows:

$$R_L = \frac{V_{OH} - V_{OL}}{|I_{OL} - I_{OH}|} \qquad V_L = V_{OH} - (I_{OH})(R_L)$$

FIGURE 3. LOAD CIRCUIT

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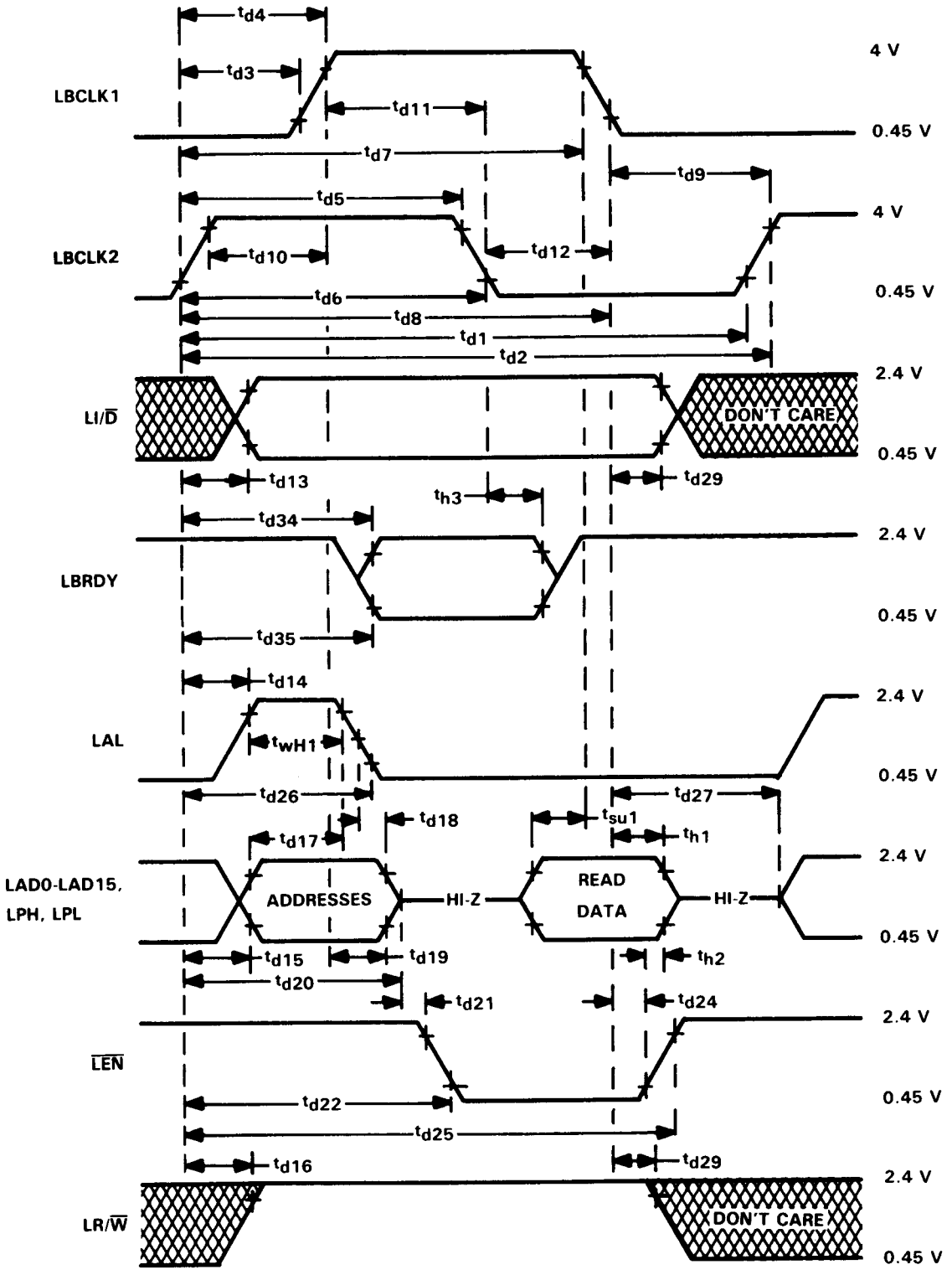
LAN adapter bus read timing



NOTE 8: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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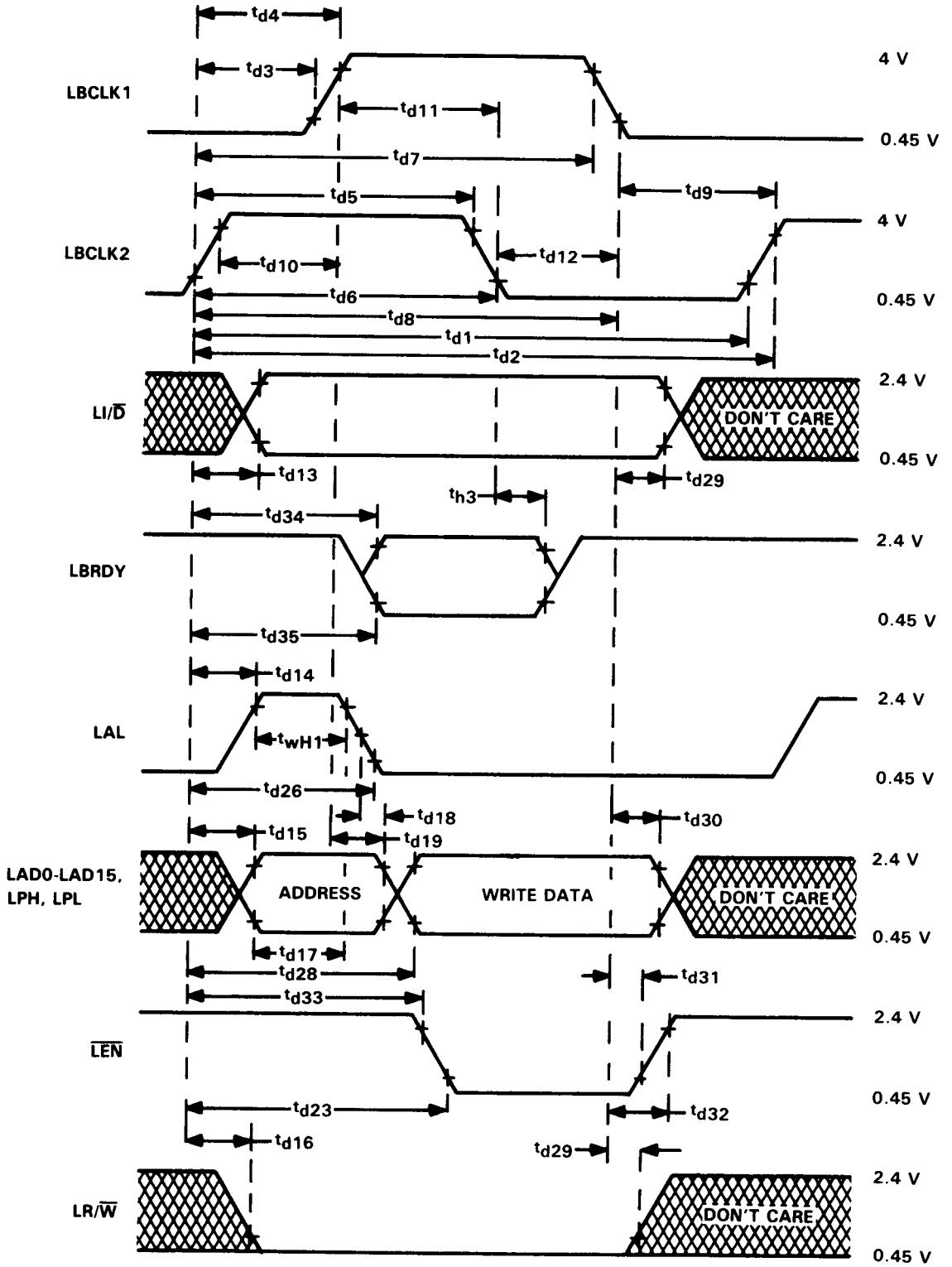
LAN adapter bus write timing



NOTE 8: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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LAN ADAPTER BUS ARBITRATION PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay of $\overline{LBRQS}$ from LBCLK1 low		48	ns
t_{d37}	Delay of $\overline{LBRQS}$ after LBCLK1 rise	0		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer high impedance by TMS38030	2Q – 9		
t_{d39}	Delay time, LBCLK2 rise to LAL driven low by TMS38030		3Q – 15	
t_{d40}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer high impedance by TMS38030	80		
t_{d41}	Delay time, LBCLK2 rise to $\overline{LEN}$ driven high by TMS38030		74	
t_{d42}	Delay time, LBCLK1 low to LR/$\overline{W}$, LI/$\overline{D}$, LAD0-LAD15, LPH, and LPL no longer high impedance by TMS38030	80		

NOTE 6: Q = 0.25 $t_{c(LA)}$.

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d43}	Delay time, LBCLK2 rise to $\overline{LBGRS}$ valid		2Q – 73	ns
t_{d44}	Delay time, LBCLK2 rise to $\overline{LBGRS}$ no longer valid	– 6		
t_{d45}	Delay time, LBCLK2 rise to LAL no longer driven low from old bus master	3Q – 15		
t_{d46}	Delay time, LBCLK2 rise to LAL high impedance from old bus master		4Q – 2	
t_{d47}	Delay time, LBCLK2 rise to $\overline{LEN}$ high impedance from old bus master		74	
t_{d48}	Delay time, LBCLK1 low to LR/$\overline{W}$, LI/$\overline{D}$, LAD0-LAD15, LPH, and LPL high impedance from old bus master		80	

NOTE 6: Q = 0.25 $t_{c(LA)}$.

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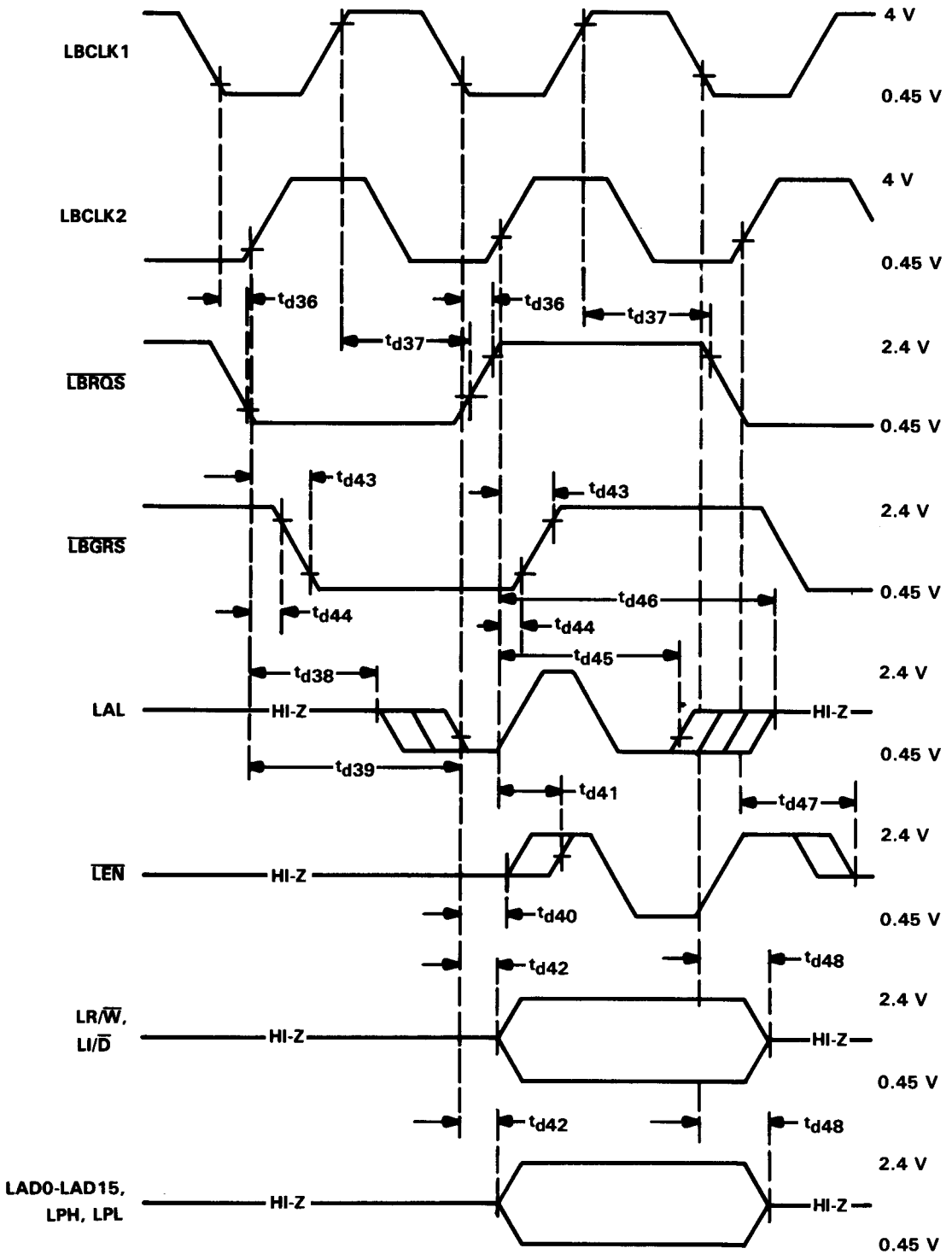
LAN adapter bus arbitration



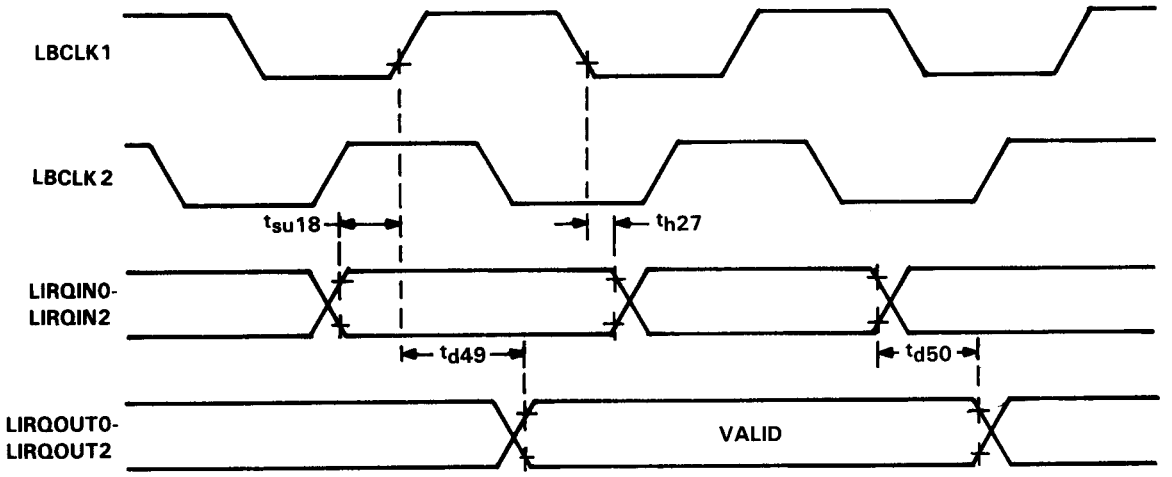
NOTE 9: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d49}	Delay time, LBCLK1 rise to LIRQOUT0-LIRQOUT2 valid		140	ns
t_{su18}	LIRQIN0-LIRQIN2 setup before LBCLK1 rise	0		
t_{h27}	Hold time, LIRQIN0-LIRQIN2 after LBCLK1 low	0		
t_{d50}	Delay time, LIRQIN0-LIRQIN2 no longer valid to LIRQOUT0-LIRQOUT2 no longer valid	0		

interrupt timing



NOTE 10: LIRQOUTs may not follow LIRQINs because the TMS38030 prioritizes LIRQOUT0-LIRQOUT2 outputs between internal TMS38030 interrupts and LIRQIN0-LIRQIN2.

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SYSTEM DMA TIMING PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{wH2}	Pulse duration, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ high	$t_{c(SC)}+$ $t_{w(SCL)}-40$		ns
t_{d51}	Delay from T1 high to $\overline{SUDS}$ and $\overline{SLDS}$ active (read cycle only) (Note 11)		55	
t_{d52}	Delay from T2 high to $\overline{SUDS}$ and $\overline{SLDS}$ active (write cycle only) (Note 11)		55	
t_{d53}	Delay of output data valid to $\overline{SUDS}$ and $\overline{SLDS}$ no longer high	$t_{w(SCL)}-40$		
t_{d54}	Delay from SBCLK low to address valid (Note 11)		45	
t_{d55}	Delay from T1 low to SAD HI-Z		45	
t_{wH3}	Pulse duration, SALE and SXAL high	$t_{c(SC)}-70$		
t_{d56}	Delay from SBCLK high to SALE or SXAL high (Note 11)		70	
t_{h4}	Hold of SALE or SXAL low after $\overline{SRD}$, $\overline{SWR}$, $\overline{SUDS}$, $\overline{SLDS}$, and $\overline{SAS}$ high	$t_{w(SCL)}-40$		
t_{d57}	Delay from T1 high to SALE low or TX high to SXAL low (Note 11)		45	
t_{h5}	Hold of address valid after SALE, SXAL low	$t_{w(SCH)}-30$		
t_{d58}	Delay from T1 low to output data and parity valid		50	
t_{d59}	Delay from T4 low to SAD, SPL, SPH, $\overline{SUDS}$, $\overline{SLDS}$ HI-Z, bus release		100	
t_{h6}	Hold of output data, parity valid after write strobe high	$t_{c(SC)}-60$		
t_{d60}	Delay from SBCLK high to $\overline{SAS}$ low		55	
t_{d61}	Delay from T4 low to $\overline{SBHE}$/SRNW high, bus release		75	
t_{d62}	Delay from T4 low to $\overline{SBHE}$/SRNW HI-Z		145	
t_{d63}	Delay from T3 low to $\overline{SRD}$, $\overline{SUDS}$, $\overline{SLDS}$, $\overline{SAS}$ high on read cycle (Note 12)		60	
t_{d64}	Delay from SBCLK low to $\overline{SWR}$, $\overline{SUDS}$, $\overline{SLDS}$, $\overline{SAS}$ high on write cycle		60	
t_{d65}	Delay from SBCLK high in cycle before T1/TX to $\overline{SOWN}$ low (Note 13)		75	
t_{d66}	Delay from SBCLK high in 2nd cycle after T4 to $\overline{SOWN}$ high (Note 11)		75	
t_{d67}	Delay from TX high to SDDIR low in DMA read cycle (Note 11)		75	
t_{d68}	Delay from T4 low in last read cycle to SDDIR high (Note 11)		75	
t_{d69}	Delay from T3 low to $\overline{SDBEN}$ high, read cycle (Note 11)	Note 12	75	
t_{d70}	Delay from T4 high to $\overline{SDBEN}$ high, write cycle (Note 11)		60	
t_{h7}	Hold of $\overline{SDBEN}$ low after write data strobe high	$t_{w(SCL)}-40$		
t_{d71}	Delay from SAD HI-Z to $\overline{SRD}$ low	0		
t_{d72}	Delay from T1 low to $\overline{SRD}$ low		70	
t_{d73}	Delay from T1 low to $\overline{SWR}$ low		55	
t_{h8}	Hold of SAD HI-Z after T4 low	0		

Continued next page.

NOTES: 11. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including HI-Z) until the start of that SBCLK transition.
12. On read cycle, the read strobe remains active until the internal sample of incoming data is complete. Input data may be removed when either the read strobe or $\overline{SDBEN}$ becomes no longer active.
13. While SIF DMA controls are active (i.e., $\overline{SOWN}$ is asserted), the $\overline{SCS}$ input is disabled.

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switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3) (concluded)

	PARAMETER	MIN	MAX	UNIT
t_{d74}	Delay from SBCLK high to bus request valid (Note 11)		60	ns
t_{wL1}	Pulse duration, $\overline{SRD}$ low	$2t_{c(SC)}-40$		
t_{wL2}	Pulse duration, $\overline{SWR}$ low	$2t_{c(SC)}-40$		
t_{su2}	Setup of address valid before SALE, SXAL no longer high	$t_{w(SCL)}-43$		
t_{su3}	Setup of address valid before $\overline{SAS}$ no longer high	$t_{w(SCL)}-32$		
t_{d75}	Delay from T2 high to $\overline{SDBEN}$ low in read cycle (Note 11)		80	
t_{d76}	Delay from T1 high to $\overline{SDBEN}$ low in write cycle (Note 11)		60	
t_{wL3}	Pulse duration, $\overline{SAS}$ on read and write; pulse duration, $\overline{SUDS}$ and $\overline{SLDS}$ on read	$2t_{c(SC)}+t_{w(SCH)}-50$		
t_{su4}	Setup of control signals HI-Z before $\overline{SOWN}$ no longer low	0		
t_{d77}	Delay from TX high to data strobes high, bus acquisition (Note 11)		70	
t_{h9}	Hold of data strobe HI-Z after $\overline{SOWN}$ low, bus acquisition	$t_{c(SC)}-70$		
t_{wL4}	Pulse duration, $\overline{SUDS}$ and $\overline{SLDS}$ on write	$t_{c(SC)}+t_{w(SCH)}-50$		
t_{d78}	Delay from $\overline{SRESET}$ low to $\overline{LRESET}$ low, V_{CC} at V_{CC} min		100	
t_{d79}	Delay from $\overline{SRESET}$ high to $\overline{LRESET}$ high		200	
t_{d80}	Delay from reaching minimum V_{CC} during power-up to valid SBCLK, LBCLK1, LBCLK2		90	ms

NOTE 11: Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including HI-Z) until the start of that SBCLK transition.

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timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER			MIN	MAX	UNIT
$t_{c(SC)}$	Cycle time of SBCLK (Note 14)	TMS38030-6	166	500	ns
		TMS38030-8	125	500	
		TMS38030-10	100	500	
$t_{w(SCL)}$	Pulse duration, SBCLK low	TMS38030-6	65		ns
		TMS38030-8	55		
		TMS38030-10	45		
$t_{w(SCH)}$	Pulse duration, SBCLK high	TMS38030-6	65		ns
		TMS38030-8	55		
		TMS38030-10	45		
$t_{t(SC)}$	Transition time of SBCLK			10	ns
t_{su5}	Setup of input data valid before T3 no longer high		15		ns
t_{h10}	Hold of input data valid after T3 low, if t_{h11} and t_{h12} not met		40		ns
t_{h11}	Hold of input data valid after data strobe no longer low		0		ns
t_{h12}	Hold of input data valid after $\overline{SDBEN}$ no longer low		0		ns
t_{su6}	Setup of asynchronous input before SBCLK no longer high to guarantee recognition		20		ns
t_{h13}	Hold of asynchronous input after SBCLK low to guarantee recognition		40		ns
t_{h14}	Hold of $\overline{SBRLS}$ low after $\overline{SOWN}$ high		0		ns
t_{su7}	Setup of $\overline{SBERR}$ low before $\overline{SRDY}/\overline{SDTACK}$ no longer high, if t_{su6} not met		65		ns
t_{su8}	Setup of $\overline{SRDY}/\overline{SDTACK}$ low before data valid if t_{su6} not met			45	ns
t_{wL5}	Pulse duration, $\overline{SRESET}$ and $\overline{LRESET}$ asserted with minimum V_{CC} or greater applied and valid LBCLKs		14		μs
t_{wL6}	Pulse duration, $\overline{SRESET}$ asserted after V_{CC} above V_{CC} (min) at power-up		100		ms
$t_{r(LRS)}$	Rise time of $\overline{LRESET}$			100	ns
$t_{r(VCC)}$	Rise time from 1.2 volts to V_{CC} minimum, at the V_{CC} pins		1		ms

NOTE 14: The MXTALOUT signal output of the TMS38010 cannot be used as the SBCLK input.

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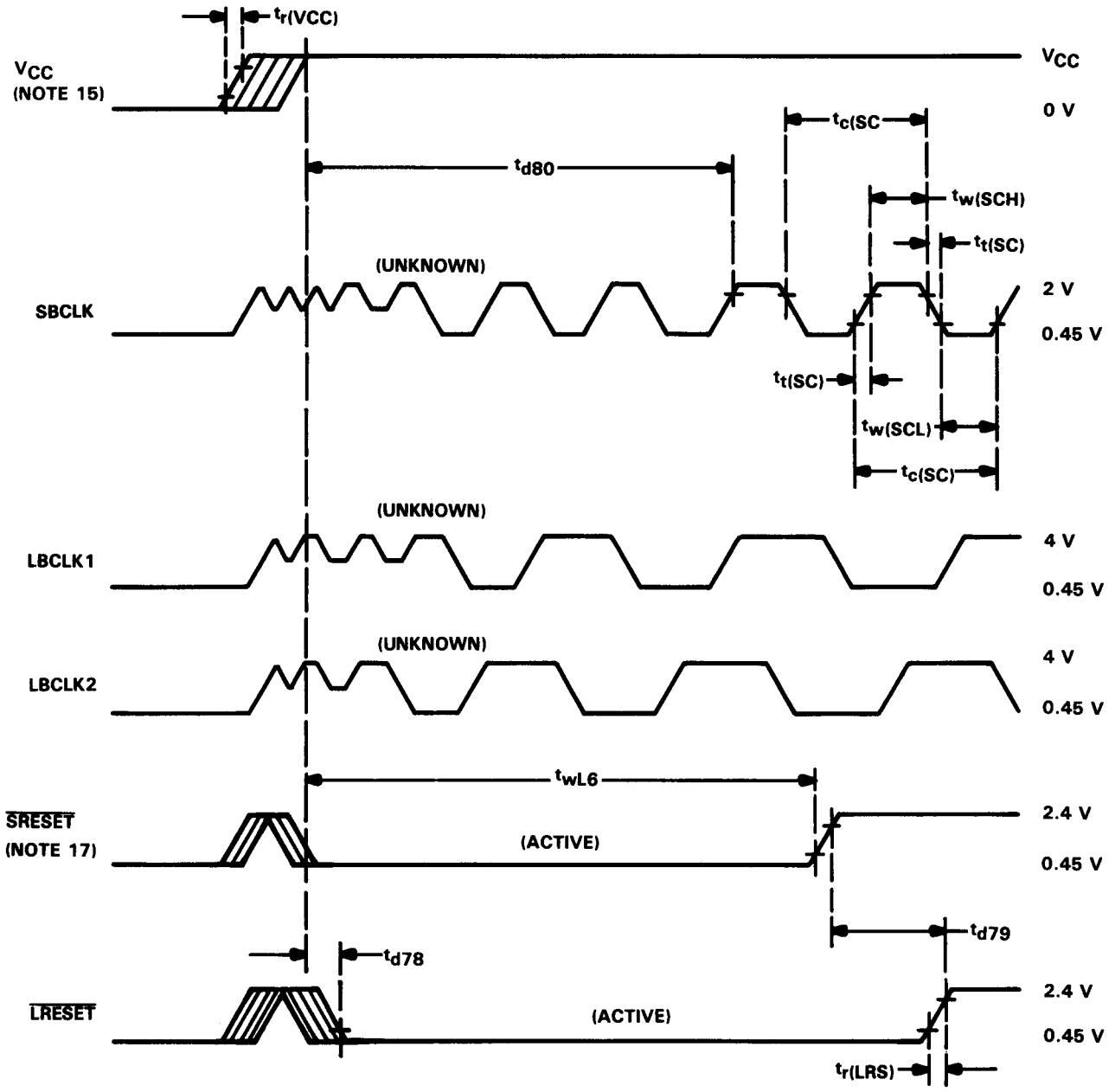
power-up, SBCLK, LBCLK, $\overline{\text{SRESET}}$, and $\overline{\text{LRESET}}$ timing

power on



NOTES: 15. A minimum one second interval between power off and power on is required for correct initialization of the TMS38030.
16. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for SBCLK, $\overline{\text{SRESET}}$, and $\overline{\text{LRESET}}$ are 2 V and 0.8 V. The timing reference points for V_{CC} are 4.5 V and 1.2 V.
17. During power-up, $\overline{\text{SRESET}}$ is undefined (asserted) prior to 1.2 V applied to the V_{CC} pins of the TMS38030. $\overline{\text{SRESET}}$ must remain asserted from V_{CC} = 1.2 V to V_{CC} minimum. The TMS38030 must not be accessed from either the system or LAN Adapter bus interface within 3 μs of the de-assertion of $\overline{\text{SRESET}}$. This is primarily a test limitation since currently available processors cannot violate this condition.

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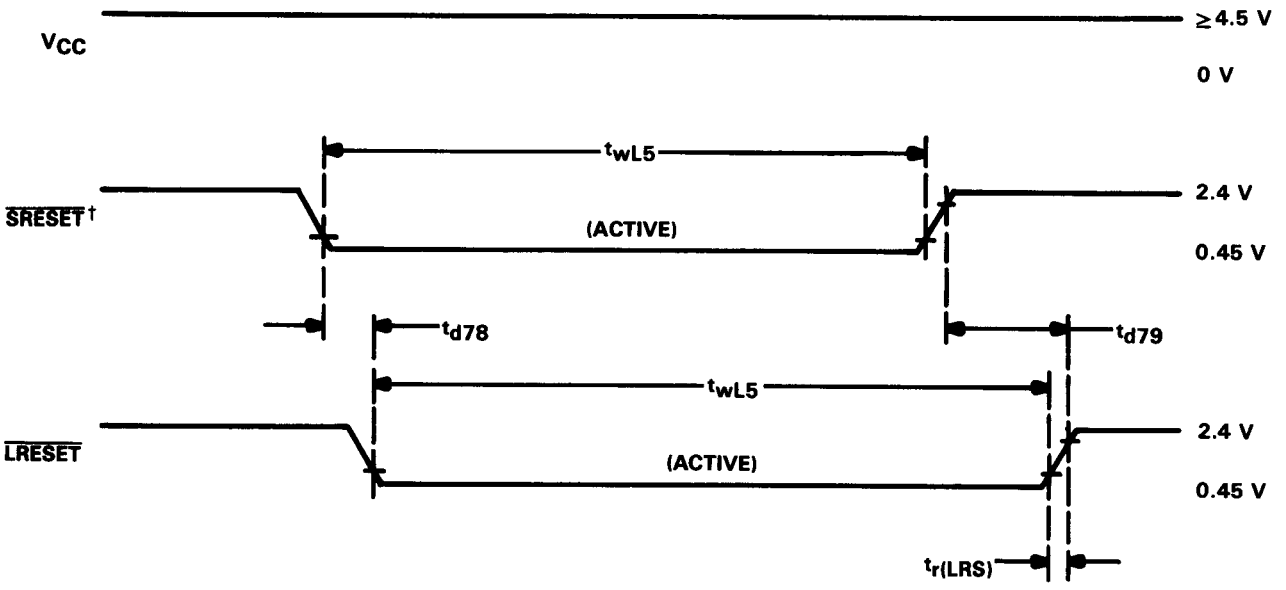
$\overline{\text{SRESET}}$ and $\overline{\text{LRESET}}$ timing

operational



NOTE 18: The timing reference points for $\overline{\text{SRESET}}$ and $\overline{\text{LRESET}}$ are 2 V and 0.8 V.
†Following a low-to-high transition of $\overline{\text{SRESET}}$, $\overline{\text{SRESET}}$ must remain high for a minimum of 20 milliseconds before again driven low.

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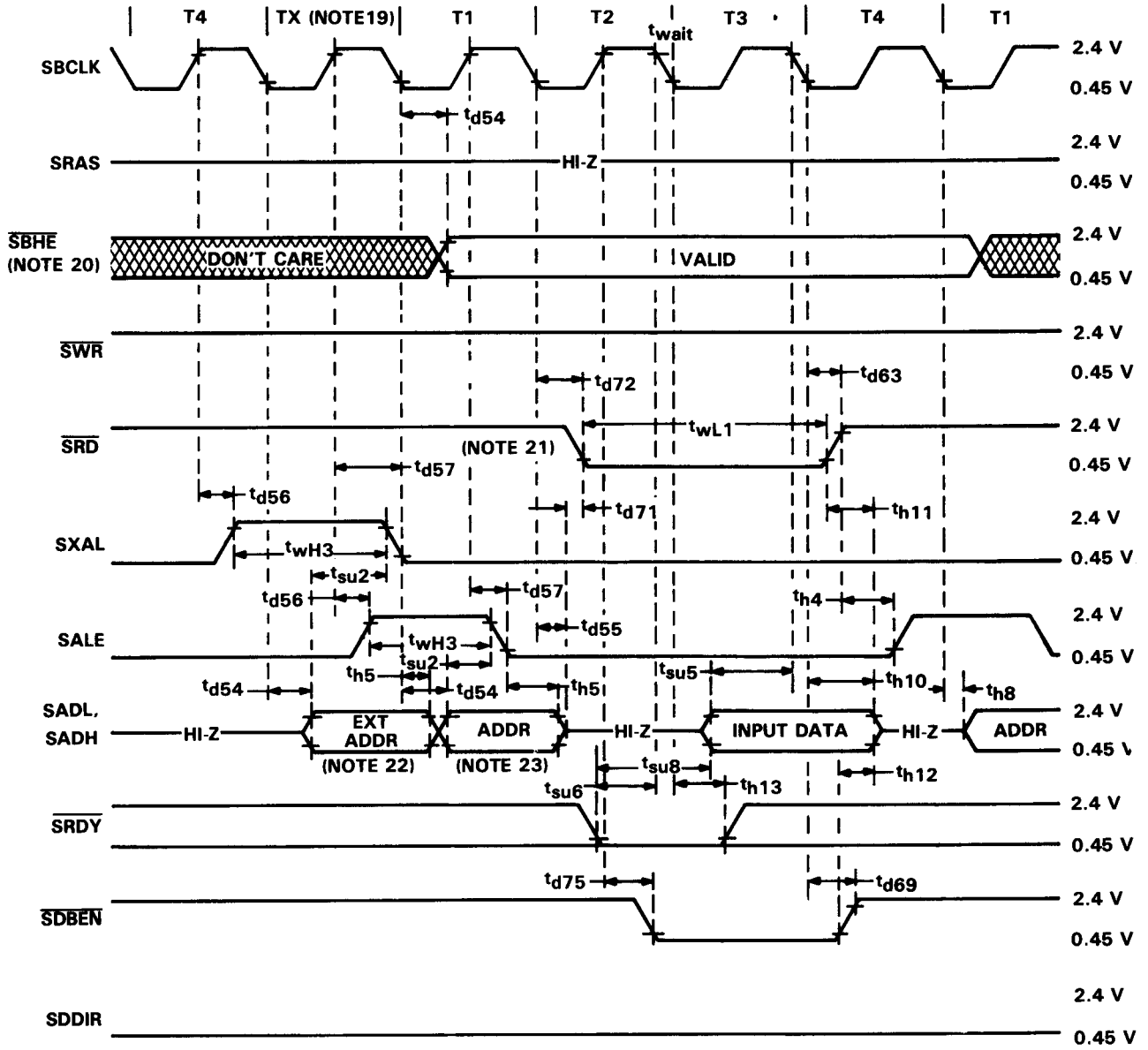
808X mode DMA read timing



NOTES: 19. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer, and whenever the increment of the address carries beyond the least-significant 8 bits.
20. In 8-bit 808X Mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
21. If the TX state is not present, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ are asserted in the T1 state.
22. In state TX, SADH continues to output the most-significant byte of the address.
23. In 8-bit mode, the most-significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to t_{h6}, i.e., held after T4 high.

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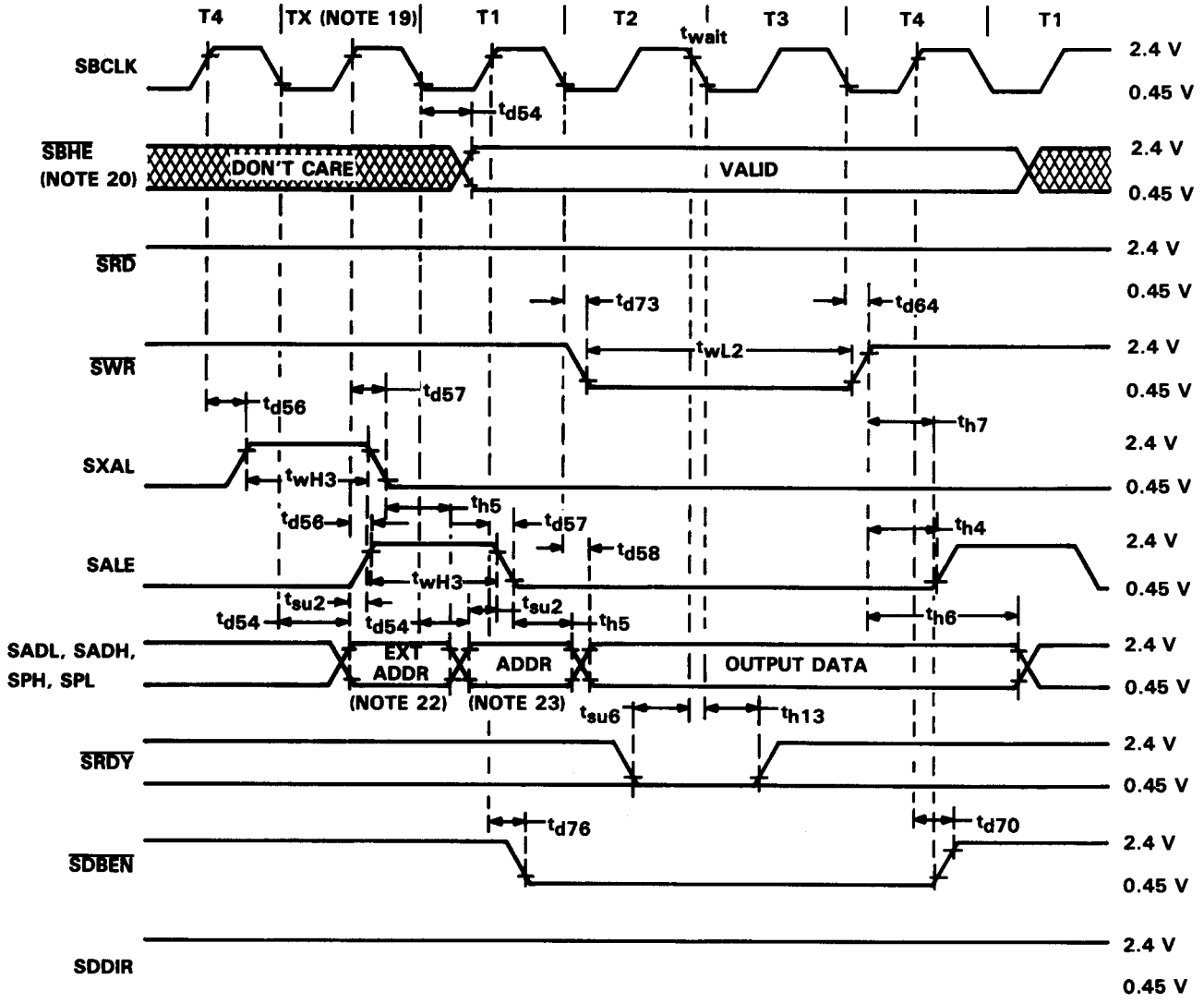
808X mode DMA write timing

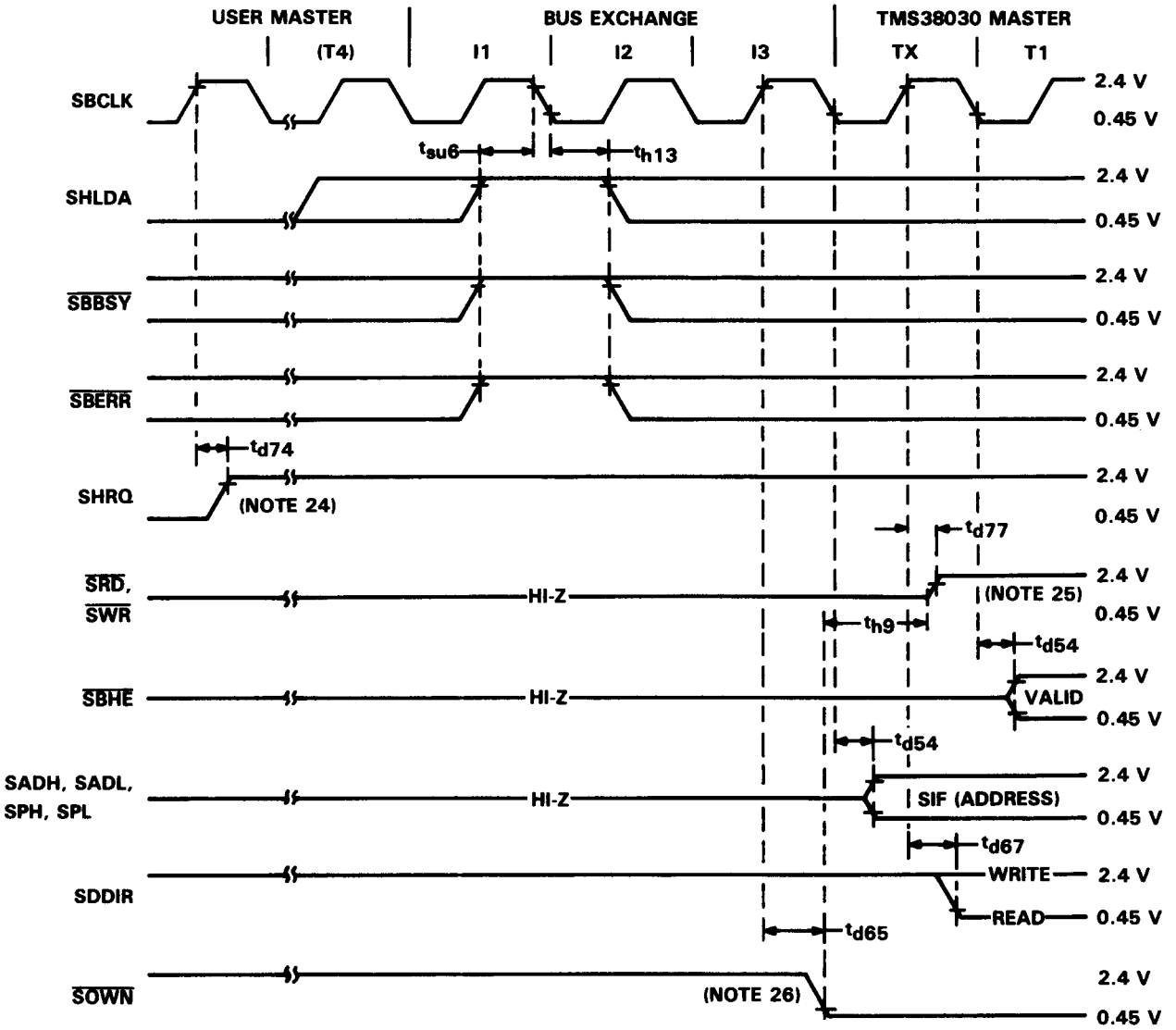


NOTES: 19. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer, and whenever the increment of the address carries beyond the least-significant 8 bits.
20. In 8-bit 808X Mode, $\overline{\text{SBHE}}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
22. In state TX, SADH continues to output the most-significant byte of the address.
23. In 8-bit mode, the most-significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to t_{h6}, i.e., held after T4 high.

A

808X mode bus arbitration timing

TMS38030 takes control of system bus from user processor



NOTES: 24. SHLDA/$\overline{\text{SBGR}}$ must be sampled in its deasserted state on the falling edge of SBCLK. The TMS38030 will then assert SHRQ/$\overline{\text{SBRQ}}$ on the second subsequent rising edge of SBCLK.

25. When taking over the system bus, the TMS38030 drives all data strobes high for the time between T1 high and the edge at which the strobes are driven low. The logical value of the strobes in this period is not defined.

26. While TMS38030 DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

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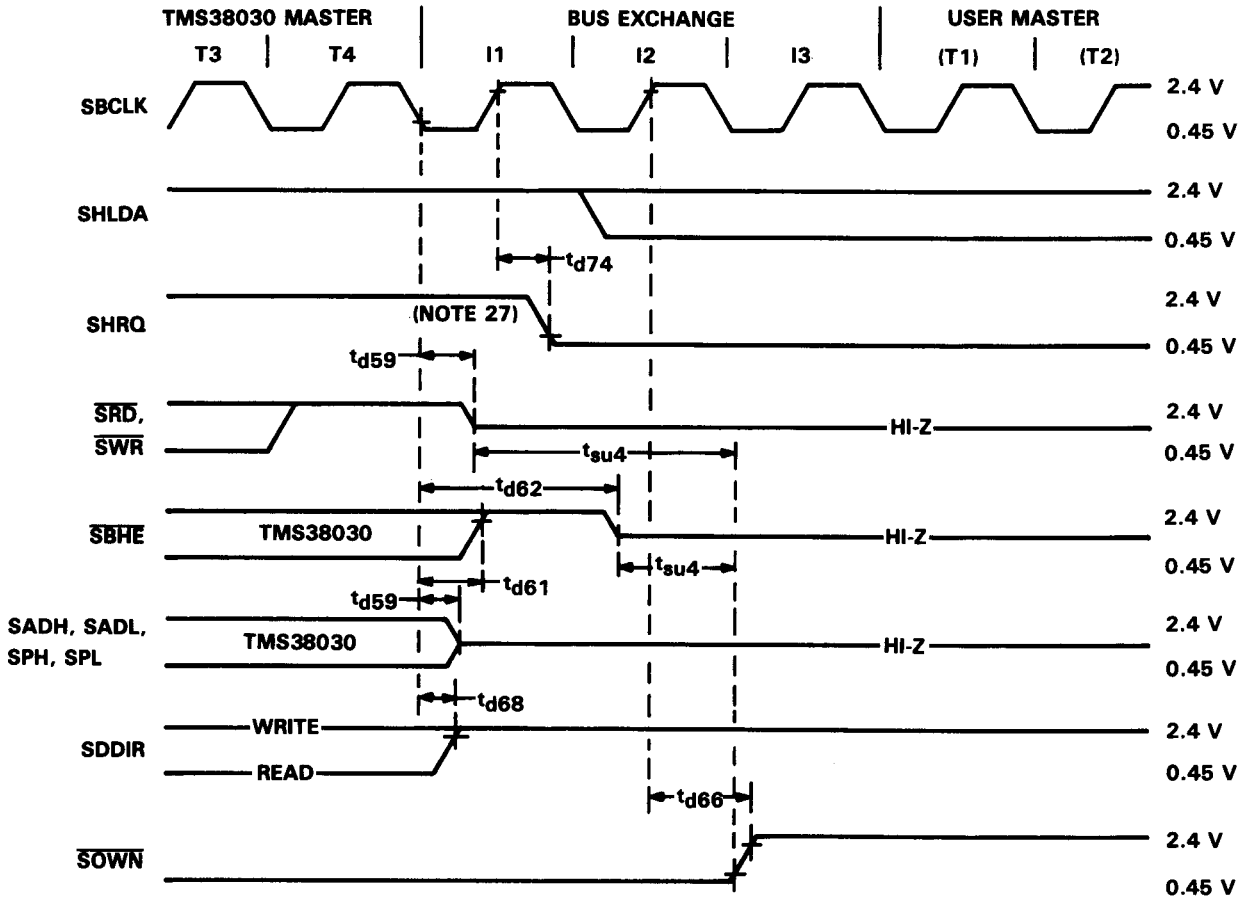
808X mode bus arbitration timing

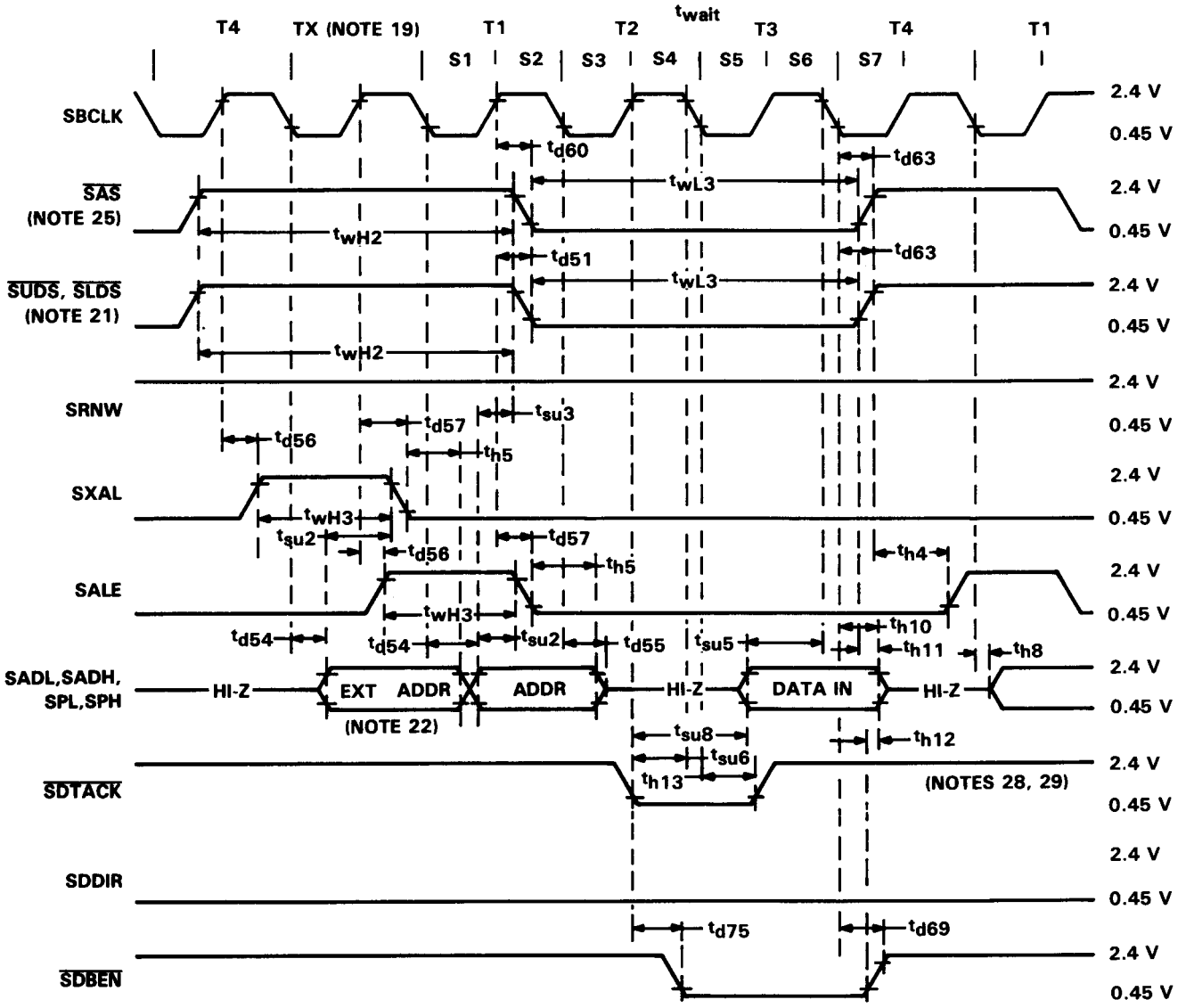
TMS38030 returns control to user processor



NOTE 27: In 808X Mode, the TMS38030 deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 680XX Mode, the TMS38030 deasserts $\overline{\text{SBRQ}}$ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

A

680XX mode DMA read timing



NOTES: 19. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer, and whenever the increment of the address carries beyond the least-significant 8 bits.
21. If the TX state is not present, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ are asserted in the T1 state.
22. In state TX, SADH continues to output the most-significant byte of the address.
28. $\overline{SDTACK}$ is not sampled to verify that it is deasserted.
29. 680XX-style bus slaves hold $\overline{SDTACK}$ active until the bus master deasserts $\overline{SAS}$. In this case, the slave still meets t_{h13}.

A

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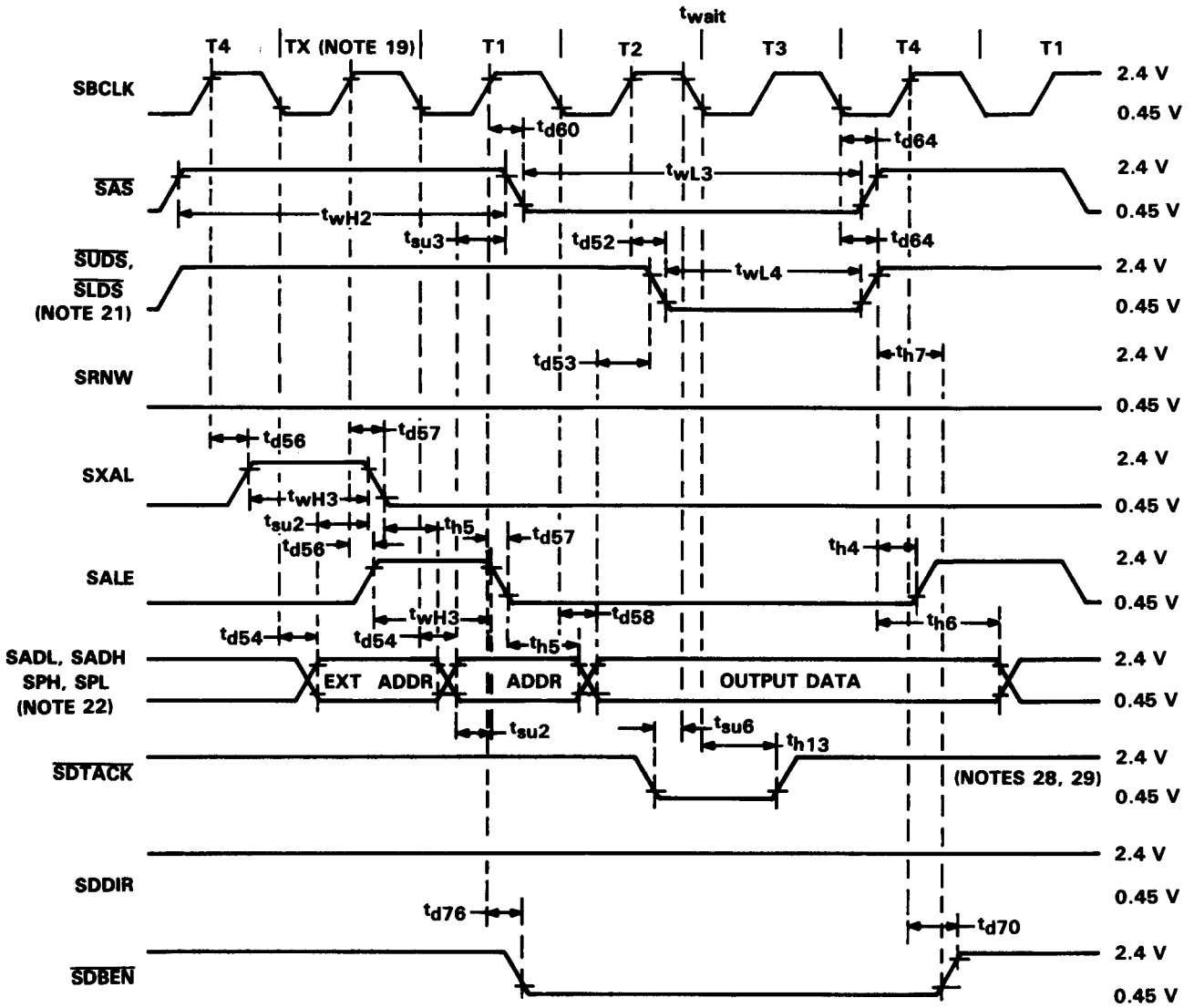
680XX mode DMA write timing



NOTES: 19. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer, and whenever the increment of the address carries beyond the least-significant 8 bits.

21. If the TX state is not present, $\overline{SAS}$,$\overline{SUDS}$, and $\overline{SLDS}$ are asserted in the T1 state.

22. In state TX, SADH continues to output the most-significant byte of the address.

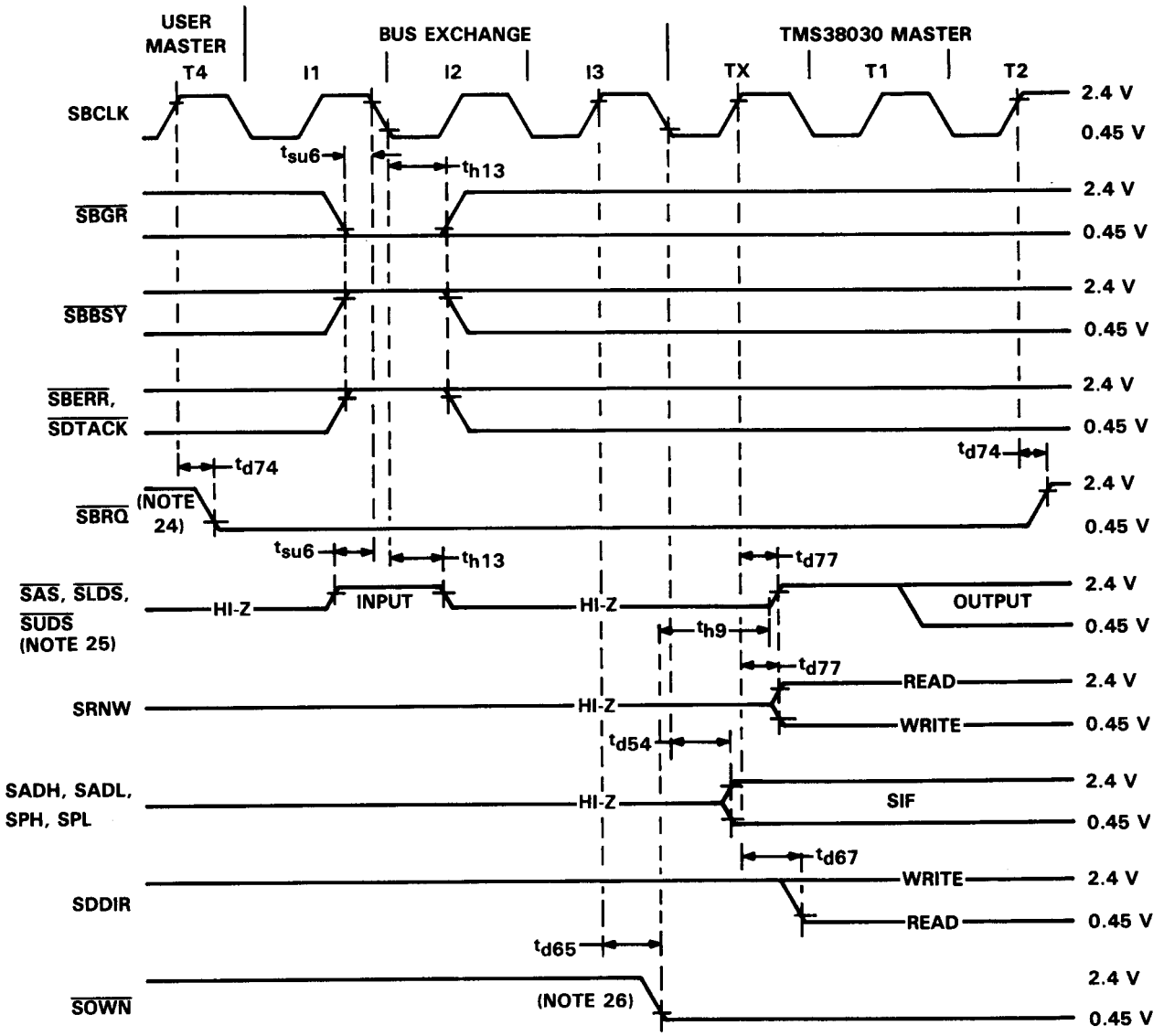
28. $\overline{SDTACK}$ is not sampled to verify that it is deasserted.

29. 680XX-style bus slaves hold $\overline{SDTACK}$ active until the bus master deasserts $\overline{SAS}$. In this case, the slave still meets t_{h13}.

A

680XX mode bus arbitration timing

TMS38030 takes control of system bus from user processor



NOTES: 24. SHLDA/$\overline{\text{SBGR}}$ must be sampled in its deasserted state on the falling edge of SBCLK. The TMS38030 will then assert SHRQ/$\overline{\text{SBRQ}}$ on the second subsequent rising edge of SBCLK.

25. When taking over the system bus, the TMS38030 drives all data strobes high for the time between T1 high and the edge at which the strobes are driven low. The logical value of the strobes in this period is not defined.

26. While TMS38030 DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

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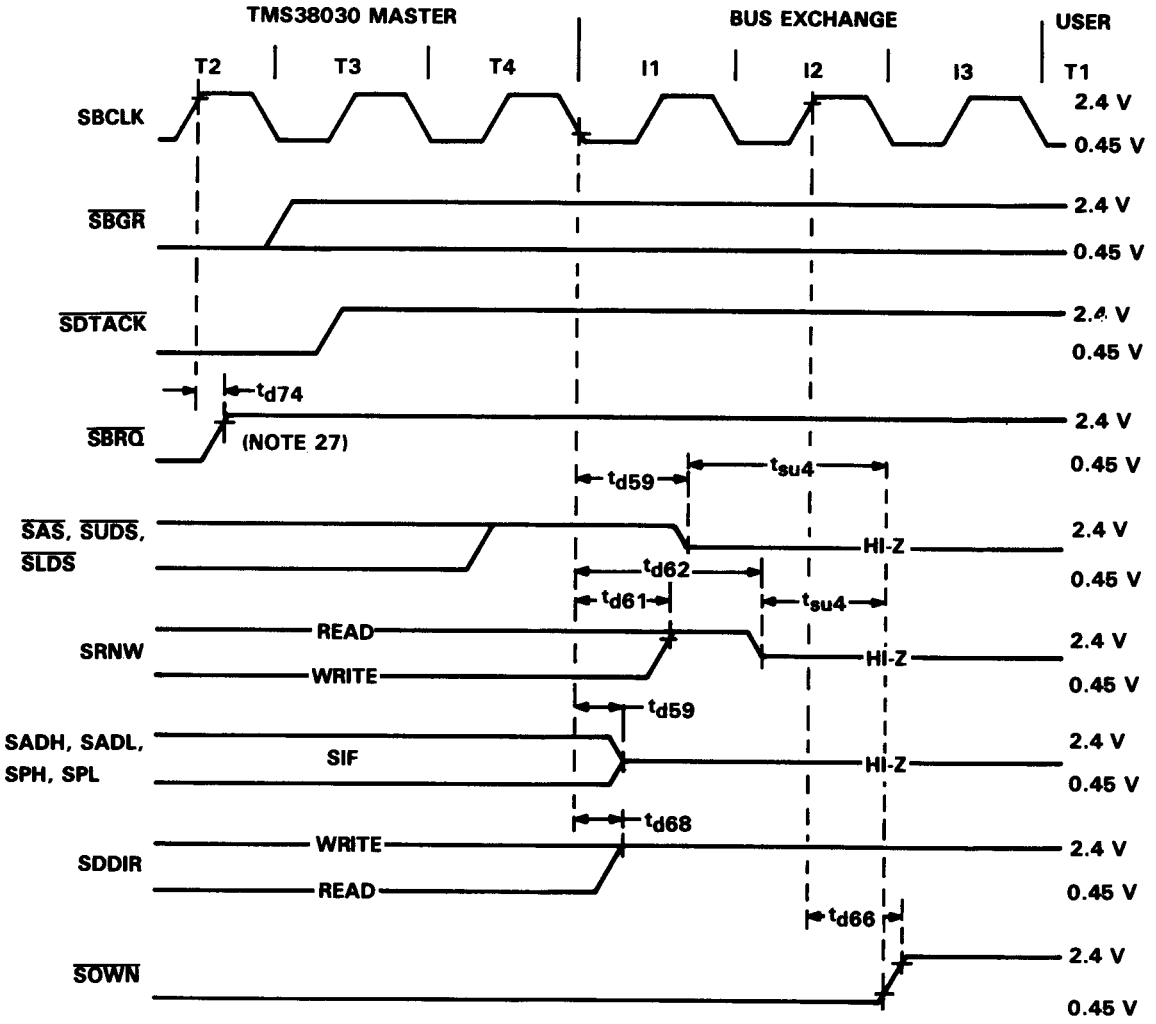
680XX mode bus arbitration timing

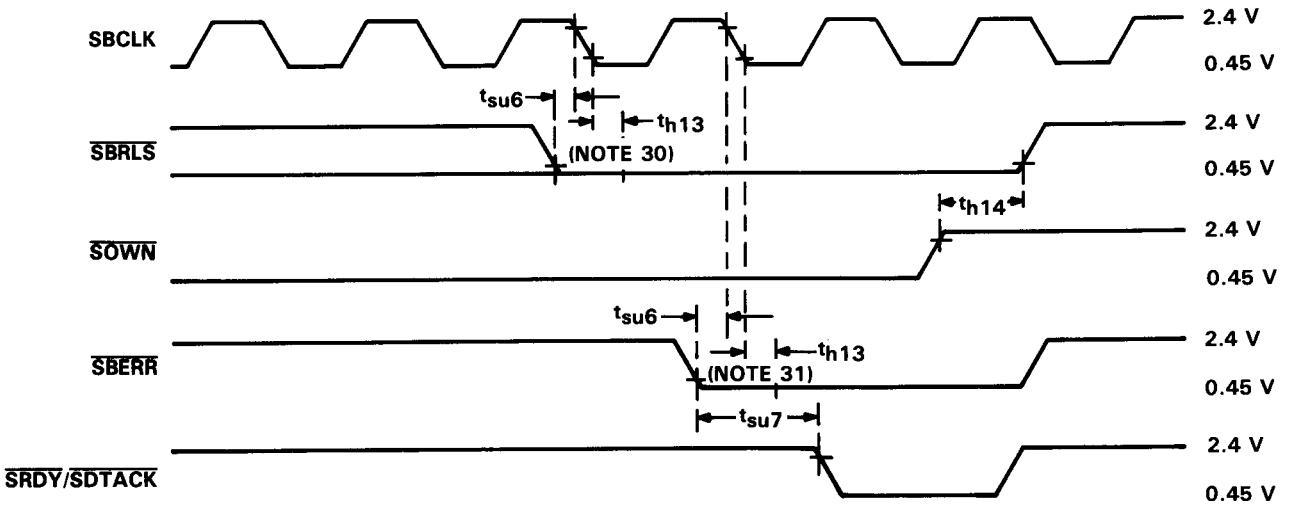
TMS38030 returns control to user processor



NOTE 27: In 808X Mode, the TMS38030 deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 680XX Mode, the TMS38030 deasserts $\overline{\text{SBRQ}}$ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

A

bus release and error timing



NOTES: 30. The TMS38030 ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the system bus, then when it detects the assertion of $\overline{\text{SBRLS}}$ it will complete any internally started DMA cycle and relinquish control of the bus. If no DMA transfer has internally started, then the TMS38030 will release the bus before starting another.

If $\overline{\text{SBRLS}}$ is asserted prior to state T1, then that DMA cycle will be the last cycle before the TMS38030 releases the bus. If $\overline{\text{SBRLS}}$ is asserted after state T1 in a DMA cycle, the TMS38030 will complete the current cycle and the next cycle before releasing the system bus.

The TMS38030 will deassert SHRQ/$\overline{\text{SBRQ}}$ during state I1 of the bus exchange cycle. SHLDA/$\overline{\text{SBGR}}$ must be deasserted to cause the TMS38030 to re-request the bus.

31. If $\overline{\text{SBERR}}$ is asserted when the TMS38030 controls the system bus, then the current bus transfer is completed, regardless of the value of $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$. In this case, the TMS38030 will then release control of the system bus. The TMS38030 ignores $\overline{\text{SBERR}}$ if it is not performing a DMA cycle. When $\overline{\text{SBERR}}$ is properly asserted, however, the TMS38030 releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the LAN Adapter bus and DMA stops on the LAN Adapter bus side. The value of SDMAADR, LDMAADR, and SDMALEN registers in the TMS38030 are not defined after a system bus error.

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SYSTEM DIO TIMING PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{h15}	Hold of SAD HI-Z after read strobe no longer high	0		ns
t_{su9}	Setup of output data valid before $\overline{SRDY}$/SDTACK no longer HI-Z	25		ns
t_{d81}	Delay from read strobe high to SAD HI-Z		80	ns
t_{h16}	Hold of output data valid after read strobe or $\overline{SCS}$ no longer low	0		ns
t_{d82}	Delay from data strobe or $\overline{SCS}$ high to $\overline{SRDY}/\overline{SDTACK}$ high		60	ns
t_{d83}	Delay from SBCLK edge high at which $\overline{SRDY}/\overline{SDTACK}$ driven in first DIO access to SIFD or SIFADR register to $\overline{SRDY}/\overline{SDTACK}$ low in immediately following access to SIFD or SIFADR		4.9 μs $+t_{c(SC)}$	μs
t_{h17}	Hold of $\overline{SRDY}/\overline{SDTACK}$ HI-Z after SBCLK no longer low, read cycle (Note 32)	0		ns
t_{h18}	Hold of $\overline{SRDY}/\overline{SDTACK}$ HI-Z after $\overline{SDBEN}$ high, write cycle (Note 32)	0		ns
t_{d84}	Delay from SBCLK high to $\overline{SRDY}/\overline{SDTACK}$ low, read cycle (Note 32)		80	ns
t_{d85}	Delay from SBCLK high to $\overline{SRDY}/\overline{SDTACK}$ low, write cycle (Note 32)		130	ns
t_{d86}	Delay from data strobe high to $\overline{SRDY}/\overline{SDTACK}$ HI-Z (Note 33)		100	ns
t_{d87}	Delay from write strobe low to SDDIR low (Note 34)		80	ns
t_{d88}	Delay from write strobe high to SDDIR high (Note 34)		80	ns
t_{h19}	Hold of SDDIR low after write data strobe no longer low	0		ns
t_{d89}	Delay from read strobe low to $\overline{SDBEN}$ low (Note 34)		80	ns
t_{d90}	Delay from read strobe high to $\overline{SDBEN}$ high (Note 34)		75	ns
t_{d91}	Delay from SBCLK high to $\overline{SDBEN}$ high, write cycle (Note 32)		70	ns
t_{d92}	Delay from SBCLK high to $\overline{SDBEN}$ low in write cycle		55	ns
t_{su10}	Setup of SDDIR low to $\overline{SDBEN}$ no longer high	$2t_{c(SC)}+$ $t_{w(SCL)}-125$		ns

NOTES: 32. On DIO read cycles, the cycle begins with a "sample point" which is the falling edge of SBCLK at which the TMS38030 recognizes the assertion of $\overline{SCS}$, the assertion of a read data strobe, and the deassertion of an internal "busy" signal. The TMS38030 asserts $\overline{SDBEN}$ asynchronously when $\overline{SCS}$, the read data strobe, and the internal busy signal are at the appropriate level.

On DIO write cycles, the sample point is defined as the falling edge of SBCLK at which the TMS38030 recognizes that $\overline{SCS}$ is asserted, the write data strobe is asserted, and the internal DIO "busy" signal is deasserted. The TMS38030 asserts $\overline{SDBEN}$ on the third rising edge after the sample point.

33. Internal logic will drive $\overline{SRDY}/\overline{SDTACK}$ high and verify that it has reached a valid high level before tristating the signal.
34. For 680XX mode, skew between $\overline{SLDS}$ and $\overline{SUDS}$ must not exceed 10 ns. Providing this limitation is observed, all events referenced to a data strobe edge are to the later occurring edge. Events defined by two data strobe edges, parameter t_{wH4}, are measured between latest and earlier edges.

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timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{wH4}	Pulse duration, data strobe high between DIO accesses	100		ns
t_{su11}	Setup of asynchronous input to SBCLK no longer high in order to guarantee recognition (Note 34)	35		
t_{h20}	Hold of asynchronous input after SBCLK low to guarantee strobe not recognized.	45		
t_{h21}	Hold of $\overline{SCS}$ or data strobe low after $\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z (Note 35)	0		
t_{d93}	Delay from $\overline{SRDY}/\overline{SDTACK}$ low to either $\overline{SCS}$ or data strobe high (Note 36)		1000	
t_{wH5}	Pulse duration, SRAS high	40		
t_{su12}	Setup of write data valid before SBCLK no longer low (Note 37)	105		
t_{d94}	Delay from write strobe low to input write data valid (Note 37)		$4t_{c(SC)}+t_{w(SCL)}-150$	
t_{h22}	Hold of write data valid after $\overline{SDBEN}$ NO LONGER LOW (Note 38)	0		
t_{su13}	Setup of SRS0-SRS2, $\overline{SCS}$ (not shown) and $\overline{SBHE}$ to SRAS no longer high	18		
t_{h23}	Hold of SRS0-SRS2, $\overline{SCS}$ (not shown) and $\overline{SBHE}$ after SRAS low	20		
t_{su14}	Setup of SRAS high to data strobe no longer high	42		
t_{su15}	Setup of register address before data strobe no longer high	20		
t_{h24}	Hold of register address valid after $\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z (Note 35)	0		
t_{su16}	Setup of SRNW before data strobe no longer high	40		
t_{su17}	Setup of inactive data strobe high to active data strobe no longer high	100		
t_{h25}	Hold of SRNW after $\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z (Note 38)	0		
t_{h26}	Hold of inactive data strobe high after active data strobe high	100		
t_{wH6}	Pulse duration, $\overline{SCS}$ and $\overline{SIACK}$ both high	100		
t_{wL7}	Pulse duration, $\overline{SIACK}$ low on first pulse of two pulses in 808X Mode	150		

NOTES: 34. For 680XX mode, skew between $\overline{SLDS}$ and $\overline{SUDS}$ must not exceed 10 ns. Providing this limitation is observed, all events referenced to a data strobe edge are to the later occurring edge. Events defined by two data strobe edges, parameter t_{wH4}, are measured between latest and earlier edges.

35. In 808X Mode, SRAS may be used to strobe the values of $\overline{SBHE}$, SRS0-SRS2 and $\overline{SCS}$. When used to do so, SRAS must meet parameter t_{su14} and $\overline{SBHE}$, SRS0-SRS2, and $\overline{SCS}$ must meet parameter t_{su13}. If SRAS is strapped high, then parameters t_{su14} and t_{su13} are irrelevant.

36. The system must provide sufficient delay between TMS38030's assertion of $\overline{SRDY}/\overline{SDTACK}$ and the system's deassertion of the data strobe(s) in order to allow the TMS38030 to hold SDDIR valid after $\overline{SDBEN}$ is inactive.

37. Write data is sampled on the fifth rising edge of SBCLK following the recognition of a write data strobe on a falling edge of SBCLK.

38. Since $\overline{SDBEN}$ is deasserted before $\overline{SRDY}/\overline{SDTACK}$ is asserted, external logic may remove write data when $\overline{SRDY}/\overline{SDTACK}$ is asserted. Register addresses and SRNW may also be deasserted when $\overline{SRDY}/\overline{SDTACK}$ is asserted. For testing purposes, the timing point "$\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z" refers to the 2 V point of the falling edge of the $\overline{SRDY}/\overline{SDTACK}$ signal with a 10 kΩ pullup to V_{CC}.

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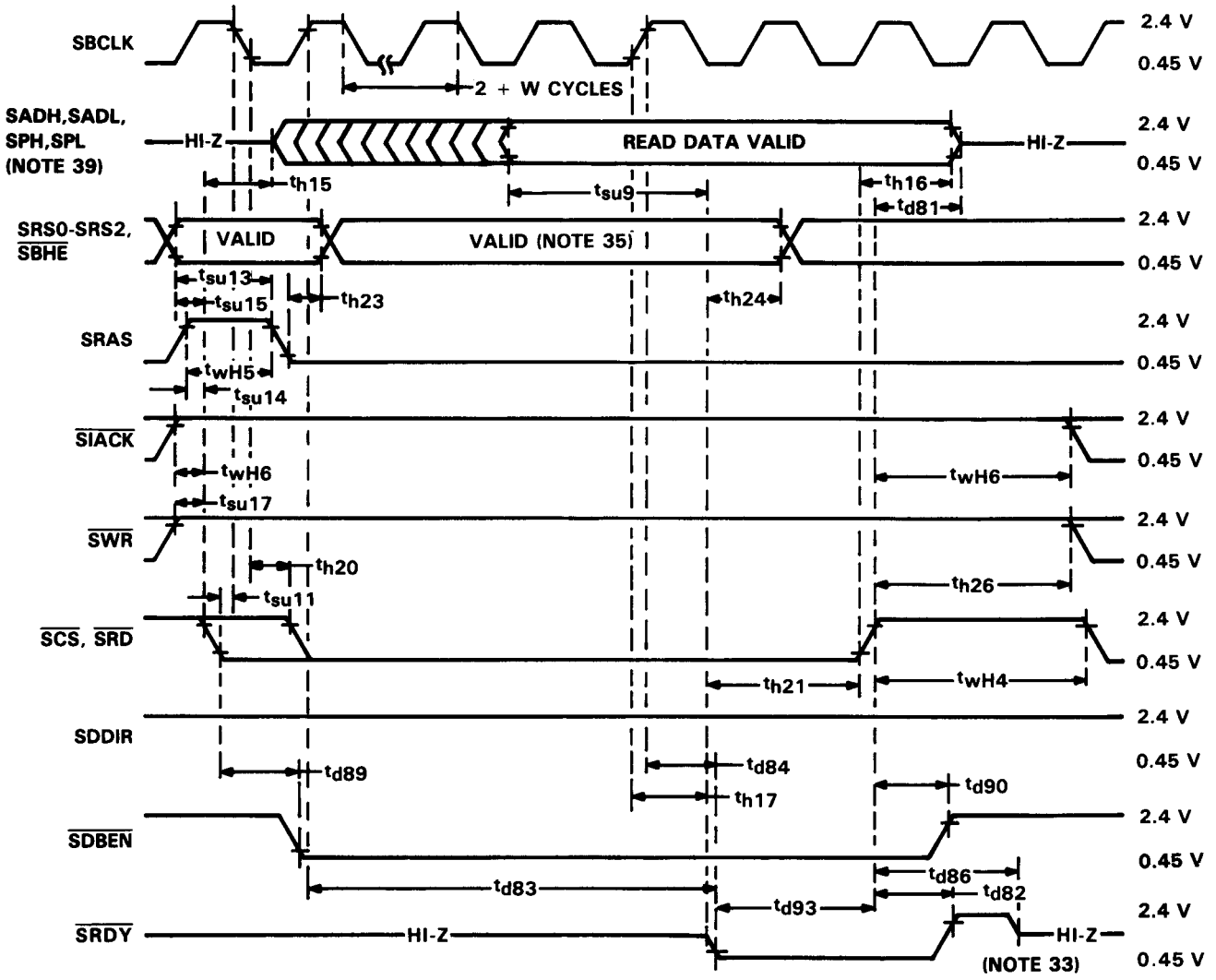
808X mode DIO read timing



NOTES: 33. Internal logic will drive $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$ high and verify that it has reached a valid high level before tristating the signal.
35. In 808X Mode, SRAS may be used to strobe the values of $\overline{\text{SBHE}}$, SRS0-SRS2 and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter t_{su14} and $\overline{\text{SBHE}}$, SRS0-SRS2, and $\overline{\text{SCS}}$ must meet parameter t_{su13}. If SRAS is strapped high, then parameters t_{su14} and t_{su13} are irrelevant.
39. In 8-bit mode DIO reads, the SADH lines will be tristated during the data portion of the cycle.

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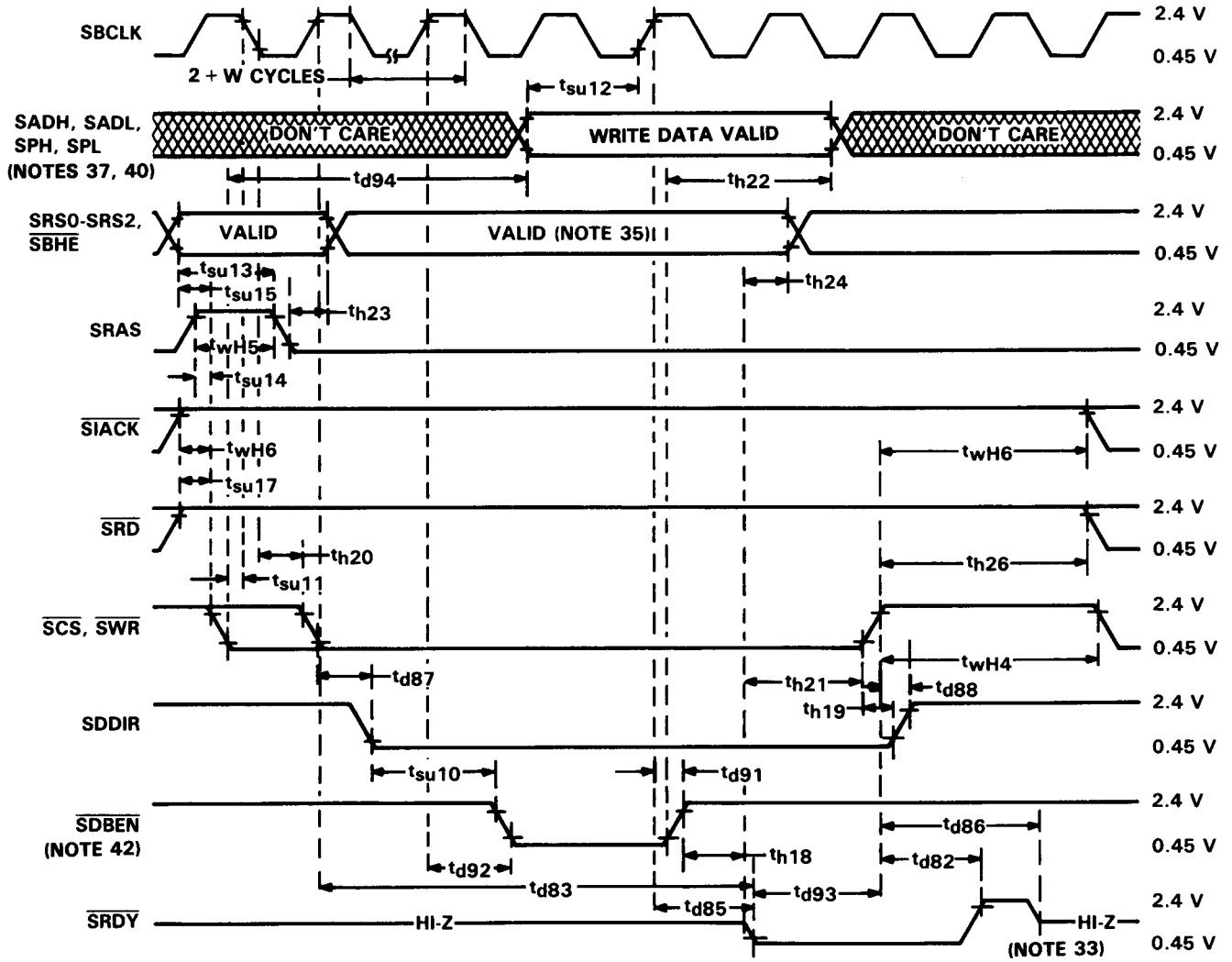
808X mode DIO write timing



NOTES: 33. Internal logic will drive $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$ high and verify that it has reached a valid high level before tristating the signal.
35. In 808X Mode, SRAS may be used to strobe the values of $\overline{\text{SBHE}}$, SRS0-SRS2 and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter t_{su14} and $\overline{\text{SBHE}}$, SRS0-SRS2, and $\overline{\text{SCS}}$ must meet parameter t_{su13}. If SRAS is strapped high, then parameters t_{su14} and t_{su13} are irrelevant.
37. Write data is sampled on the fifth rising edge of SBCLK following the recognition of a write data strobe on a falling edge of SBCLK.
40. In 8-bit mode DIO writes, the value placed on SADH is a don't care.
42. In a write cycle, $\overline{\text{SDBEN}}$ is asserted on the third rising edge of SBCLK following the sample of a write data strobe.

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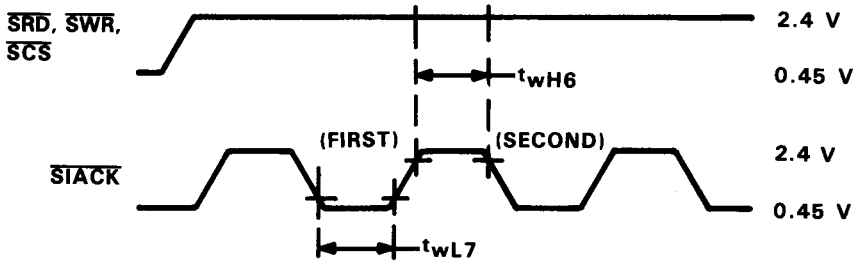
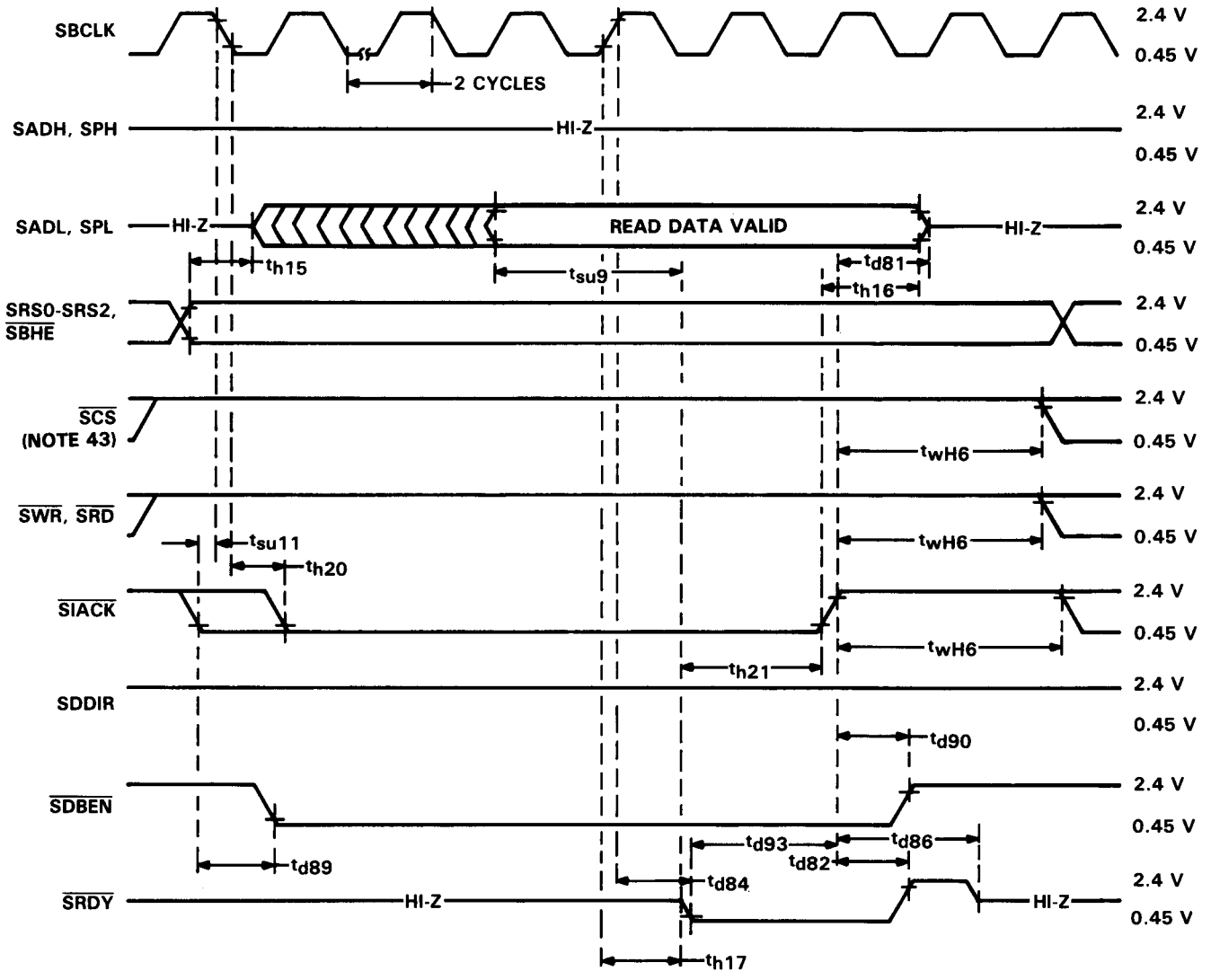
808X mode interrupt acknowledge timing—first $\overline{\text{SIACK}}$ pulse

808X reads interrupt vector from TMS38030.



808X mode interrupt acknowledge timing—second $\overline{\text{SIACK}}$ pulse

808X master reads interrupt vector from TMS38030.

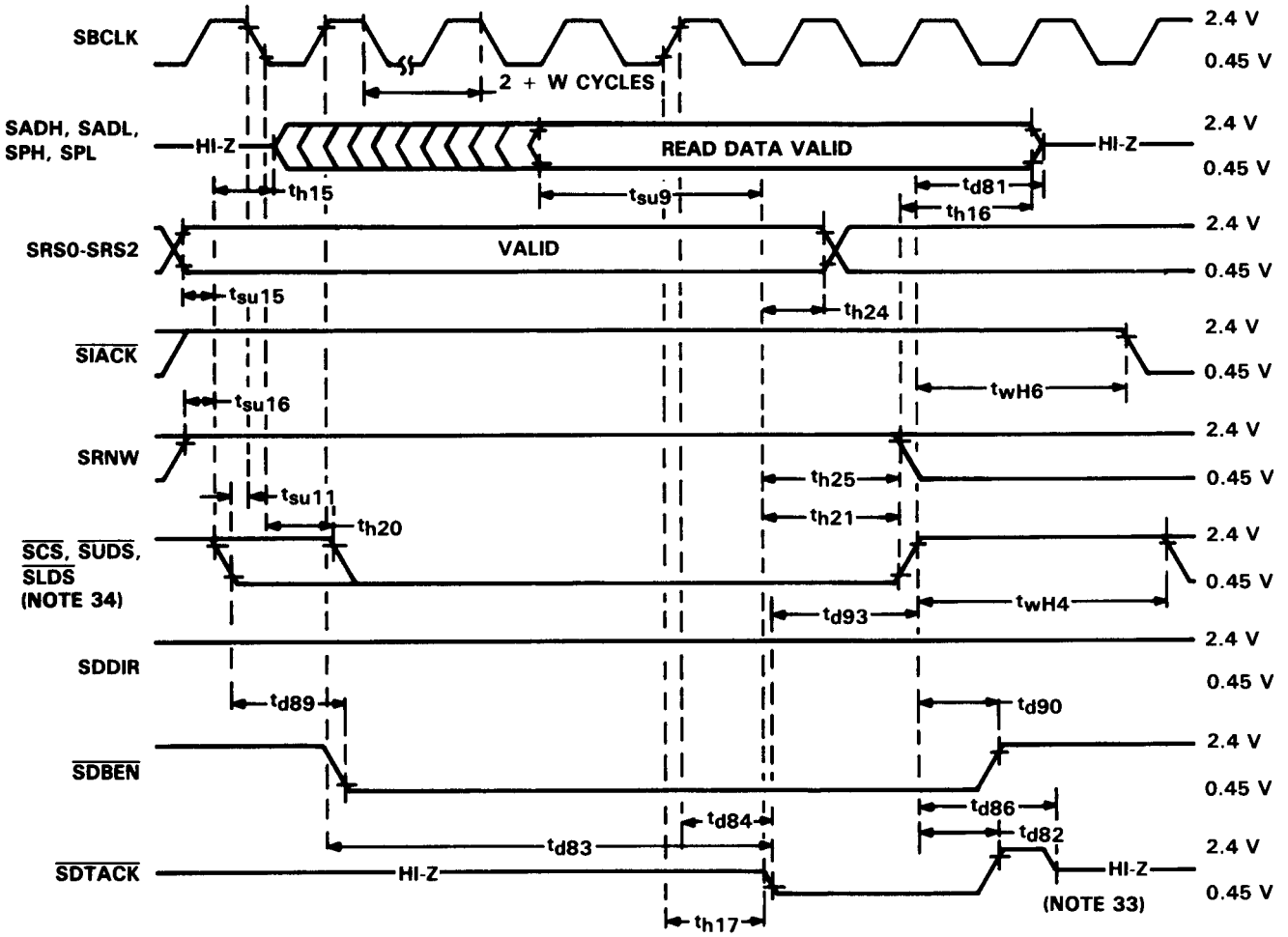


NOTE 43: The "inactive" chip select is SIACK in DIO read and DIO write cycles, and SCS in interrupt acknowledge cycles.

A

680XX mode DIO read timing

680XX master reads TMS38030 DIO register



NOTES: 33. Internal logic will drive $\overline{SRDY}/\overline{SDTACK}$ high and verify that it has reached a valid high level before tristating the signal.
34. For 680XX mode, skew between $\overline{SLDS}$ and $\overline{SUDS}$ must not exceed 10 ns. Providing that limitation is observed, all events referenced to a data strobe edge are to the later occurring edge. Events defined by two data strobe edges, parameter t_{wH4}, are measured between latest and earlier edges.

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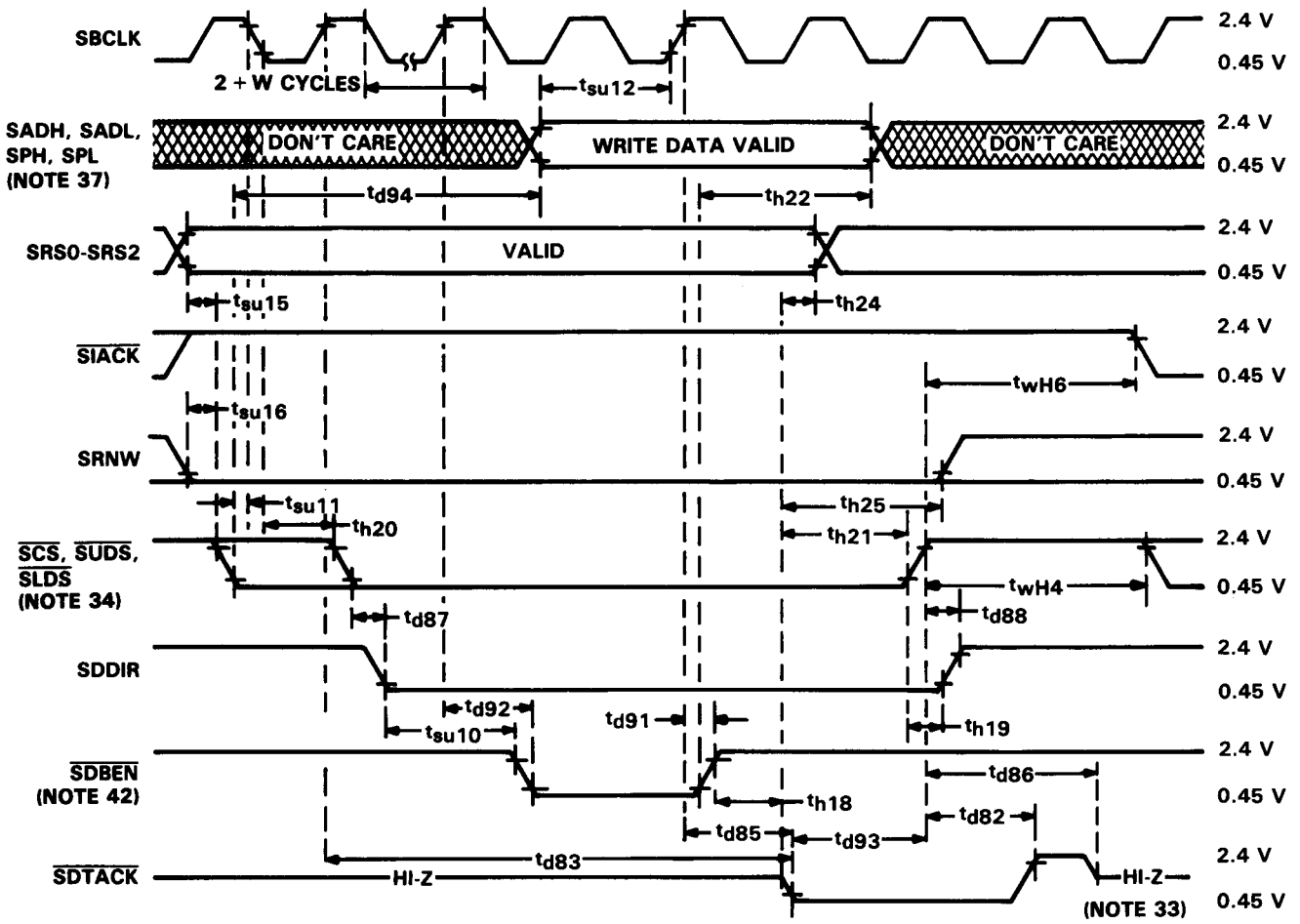
680XX mode DIO write timing

680XX master writes to TMS38030 DIO register



NOTES: 33. Internal logic will drive $\overline{\text{SRDY}}/\overline{\text{SDTACK}}$ high and verify that it has reached a valid high level before tristating the signal.
34. For 680XX mode, skew between $\overline{\text{SLDS}}$ and $\overline{\text{SUDS}}$ must not exceed 10 ns. Providing that limitation is observed, all events referenced to a data strobe edge are to the later occurring edge. Events defined by two data strobe edges, parameter t_{wH4}, are measured between latest and earlier edges.
37. Write data is sampled on the fifth rising edge of SBCLK following the recognition of a write data strobe on a falling edge of SBCLK.
42. In a write cycle, $\overline{\text{SDBEN}}$ is asserted on the third rising edge of SBCLK following the sample of a write data strobe.

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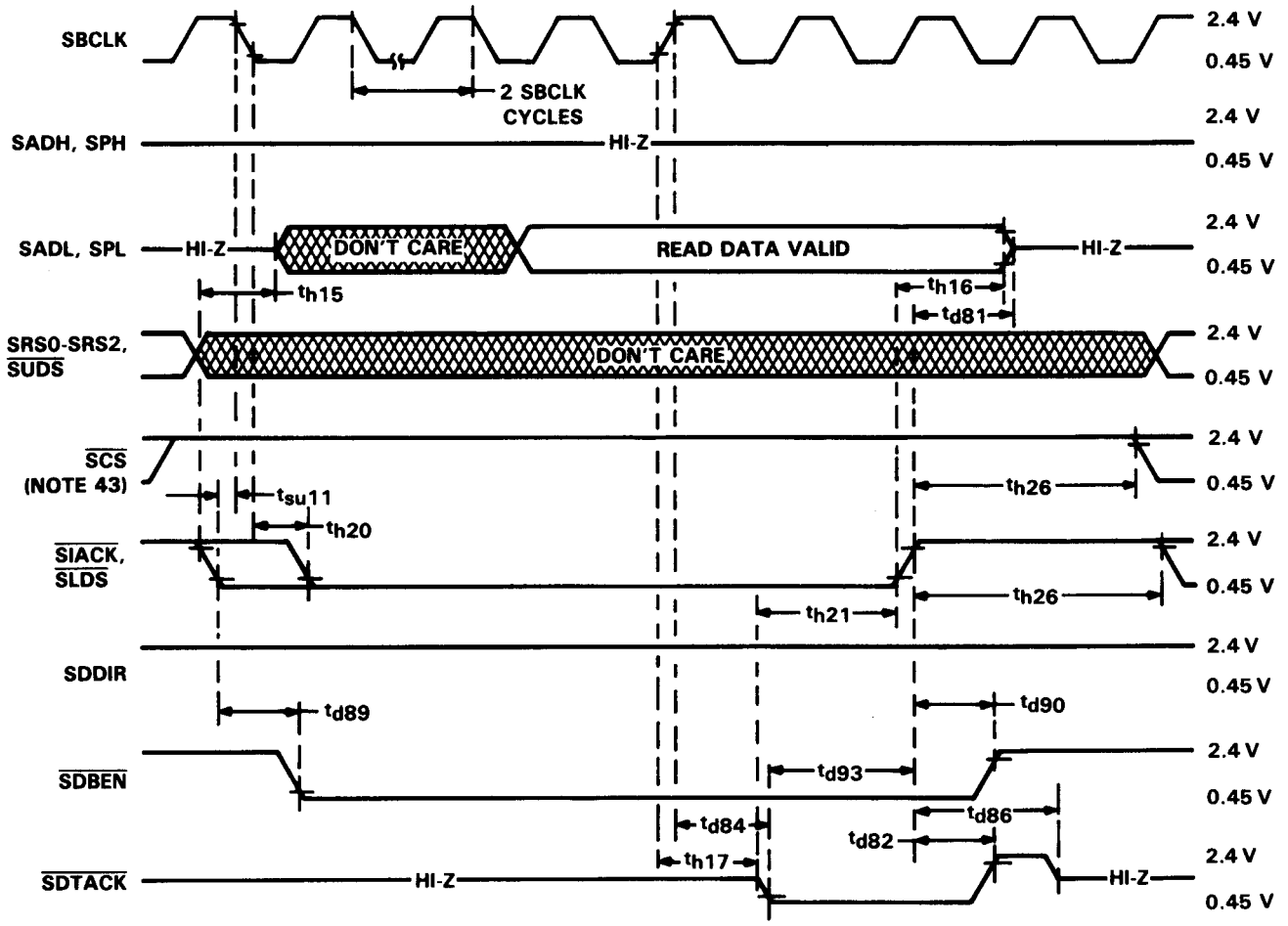
680XX mode interrupt acknowledge cycle timing

680XX master reads interrupt vector from TMS38030



NOTE 43: The "inactive" chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ in interrupt acknowledge cycles.

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