



MICROCIRCUIT DATA SHEET

MN100115-X REV 0A0

Original Creation Date: 10/24/95
 Last Update Date: 08/28/96
 Last Major Revision Date: 10/24/95

LOW-SKEW QUAD CLOCK DRIVER

General Description

The F100115 contains four low skew differential drivers designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing.

Industry Part Number

100115

NS Part Numbers

100115FM-MLS
 100115FMQB.

Prime Die

F115

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	0
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Differential Inputs and Outputs
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: -4.2V to -5.7V
- Military and industrial grades available

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature (Tstg)	-65 C to +150 C
Maximum Junction Temperature (Tj)	
Ceramic	+175 C
Plastic	+150 C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	Vcc to +0.5V
Output Current (DC Output HIGH)	-50mA
ESD (Note 2)	≥ 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Military	-55 C to +125 C
Industrial	-40 C to +85 C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -4.8V, Tc= -55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH(1)	Input HIGH Current	Vee= -4.8V, VM= -0.87V	1, 3	CLKIN, CLKIN		100	uA	1, 2
			1, 3	CLKIN, CLKIN		150	uA	3
IIH(2)	Input HIGH Current	Vee= -4.8V, VM= -0.87V	1, 3	TCLK		300	uA	1, 2
			1, 3	TCLK		450	uA	3
IIH(3)	Input HIGH Current	Vee= -4.8V, VM= -0.87V	1, 3	CLKSEL		260	uA	1, 2
			1, 3	CLKSEL		380	uA	3
IIL	Input Low Current	Vee= -4.2V, VM= -1.83V	1, 3	TCLK CLKSEL	0.5		uA	1, 2, 3
ICBO	Input Leakage Current	Vee= -4.2V, VM= -4.2V	1, 3	CLKIN CLKIN	-10		uA	1, 2, 3
VOH	Output HIGH Voltage	Vee=-4.2V/-4.8V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms To -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-4.8V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage	Vee=-4.2V/-4.8V, VIH=-1.165V, VIL=-1.475V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage	Vee=-4.2V/-4.8V, VIH=-1.165V, VIL=-1.475V, LOADING:50 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	TCLK, CLKSEL	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	TCLK CLKSEL	-1830	-1475	mV	1, 2, 3
VCM	Common Mode Voltage	VEE= -4.2/-4.8V	1, 3, 7	CLKIN CLKIN	-2000	-500	mV	1, 2, 3
VDIFF	Input Voltage Differential	VEE= -4.2/-4.8V	1, 3, 7	CLKIN CLKIN	150		mV	1, 2, 3
IEE	Power Supply Current	Vee= -4.2/-4.8V	1, 3	VEE	-80	-25	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: Vee Range: -4.2V to -4.8V, VCC=VCCA=GND, LOADING: 50 Ohms To -2.0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH/tPHL (1)	Propagation Delay	Vee= -4.2/-4.8V	2, 4	CLKIN to CLKn	0.63	0.88	ns	9
			2, 4	CLKIN to CLKn	0.72	1.02	ns	10
			2, 4	CLKIN to CLKn	0.58	0.88	ns	11
tPLH/tPHL (2)	Propagation Delay	Vee= -4.2/-4.8V	2, 4	TCLK to CLKn	0.30	1.50	ns	9
			2, 4	TCLK to CLKn	0.40	1.70	ns	10
			2, 4	TCLK to CLKn	0.30	1.60	ns	11
tPLH/tPHL (3)	Propagation Delay	Vee= -4.2/-4.8V	2, 4	CLKSEL to CLKn	0.40	1.70	ns	9
			2, 4	CLKSEL to CLKn	0.50	1.80	ns	10
			2, 4	CLKSEL to CLKn	0.40	1.80	ns	11
ts(G-G)	Skew GATE to GATE	Vee= -4.2/-4.8V	2, 4	Gate to Gate Skew		100	ps	9
			2, 4	Gate to Gate Skew		120	ps	10, 11
tTLH/tTHL	Transition Time	Vee= -4.2/-4.8V	6	CLKn	0.25	0.85	ns	9
			6	CLKn	0.20	0.85	ns	10
			6	CLKn	0.30	0.90	ns	11

- Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
- Note 2: Screen tested 100% on each device at +25 C temp only, subgroup A9.
- Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
- Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
- Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
- Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
- Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

Graphics and Diagrams

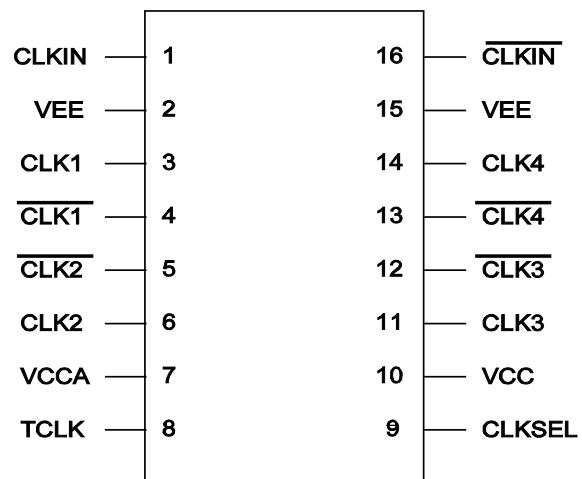
GRAPHICS#	DESCRIPTION
P000032A	CERPAC (W), 16 LEAD (PIN OUT)
W16ARL	CERPAC (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

CONNECTION DIAGRAM

100115

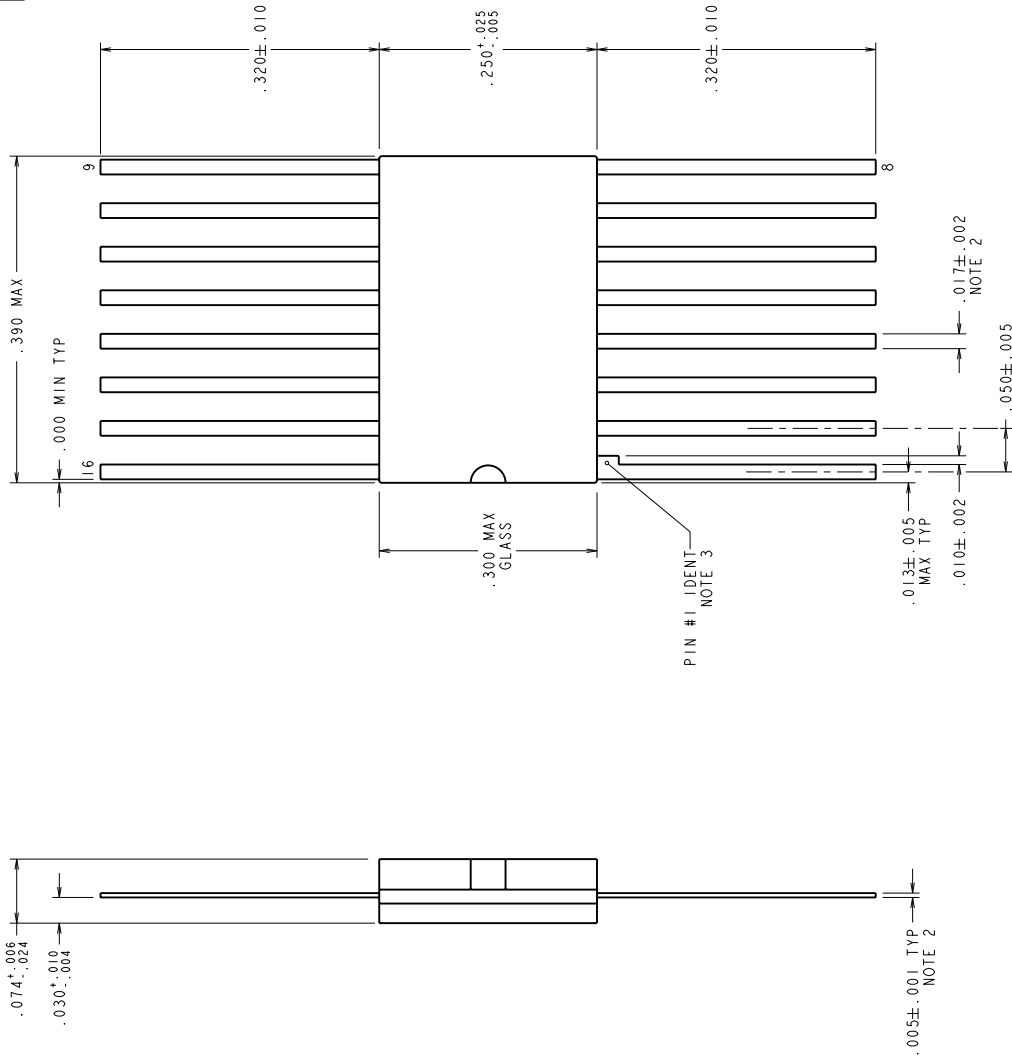
FLATPACK PINOUT



DWG# P000032A

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
 - a) A NOTCH OR OTHER MARK WITHIN THIS AREA
 - b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS	DATE
DRWN: <i>D.F. Grady</i>	07/28/94
DTG. CHK.	
EMR. CHK.	

PROJECTION	
	1/4" MIN

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING SHEET 1 of 1

National Semiconductor
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CERPACK, 16 LEAD