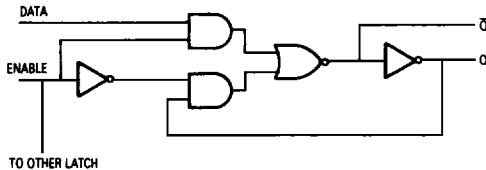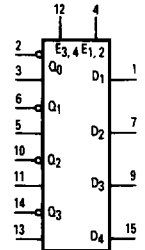# MOTOROLA

Military 54LS375

4-Bit Bistable Latch

ELECTRICALLY TESTED PER:
MIL-M-38510/31604

The 54LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.
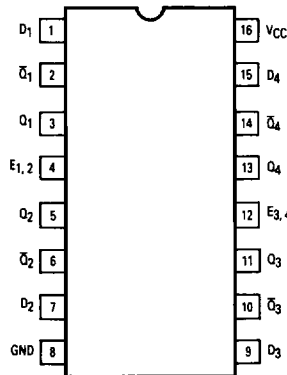
LOGIC DIAGRAM

LOGIC SYMBOL

CONNECTION DIAGRAM

AVAILABLE AS:

1) JAN: JM38510/31604BXA
2) SMD: *
3) 883C: 54LS375/BXAJC

X = CASE OUTLINE AS FOLLOWS:
    PACKAGE: CERDIP: E
           CERFLAT: F
           LCC: 2
*Call Factory for latest update

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
D_1	1	1	2	V_{CC}
Q_1	2	2	3	OPEN
$\overline{Q}_1$	3	3	4	V_{CC}
E_{n1-2}	4	4	5	V_{CC}
Q_2	5	5	7	V_{CC}
$\overline{Q}_2$	6	6	8	OPEN
D_2	7	7	9	V_{CC}
GND	8	8	10	GND
D_3	9	9	12	V_{CC}
Q_3	10	10	13	OPEN
$\overline{Q}_3$	11	11	14	V_{CC}
E_{n3-4}	12	12	15	V_{CC}
Q_4	13	13	17	V_{CC}
$\overline{Q}_4$	14	14	18	OPEN
D_4	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

Pin Names		Loading (Note a)	
		HIGH	LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_0–E_1	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_2–E_3	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1–Q_4	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_1$–$\overline{Q}_4$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

TRUTH TABLE (Each Latch)

t_n	t_{n+1}
D	Q
H	H
L	L

t_n = Bit time before enable negative-going transition
t_{n+1} = Bit time after enable negative-going transition

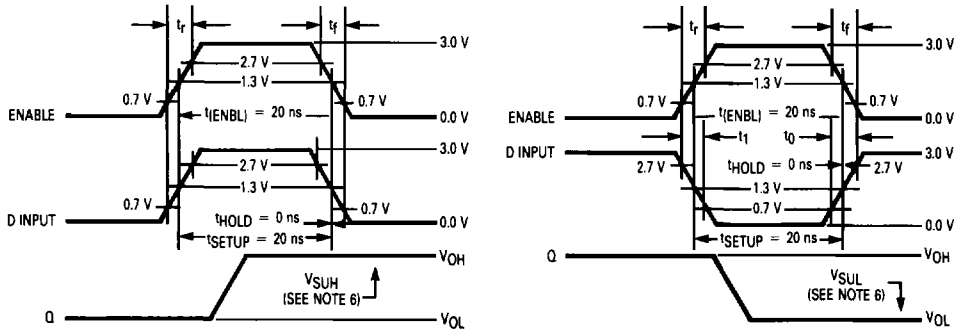**MOTOROLA MILITARY ALS/FAST/LS/TTL DATA**
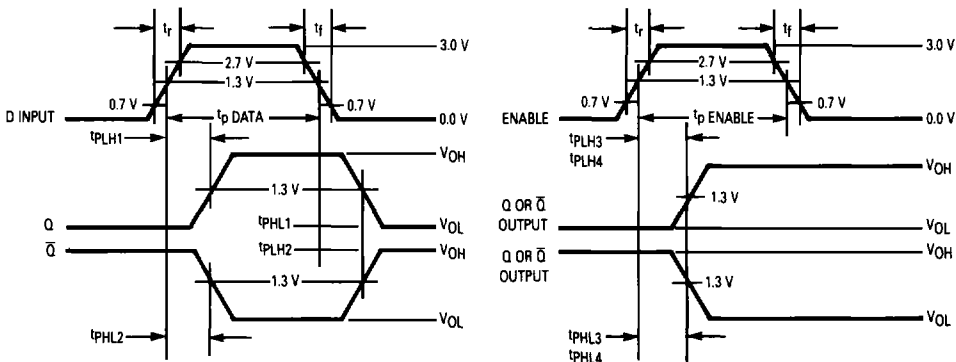
6-412

54LS375

AC TEST CIRCUIT

WAVEFORMS

Switching Test Circuit and Waveforms

Setup and Hold Waveforms

54LS375

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	$V_{CC} = 4.5$ V, $I_{OH} = -0.4$ mA, $V_{IH} = 2.0$ V or 0.7 V per truth table, Enable = (See Note 7).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	$V_{CC} = 4.5$ V, $I_{OL} = 4.0$ mA, $V_{IL} = 0.7$ V or 2.0 V per truth table, Enable = (See Note 7).
V_{IC}	Input Clamping Voltage		−1.5					V	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA, other inputs are open.
I_{IH}	Logical "1" Input Current (D inputs)		20		20		20	μA	$V_{CC} = 5.5$ V, $V_{IH} = 2.7$ V, other input is open.
I_{IHH}	Logical "1" Input Current (En inputs)		80		80		80	μA	$V_{CC} = 5.5$ V, $V_{IH} = $ GND, $V_{IN}(E_n) = 2.7$ V.
I_{IH}	Logical "1" Input Current (D inputs)		100		100		100	μA	$V_{CC} = 5.5$ V, $V_{IH} = 5.5$ V, $V_{IN}(E_n) = $ GND.
I_{IHH}	Logical "1" Input Current (En inputs)		400		400		400	μA	$V_{CC} = 5.5$ V, $V_{IH} = $ GND, $V_{IN}(E_n) = 5.5$ V.
I_{IL}	Logical "0" Input Current (D inputs)	−0.16	−0.4	−0.16	−0.4	−0.16	−0.4	mA	$V_{CC} = 5.5$ V, $V_{IL} = 0.4$ V, $V_{IN}(E_n) = 4.5$ V.
I_{IL}	Logical "0" Input Current (En inputs)	−0.64	−1.6	−0.64	−1.6	−0.64	−1.6	mA	$V_{CC} = 5.5$ V, $V_{IN}(E_n) = 0.4$ V, other input = 4.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	$V_{CC} = 5.5$ V, $V_{IN}(E_n) = 4.5$ V, other input = GND.
I_{CC}	Power Supply Current		12		12		12	mA	$V_{CC} = 5.5$ V, $V_{IN} = 0$ V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	$V_{CC} = 4.5$ V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	$V_{CC} = 4.5$ V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with $V_{CC} = 5.0$ V, $V_{INL} = 0.4$ V, and $V_{INH} = 2.5$ V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Switching Parameters	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay Data-Output Data to Q	3.0	22 17	3.0	29 24	3.0	29 24	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay Data-Output Data to Q	3.0	32 27	3.0	42 37	3.0	42 37	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PHL2} t_{PHL2}	Propagation Delay Data-Output Data to Q̄	3.0	20 15	3.0	26 21	3.0	26 21	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PLH2} t_{PLH2}	Propagation Delay Data-Output Data to Q̄	3.0	25 20	3.0	32 27	3.0	32 27	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PHL3} t_{PHL3}	Propagation Delay Data-Output Enable to Q	3.0	30 25	3.0	39 34	3.0	39 34	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PLH3} t_{PLH3}	Propagation Delay Data-Output Enable to Q	3.0	32 27	3.0	42 37	3.0	42 37	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PHL4} t_{PHL4}	Propagation Delay Data-Output Enable to Q̄	3.0	20 15	3.0	26 21	3.0	26 21	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
t_{PLH4} t_{PLH4}	Propagation Delay Data-Output Enable to Q̄	3.0	35 30	3.0	46 41	3.0	46 41	ns ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%. $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 2.0$ kΩ ± 5.0%.
V_{SUH}	Logical "1" Setup Voltage	2.5		2.5		2.5		V	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%.
V_{SUL}	Logical "0" Setup Voltage		0.4		0.4		0.4	V	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ ± 5.0%.

NOTES:
1. The D input pulse generator has the following characteristics: $V_{GEN} = 3.0$ V, $t_r \leqslant 15$ ns, $t_f \leqslant 6.0$ ns, $t_p = 30$ ns and $Z_{OUT} = 50$ Ω except when measuring V_{SETUP}.
2. The enable pulse generator is identical to the D input pulse generator.
3. $C_L = 50$ pF ± 10%, which includes probe and jig capacitance.
4. $R_L = 2.0$ kΩ ± 5.0%.
5. All diodes are 1N3064 or equivalent.
6. V_{SETUP} is to be measured 500 ns minimum after input transition to assure that the device has latched with minimum setup and maximum hold conditions applied to inputs.
7. Apply 0.0 V/3.0 V–5.0 V/0.0 V momentary pulse 500 ns minimum prior to measurement.
8. For all t_{PLH} and V_{SUH} tests, preset output into the ZERO state prior to making test.
9. For all t_{PHL} and V_{SUL} tests, preset output into ONE state prior to making test.
10. The limits specified for $C_L = 15$ pF are guaranteed but not tested.

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