MOTOROLA

Military 54F353

Dual 4-Input Data Selector/ Multiplexer With 3-State Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/33910

The 54F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

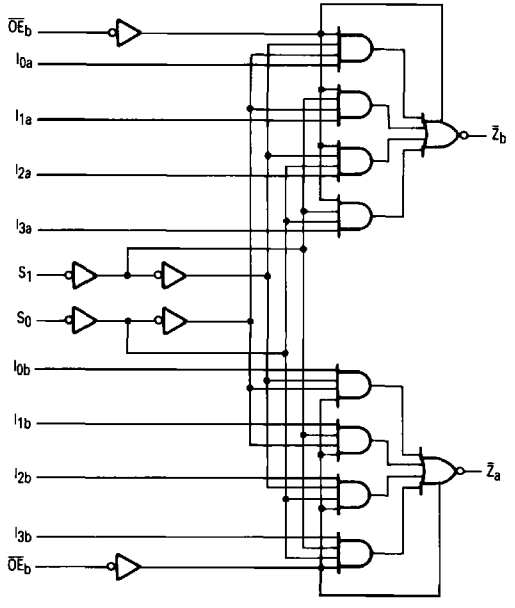
- Inverted Version of 'F253
- Multifunction Capability
- Separate Enables for Each Multiplexer

AVAILABLE AS:

1) JAN: JM38510/33910BXA
2) SMD: *
3) 883C: 54F353/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{OE}_a$	1	1	2	V_{CC}
S_1	2	2	3	V_{CC}
I_{3a}	3	3	4	V_{CC}
I_{2a}	4	4	5	V_{CC}
I_{1a}	5	5	7	V_{CC}
I_{0a}	6	6	8	V_{CC}
$\overline{Z}_a$	7	7	9	OPEN
GND	8	8	10	GND
$\overline{Z}_b$	9	9	12	OPEN
I_{0b}	10	10	13	V_{CC}
I_{1b}	11	11	14	V_{CC}
I_{2b}	12	12	15	V_{CC}
I_{3b}	13	13	17	V_{CC}
S_0	14	14	18	V_{CC}
$\overline{OE}_b$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

The 'F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are as shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

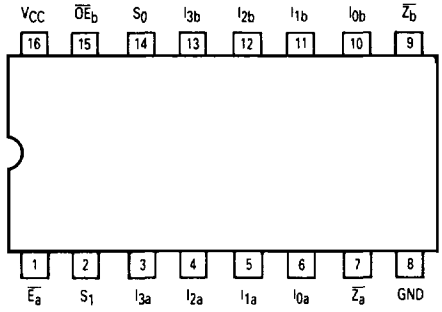
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = HIGH Impedance

CONNECTION DIAGRAM



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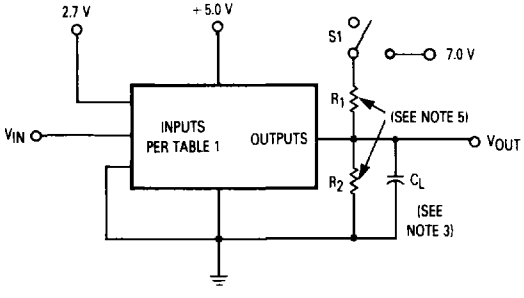
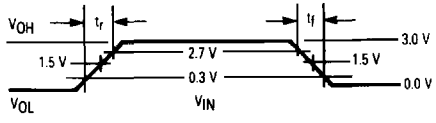
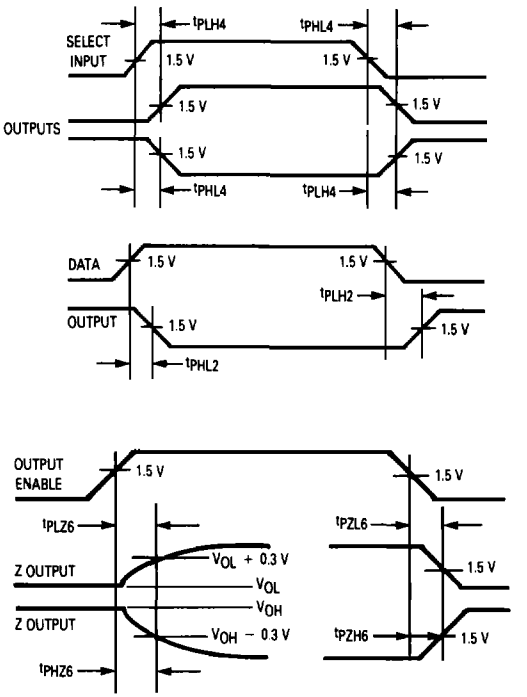
AC TEST CIRCUIT



Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed



WAVEFORMS



NOTES:
1. V_{IN} Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2 = 499\ \Omega \pm 5.0\%$.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IL} = 0.8 V, other inputs are open, $\overline{OE}_{a/b}$ = 0.8 V/open, $S_{1/0}$ = 0.8 V/2.0 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V, other inputs are open, $\overline{OE}_{a/b}$ = 0.8 V/ open, $S_{1/0}$ = 0.8 V/2.0 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{OE}_{a/b}$ = 4.5 V/ (2.7 V), $S_{1/0}$ = 4.5 V, 0 V, or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open, $\overline{OE}_{a/b}$ = 4.5 V/ (7.0 V), $S_{1/0}$ = 4.5 V, 0 V or (7.0 V).
I_{OD}	Diode Current	35		35		35		mA	V_{CC} = 4.5 V, V_{IN} = 5.5 V, other inputs are open, $\overline{OE}_{a/b}$ & $S_{1/0}$ = 0 V, V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, $\overline{OE}_{a/b}$ = 0 V/ (0.5 V), $S_{1/0}$ = 4.5 V, 0 V, or (0.5 V).
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs are open, V_{OUT} = 0 V, $\overline{OE}_{a/b}$ & $S_{1/0}$ = 0 V.
I_{IOZH}	Output Off Current High		50		50		50	μA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs are open, V_{OUT} = 2.4 V, $\overline{OE}_{a/b}$ = 2.0 V/open, $S_{1/0}$ = 0 V.
I_{IOZL}	Output Off Current Low		−50		−50		−50	μA	V_{CC} = 5.5 V, V_{IN} = 0.8 V, other inputs are open, V_{OUT} = 0.5 V, $\overline{OE}_{a/b}$ = 2.0 V/open, $S_{1/0}$ = 0 V.
I_{CCH}	Power Supply Current Off		14		14		14	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current Off		20		20		20	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V ($I_{0a/b}$ inputs), All other inputs = 0 V.
I_{CCZ}	Power Supply Current Off		23		23		23	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), $\overline{OE}_{a/b}$ = 4.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, **(Repeat at)**, V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2}	Propagation Delay /Data-Output I_n to $\overline{Z}_n$	1.5	6.0	1.5	7.5	1.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output I_n to $\overline{Z}_n$	1.5	7.0	1.5	9.0	1.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output S_n to $\overline{Z}_n$	4.0	11	4.0	14	4.0	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output S_n to $\overline{Z}_n$	4.0	14	4.0	16	4.0	16	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLZ6}	Output Disable Time, $\overline{OE}_n$ to $\overline{Z}_n$	2.0	6.0	2.0	8.5	2.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHZ6}	Output Disable Time, $\overline{OE}_n$ to $\overline{Z}_n$	2.0	6.0	2.0	6.5	2.0	6.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZL6}	Output Enable Time, $\overline{OE}_n$ to $\overline{Z}_n$	3.0	11	3.5	15.5	3.5	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZH6}	Output Enable Time, $\overline{OE}_n$ to $\overline{Z}_n$	3.0	8.0	3.0	11	3.0	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.

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