4086B

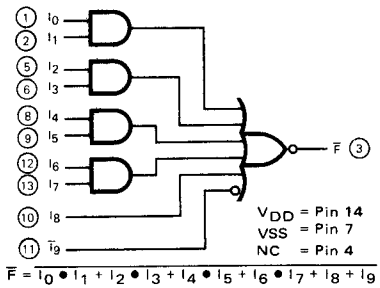
4-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION — The 4086B is a 4-Wide 2-Input AND-OR-Invert (AOI) Gate with two additional inputs (I_8 and $\overline{I}_9$) which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. A HIGH on I_8 or a LOW on $\overline{I}_9$ forces the Output ($\overline{F}$) LOW independent of the other eight inputs (I_0–I_7). The Output (F) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_0–I_8	Gate Inputs
$\overline{I}_9$	Gate Input (Active LOW)
$\overline{F}$	Output (Active LOW)

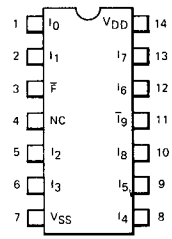
LOGIC DIAGRAM



$$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4 \bullet I_5 + I_6 \bullet I_7 + I_8 + I_9}$$

NOTE:
A HIGH on I_8 or a LOW on $\overline{I}_9$ forces the output ($\overline{F}$) LOW.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

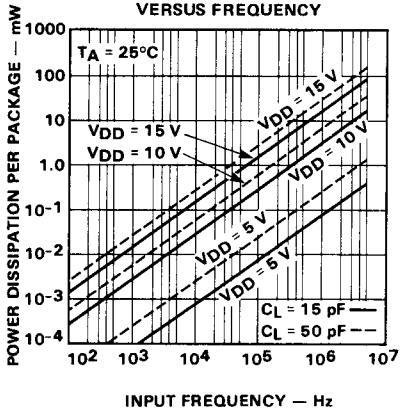
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		100	180		40	80		25	64	ns	
t_{PHL}	I_0 through I_8 to $\overline{F}$		100	180		40	80		25	64	ns	C_L = 50 pF,
t_{PLH}	Propagation Delay,		65	100		35	50		20	40	ns	R_L = 200 kΩ
t_{PHL}	$\overline{I}_9$ to $\overline{F}$		65	100		35	50		20	40	ns	Input Transition
t_{TLH}	Output Transition		55	100		25	50		18	35	ns	Times ⩽ 20 ns
t_{THL}	Time		55	100		25	50		18	35	ns	

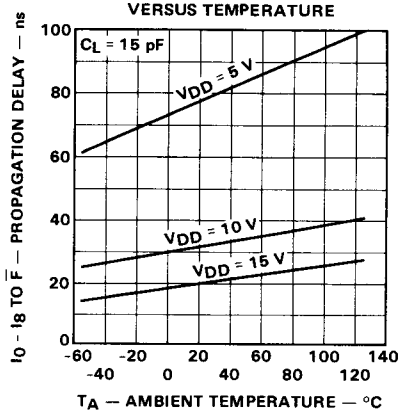
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

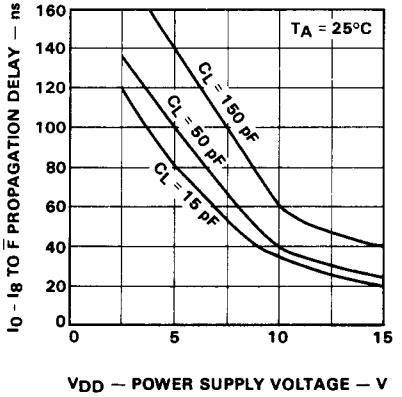
POWER DISSIPATION VERSUS FREQUENCY



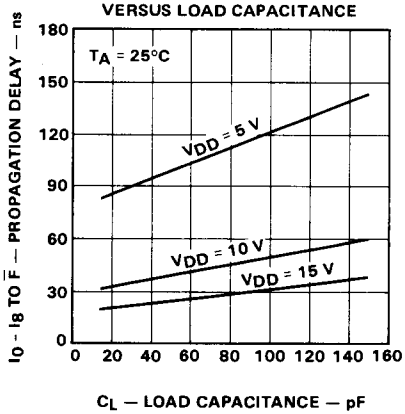
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



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