SOCS025B - FEBRUARY 1991

TTL-Compatible InputsCCD-Compatible Outputs	DW PACKAGE (TOP VIEW)			
 Variable-Output Slew Rates With External Resistor Control 	DLADJ [1 GND [2	20 V _{SS} 19 1PC2		
Frame-Transfer Operation		18] 1PC1		
 Solid-State Reliability 	SRG2,3IN 🛛 4	17 VCC		
Adjustable Clock Levels	SRG1IN [5	16 SRG3OUT		
	TRGIN 🛿 6	15 SRG2OUT		
description	2,3PC1 [7	14 SRG1OUT		
	2,3PC2 [8	13 TRGOUT		
The TMS3472A serial driver is a monolithic	SSR [9	12 V _{CC}		
CMOS integrated circuit designed to drive the serial-register gate (SRGn) and transfer-gate	Vss [10	11] TSR		
(TRG) inputs of the Texas Instruments (TI [™])				

TC241 (monochrome) CCD image sensor. The TMS3472A interfaces the TI TMS3471C or a user-defined timing generator to the TC241; it receives TTL signals from the timing generator and outputs level-shifted and slew-rate-adjusted signals to the image sensor. The TMS3472A contains three noninverting serial drivers and one noninverting transfer driver as well as circuitry for slew-rate adjustment.

The voltage levels on SRG1OUT, SRG2OUT, SRG3OUT, and TRGOUT are controlled by the levels on V_{SS} and V_{CC}. DLADJ, PD, SRG1IN, SRG2,3IN, and TRGIN are TTL compatible. A high level on PD allows the <u>TM</u>S3472 to operate normally with the level-shifted and slew-rate-adjusted outputs following the inputs. When PD is low, the device is in a low power-consumption mode and all outputs are at V_{CC} .

The slew rate of SRG1OUT, SRG2OUT, and SRG3OUT is controlled by connecting a resistor between V $_{
m CC}$ and SSR. The TRGOUT slew rate is controlled by connecting a resistor between V_{CC} and TSR. The larger the resistor values, the longer the rise and fall times are.

The TMS3472A is available in a 20-pin surface-mount package (DW) and is characterized for operation from −20°C to 45°C.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

TI is a trademark of Texas Instruments Incorporated

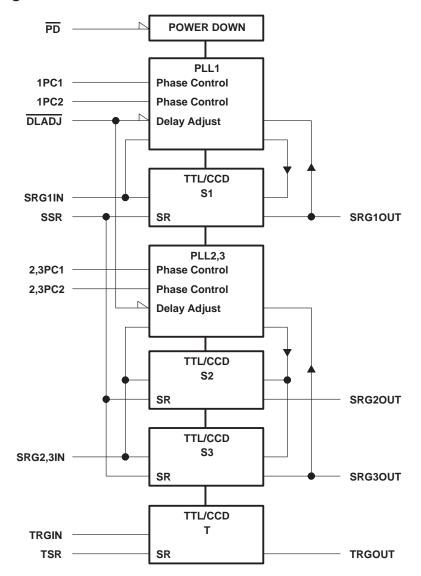
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1991, Texas Instruments Incorporated

SOCS025B - FEBRUARY 1991

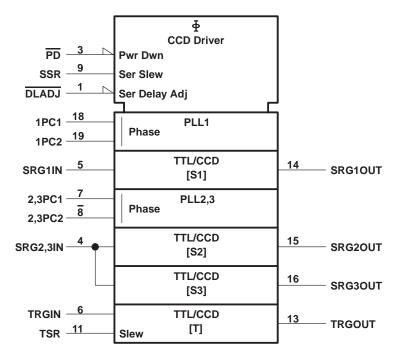
functional block diagram





SOCS025B - FEBRUARY 1991

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984.

Terminal Functions

TERMINAL		1/0	DESCRIPTION		
NAME	NO.	1/0	DESCRIPTION		
DLADJ	1	I	Delay adjust for all serial-register gates		
GND	2		Ground		
2,3PC1‡	7	I	Phase-adjust control for SRG2OUT, SRG3OUT		
2,3PC2‡	8	I	Phase-adjust control for SRG2001, SRG3001		
1PC1 [‡]	18	I	Dhage adjust control for SPC10LT		
1PC2 [‡]	19	I	Phase-adjust control for SRG1OUT		
PD	3	I	Power down		
SRG1IN	5	I	Serial-register gate 2 and 3 in		
SRG2,3IN	4	I	Serial-register gate 1 in		
SRG10UT	14	0	Serial-register gate 1 out		
SRG2OUT	15	0	Serial-register gate 2 out		
SRG3OUT	16	0	Serial-register gate 3 out		
SSR	9	I	Serial-register gate out slew-rate adjust		
TRGIN	6	I	Transfer gate in		
TRGOUT	13	0	Transfer gate out		
TSR	11	I	Transfer gate out slew-rate adjust		
VCC§	12	I	Positive supply veltage		
VCC§	17	Ι	Positive supply voltage		
VSS§	10	I			
VSS§	20	I	Negative supply voltage		

⁺A 270-pF capacitor should be connected between terminals 7 and 8 and between terminals 18 and 19.

 $\$ All terminals of the same name should be connected together externally.



SOCS025B - FEBRUARY 1991

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Positive supply voltage, V_{CC} (see Note 1) Negative supply voltage, V_{SS} (see Note 2)	
Continuous total power dissipation at (or below), $TA \leq 25$ C.	
Unmounted device (see Figure 1)	nW
Mounted device (see Figure 1)	nW
Operating free-air temperature range, T _A – 20°C to 45	
Storage temperature range, T _{STG}	5°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

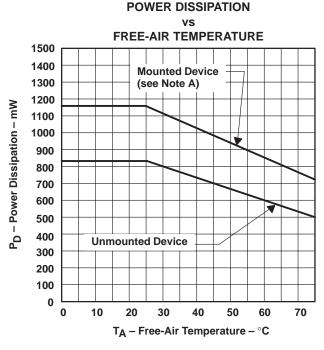


Figure 1

NOTE A: The mounted-device derating curve of Figure 1 is obtained under the following conditions: The board is 50 mm by 50 mm by 1.6 mm thick.

The board material is glass epoxy.

The copper thickness of all the etch runs is 35 microns.

Etch run dimensions – All 20 etch runs are 0.4 mm by 22 mm.

Each chip is soldered to the board.

An aluminum cooling fin 10 mm by 10 mm by 1 mm thick is coupled to the chip with thermal paste.



SOCS025B - FEBRUARY 1991

recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC}^{\dagger}		0	1	2.2	V
Negative supply voltage, V _{SS} (see Note 2) [†]		-11.1	-10.4	-9.7	V
	DLADJ, SRG1IN, SRG2,3IN, TRGIN	2	5		v
High-level input voltage, VIH	PD	2.5	5		
	DLADJ, SRG1IN, SRG2,3IN, TRGIN		0	0.8	V
Low-level input voltage, VIL	PD		0	0.9	v
Slope-bias resistance		10		50	kΩ
Operating free-air temperature, T _A		-20		45	°C

[†]V_{CC} and V_{SS} have 100-mA current limits. Adequate decoupling capacitors are required from these pins to ground.

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[‡]

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH	High-level output voltage	I _{OH (serial)} = 48 mA (peak), I _{OH (transfer)} = 67 mA (peak)	V _{CC} -0.5	VCC	V _{CC} +0.5	V
V _{OL}	Low-level output voltage	I _{OL (serial)} = 48 mA (peak), I _{OL (transfer)} = 32 mA (peak)	V _{SS} -0.6	V _{SS}	V _{SS} +0.8	V
Чн	High-level input current	$V_{IH} = 5 V$			50	μΑ
۱ _{IL}	Low-level input current	$V_{IL} = 0$			±10	μΑ
	Supply ourropt	No load, PD at 0 V			-0.85	mA
ISS	Supply current	Average load			-55	ШA

[‡] These parameters are measured with T_A = 25°C, V_{SS} = -10.3 V, V_{CC} = 2.1 V, slope-bias resistance on SSR and TSR = 22 kΩ, frequency of SRG10UT, SRG20UT, and SRG30UT = 4.8 MHz, and frequency of TRG0UT = 2.1 MHz. The load is a TC241 monochrome CCD image sensor.



SOCS025B - FEBRUARY 1991

switching characteristics for SRG1OUT, SRG2OUT, and SRG3OUT

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
	Jitter			2	ns
^t d1			15	30	ns
t _{d2}	See Figure 2			37	ns
t _{d3}		See Note 3	82		ns
tw(H)	Pulse duration, high	See Note 5	35		ns
tw(L)	Pulse duration, low		65		ns
	Slew rate	ude		400	V/µs
	Noise amplitude			300	mV

NOTE 3: These parameters are measured with T_A = 25°C, V_{SS} = -10.3 V, V_{CC} = 2.1 V, slope-bias resistance on SSR = 22 kΩ, and frequency of SRG1OUT, SRG2OUT, and SRG3OUT = 4.8 MHz. The load is a TC241 monochrome CCD image sensor.

switching characteristics for TRGOUT

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
tr	Rise time	See Note 4	135	185	ns
t _f	Fall time		50	100	ns

NOTE 4: These parameters are measured with $T_A = 25^{\circ}C$, $V_{SS} = -10.3$ V, $V_{CC} = 2.1$ V, slope-bias resistance on TSR = 22 k Ω , and frequency of TRGOUT = 2.1 MHz. The load is a TC241 monochrome CCD image sensor.



SOCS025B - FEBRUARY 1991

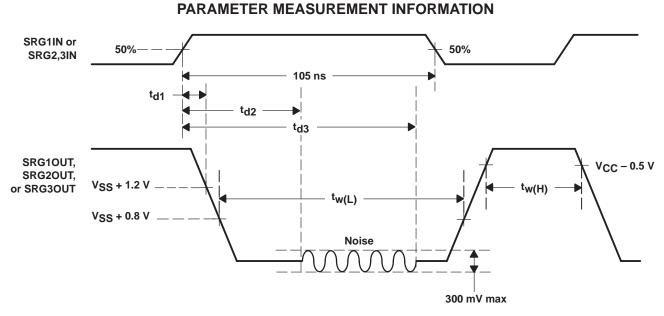


Figure 2. Serial-Register-Gate Timing Diagram



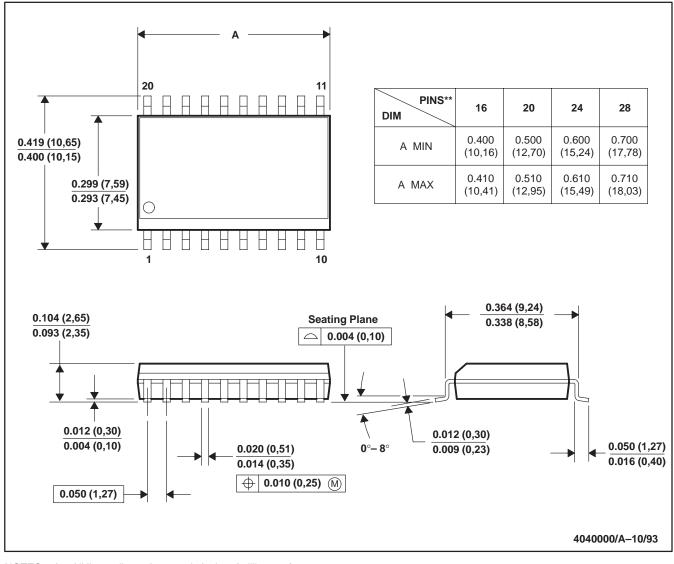
SOCS025B - FEBRUARY 1991

MECHANICAL DATA

DW/R-PDSO-G**

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated