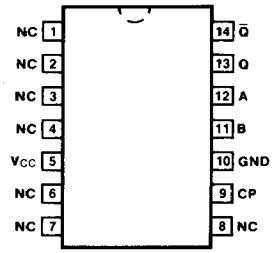
016760

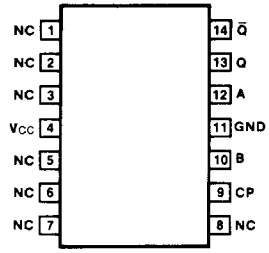
54/7491A

8-BIT SHIFT REGISTER

CONNECTION DIAGRAMS
PINOUT A

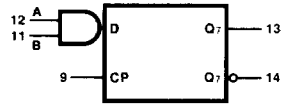


PINOUT B



DESCRIPTION — The '91 is a serial-in, serial-out, 8-bit shift register. It is composed of eight RS master/slave flip-flops, input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise immunity level of 1.0 V.

LOGIC SYMBOL
(Pinout A only)



VCC = Pin 5
GND = Pin 10

ORDERING CODE: See Section 9

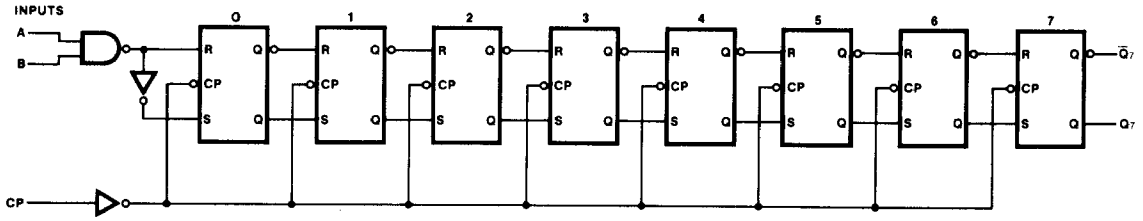
PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7491APC		9A
Ceramic DIP (D)	A	7491ADC	7491ADM	6A
Flatpak (F)	B	7491AFC	7491AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A, B	Serial Data Inputs	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
Q_7	Data Output	10/10
$\bar{Q}_7$	Complementary Data Output	10/10

FUNCTIONAL DESCRIPTION — Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and CP) appear as only one TTL input load. The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift register to be fully compatible with other edge-triggered synchronous functions.

LOGIC DIAGRAM

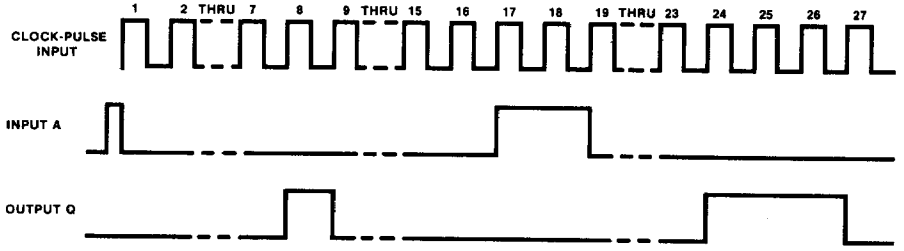


TRUTH TABLE

INPUTS		OUTPUT
t_n		t_{n+8}
A	B	Q_7
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
t_n = Bit time before clock pulse.
t_{n+8} = Bit time after eight clock pulses.
H = HIGH Voltage Level
L = LOW Voltage Level

TYPICAL INPUT/OUTPUT WAVEFORMS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		50	mA	V_{CC} = Max*
		XC		58		

*I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay		40	ns	Figs. 3-1, 3-8
t_{PHL}	CP to Q_7 or $\overline{Q}_7$		40		

AC OPERATING REQUIREMENTS: V_{CC} +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D to CP	25		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D to CP	0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D to CP	25		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D to CP	0		ns	Fig. 3-6
t_w (H)	CP Pulse Width HIGH	25		ns	Fig. 3-8