

# MM54HCT251/MM74HCT251 8-Channel TRI-STATE® Multiplexer

## General Description

This 8-channel digital multiplexer with TRI-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

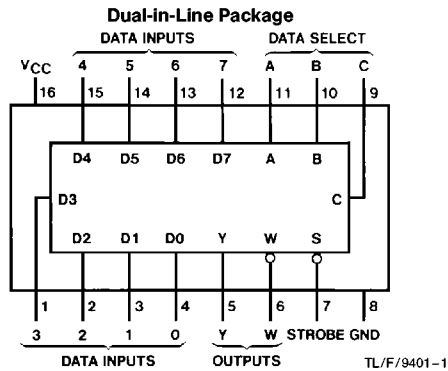
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

## Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40  $\mu$ A maximum (74HCT Series)
- Low input current: 1  $\mu$ A maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

## Connection and Logic Diagrams



Top View

Order Number MM54HCT251 or MM74HCT251

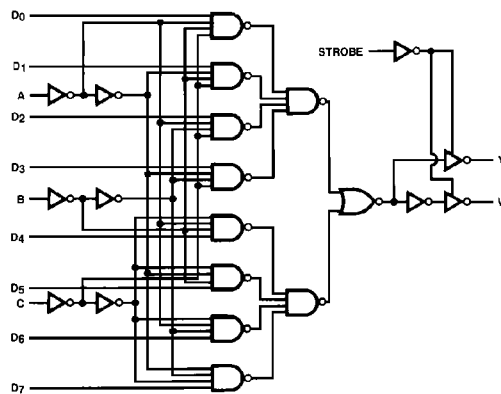
## Truth Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level

X = irrelevant, Z = high impedance (off)

D0, D1 . . . D7 = the level of the respective D input



TL/F/9401-2

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## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5V to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per Pin ( $I_{OUT}$ )	$\pm 35$ mA
DC $V_{CC}$ or GND Current, per Pin ( $I_{CC}$ )	$\pm 70$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering, 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ ) $V_{CC} = 4.5V$		500	ns

## DC Electrical Characteristics (Note 4) $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
				$T_A = -40^\circ C$ to $+85^\circ C$		$T_A = -55^\circ C$ to $+125^\circ C$	
$V_{IH}$	Minimum High Level Input Voltage			2.0	2.0	2.0	V
$V_{IL}$	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	4.5	4.4	4.4	4.4	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA, $V_{CC} = 4.5V$	4.2	3.98	3.84	3.7	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.8$ mA, $V_{CC} = 5.5V$	5.2	4.98	4.84	4.7	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA, $V_{CC} = 4.5V$	0.2	0.26	0.33	0.4	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.8$ mA, $V_{CC} = 5.5V$	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{OZ}$	Maximum TRI-STATE Output Leakage	$V_{OUT} = V_{CC}$ or GND $STROBE = V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8.0	80	160	$\mu A$
		$V_{IN} = 2.4V$ or $0.5V$	0.25	0.4	0.55	0.65	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**AC Electrical Characteristics**  $V_{CC}=5V$ ,  $T_A=25^{\circ}C$ ,  $C_L=15\text{ pF}$ ,  $t_r=t_f=6\text{ ns}$

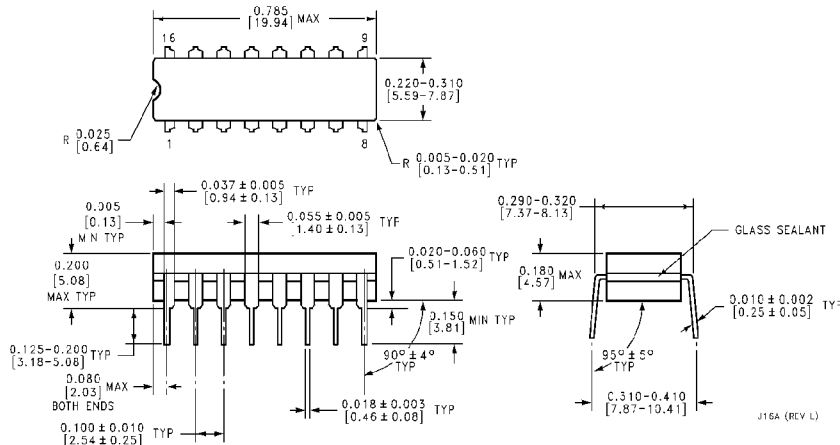
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay A, B or C to Y		26	35	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, A, B or C to W		27	35	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Any D to Y		22	31	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Any D to W		24	32	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time, W Output	$R_L=1\text{ k}\Omega$ $C_L=50\text{ pF}$	19	27	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time, Y Output	$R_L=1\text{ k}\Omega$ $C_L=50\text{ pF}$	19	26	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time W Output	$R_L=1\text{ k}\Omega$ $C_L=5\text{ pF}$	26	40	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time Y Output	$R_L=1\text{ k}\Omega$ $C_L=5\text{ pF}$	27	40	ns

**AC Electrical Characteristics**  $V_{CC}=5.0V \pm 10\%$ ,  $C_L=50\text{ pF}$ ,  $t_r=t_f=6\text{ ns}$  (unless otherwise specified)

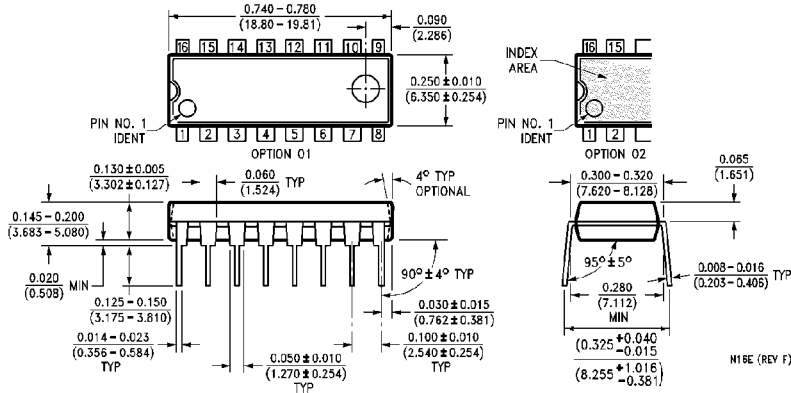
Symbol	Parameter	Conditions	$T_A=25^{\circ}C$		74HC	54HC	Units
			Typ	Guaranteed Limits		$T_A=-40^{\circ}C\text{ to }+85^{\circ}C$	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay A, B or C to Y		33	46	58	69	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, A, B or C to W		33	46	58	69	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, any D to Y		27	40	50	60	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, any D to W		27	40	50	60	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time W Output	$R_L=1\text{ k}\Omega$	21	30	38	45	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time Y Output	$R_L=1\text{ k}\Omega$	21	30	38	45	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time W Output	$R_L=1\text{ k}\Omega$	22	40	50	60	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time Y Output	$R_L=1\text{ k}\Omega$	23	40	50	60	ns
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time		8	15	19	23	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per Package)	110				pF
$C_{IN}$	Maximum Input Capacitance		5	10			pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D=C_{PD}V_{CC}^2f+l_{CC}V_{CC}$ , and the no load dynamic current consumption,  $I_S=C_{PD}V_{CC}f+l_{CC}$ .

**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54HCT521J or MM74HCT521J**  
**NS Package Number J16A**



**Molded Dual-In-Line Package (N)**  
**Order Number MM74HCT251N**  
**NS Package Number N16E**

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**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: onjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
 Tel: 81-043-299-2309  
 Fax: 81-043-299-2408

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