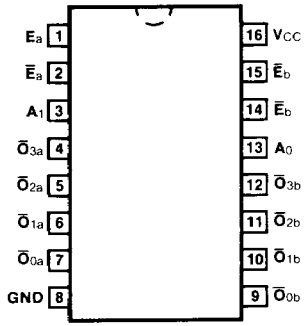
54/74155 010111
54LS/74LS155 010594

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION — The '155 contains two decoders with common Address (A_0, A_1) inputs and separate enable gates. Decoder "a" has an enable gate with one active HIGH and one active LOW input, while decoder "b" has two active LOW inputs. If the enable functions are satisfied, one output of each decoder will be LOW, as selected by the Address inputs.

CONNECTION DIAGRAM
PINOUT A



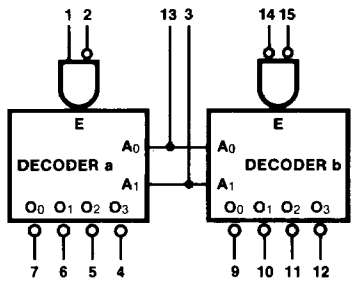
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74155PC, 74LS155PC		9B
Ceramic DIP (D)	A	74155DC, 74LS155DC	54155DM, 54LS155DM	6B
Flatpak (F)	A	74155FC, 74LS155FC	54155FM, 54LS155FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	1.0/1.0	0.5/0.25
$\bar{E}_a$, $\bar{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
E_a	Enable Input (Active HIGH)	1.0/1.0	0.5/0.25
$\bar{O}_0 - \bar{O}_3$	Outputs (Active LOW)	20/10	10/5.0 (2.5)

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '155 and '156 are dual 1-of-4 decoder/demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0 - \overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for decoder "a" requires one active HIGH input and one active LOW input (E_a, $\overline{E}_a$). In demultiplexing applications, decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for decoder "b" requires two active LOW inputs ($\overline{E}_b$, $\overline{E}_b$). The devices can be used as a 1-of-8 decoder/demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection as A_2. The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

The '155 and '156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in *Figure a*. The '156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \bullet (E + \overline{A}_0 + A_1) \bullet (E + A_0 + \overline{A}_1) \bullet (E + \overline{A}_0 + \overline{A}_1)$$
$$\text{where} = E = E_a + \overline{E}_a;\ E = E_b + E_b$$

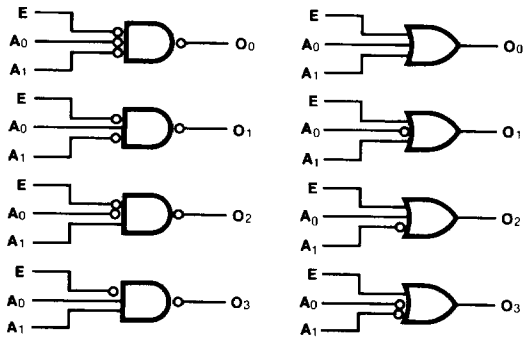
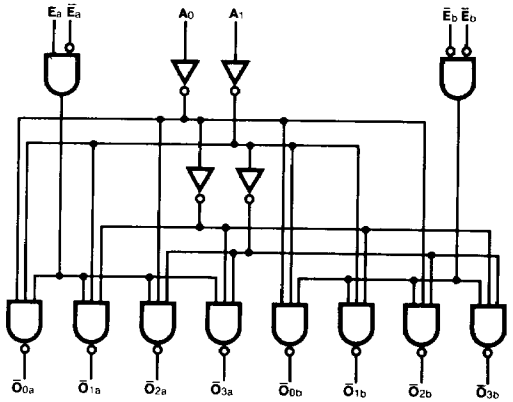


Fig. a

LOGIC DIAGRAM



TRUTH TABLE

ADDRESS		ENABLE a		OUTPUT a				ENABLE b		OUTPUT b			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-20	-100	ns	V_{CC} = Max
		XC	-18	-57	-20	-100		
I_{CC}	Power Supply Current	XM		35		10	mA	V_{CC} = Max; $\overline{E}_a$, $\overline{E}_b$ = Gnd
		XC		40		10		A_0, A_1, E_a = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		32 32		18 27	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$ or $\overline{E}_b$ to $\overline{O}_n$		20 27		15 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_a to $\overline{O}_n$		24 30		25 25	ns	Figs. 3-1, 3-4