

54/7470

JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '70 is a gated input edge-triggered JK flip-flop offering Direct Clear and Set inputs, and complementary Q and \bar{Q} outputs. Information at the J and K inputs is transferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specified voltage level of the clock pulse. When the clock input threshold voltage has been passed, the gate inputs are locked out. These flip-flops are designed for medium to high speed applications and offer a significant saving in system power dissipation and package count where input gating is required.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	\bar{Q}_n

Asynchronous Inputs:

LOW input to \bar{S}_D sets Q to HIGH level
 LOW input to \bar{C}_D sets Q to LOW level
 Clear or Set function can only occur when clock input is LOW
 Simultaneous LOW on \bar{C}_D and \bar{S}_D is indeterminate

$J = J_1 \cdot J_2 \cdot J_3$
 $K = K_1 \cdot K_2 \cdot K_3$
 t_n = Bit time before clock pulse.
 t_{n+1} = Bit time after clock pulse.
 If inputs \bar{J}_3 or \bar{K}_3 are not used they must be grounded.
 H = HIGH Voltage Level
 L = LOW Voltage Level

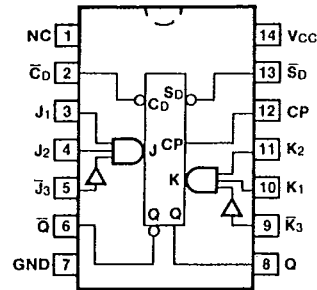
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP (P)	A	7470PC		9A
Ceramic DIP (D)	A	7470DC	5470DM	6A
Flatpak (F)	B	7470FC	5470FM	3I

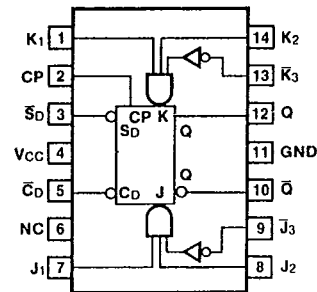
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
J_1, J_2, \bar{J}_3 } K_1, K_2, \bar{K}_3 }	Data Inputs	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
\bar{C}_D	Direct Clear Input (Active LOW)	2.0/2.0
\bar{S}_D	Direct Set Input (Active LOW)	2.0/2.0
Q, \bar{Q}	Outputs	20/10

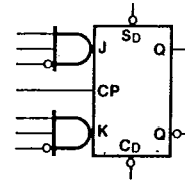
CONNECTION DIAGRAMS
PINOUT A



PINOUT B

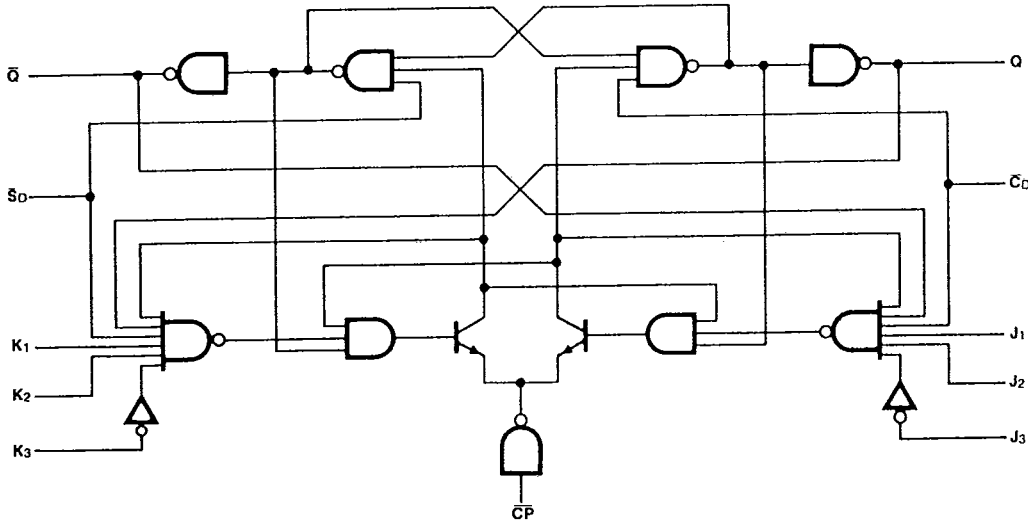


LOGIC SYMBOL



$V_{CC} = \text{Pin } 14 (4)$
 $GND = \text{Pin } 7 (11)$

LOGIC DIAGRAM



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I _{CC}	Power Supply Current		26	mA	V _{CC} = Max, V _{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	DESCRIPTION	54/74		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω			
		Min	Max		
f _{max}	Maximum Clock Frequency	20		MHz	Fig. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP to Q or Q̄		50	ns	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay S _D or C _D to Q or Q̄		50	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t _s (H)	Setup Time HIGH, J _n or K _n to CP	20		ns	Fig. 3-6
t _h (H)	Hold Time HIGH, J _n or K _n to CP	5.0		ns	Fig. 3-6
t _s (L)	Setup Time LOW, J _n or K _n to CP	20		ns	Fig. 3-6
t _h (L)	Hold Time LOW, J _n or K _n to CP	5.0		ns	Fig. 3-6
t _w (H) t _w (L)	CP Pulse Width	20 30		ns	Fig. 3-8
t _w (L)	S _D or C _D Pulse Width LOW	25		ns	Fig. 3-10