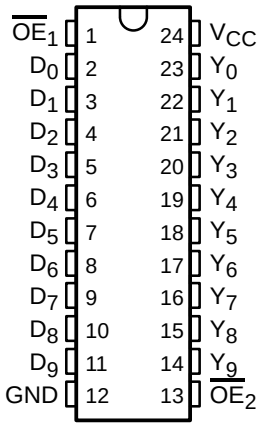
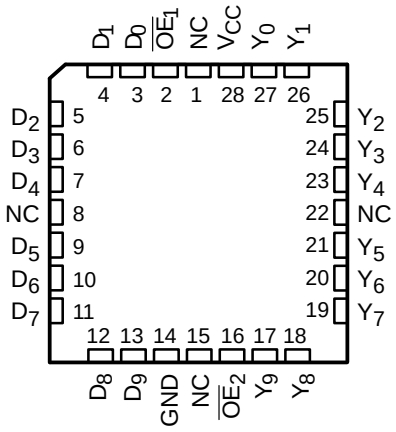
- **Function, Pinout, and Drive Compatible With FCT, F, and AM29827 Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **3-State Outputs**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **CY54FCT827T**
  - **32-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT827T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**

CY74FCT827T . . . Q OR SO PACKAGE
(TOP VIEW)



CY74FCT827T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’FCT827T devices are 10-bit bus drivers that provide high-performance bus-interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NANDed output enables for maximum control flexibility. The ’FCT827T devices are designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	4.4	CY74FCT827CTQCT	FCT827C
	SOIC – SO	Tube	4.4	CY74FCT827CTSOC	FCT827C
		Tape and reel	4.4	CY74FCT827CTSOCT	
	QSOP – Q	Tape and reel	8	CY74FCT827ATQCT	FCT827A
	SOIC – SO	Tube	8	CY74FCT827ATSOC	FCT827A
		Tape and reel	8	CY74FCT827ATSOCT	
–55°C to 125°C	LCC – L	Tube	9	CY54FCT827ATLMB	

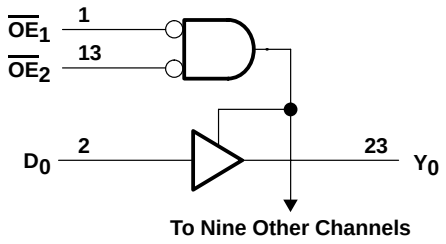
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D	Y	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-state
X	H	X	Z	

H = High logic level, L = Low logic level, X = Don't care,
Z = High-impedance state

logic diagram (positive logic)



Pin numbers shown are for the Q and SO packages.

absolute maximum rating over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package . . . . . 61°C/W
SO package . . . . . 46°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		CY54FCT827T			CY74FCT827T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			CY54FCT827T			CY74FCT827T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = –18 mA			–0.7	–1.2				V
	V_{CC} = 4.75 V,	I_{IN} = –18 mA						–0.7	–1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –12 mA		2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = –32 mA					2			
		I_{OH} = –15 mA					2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA			0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.3	0.55	
V_{hys}	All inputs				0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}				5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}							5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V				±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V							±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V				±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V							±1	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V				10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V							10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V				–10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V							–10	
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V		–60	–120	–225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V					–60	–120	–225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1			±1	µA
I_{CC}	V_{CC} = 5.5 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open							0.5	2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT827T			CY74FCT827T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CCD}¶	V_{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2$ = GND, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V				0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2$ = GND, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V							0.06	0.12	
I_C#	V_{CC} = 5.5 V, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1	2.4				
		10 bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		1.6	3.2‖				
			V_{IN} = 3.4 V or GND		4.1	13.2‖				
	V_{CC} = 5.25 V, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1	2.4	
		10 bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					1.6	3.2‖	
			V_{IN} = 3.4 V or GND					4.1	13.2‖	
C_i					5	10		5	10	pF
C_o					9	12		9	12	pF

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

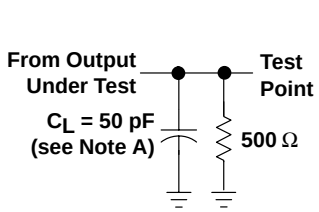
All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

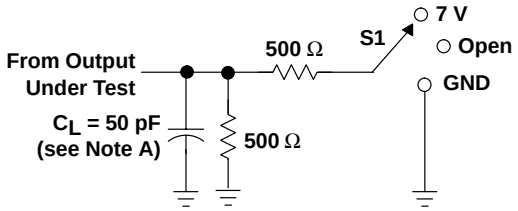
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT827AT		CY74FCT827AT		CY74FCT827CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	C_L = 50 pF, R_L = 500 Ω	1.5	9	1.5	8	1.5	4.4	ns
t_{PHL}				1.5	9	1.5	8	1.5	4.4	
t_{PLH}	D	Y	C_L = 300 pF, R_L = 500 Ω	1.5	17	1.5	15	1.5	10	ns
t_{PHL}				1.5	17	1.5	15	1.5	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω	1.5	13	1.5	12	1.5	7	ns
t_{PZL}				1.5	13	1.5	12	1.5	7	
t_{PZH}	$\overline{OE}$	Y	C_L = 300 pF, R_L = 500 Ω	1.5	25	1.5	23	1.5	14	ns
t_{PZL}				1.5	25	1.5	23	1.5	14	
t_{PHZ}	$\overline{OE}$	Y	C_L = 5 pF, R_L = 500 Ω	1.5	9	1.5	9	1.5	5.7	ns
t_{PHL}				1.5	9	1.5	9	1.5	5.7	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω	1.5	10	1.5	10	1.5	6	ns
t_{PHL}				1.5	10	1.5	10	1.5	6	

PARAMETER MEASUREMENT INFORMATION

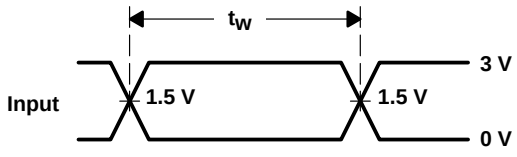


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

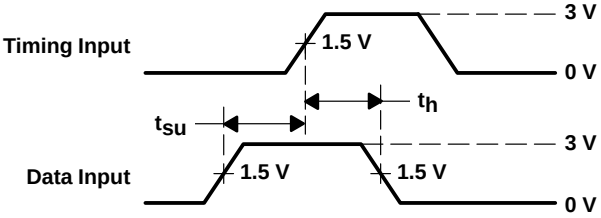


LOAD CIRCUIT FOR
3-STATE OUTPUTS

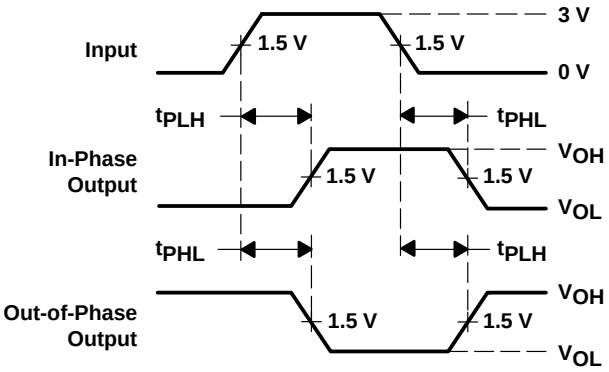
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



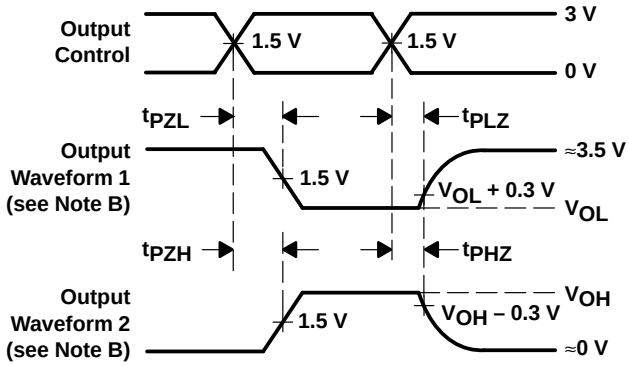
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

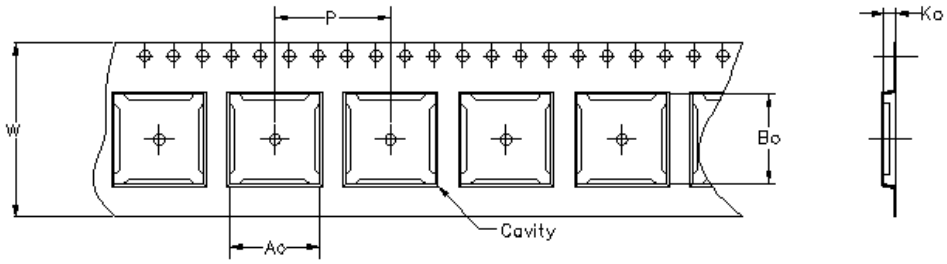
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9224701M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
CY74FCT827ATQCT	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT827ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT827ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT827ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827ATSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827ATSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827ATSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827ATSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827ATSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827CTQCT	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT827CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT827CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT827CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827CTSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827CTSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT827CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

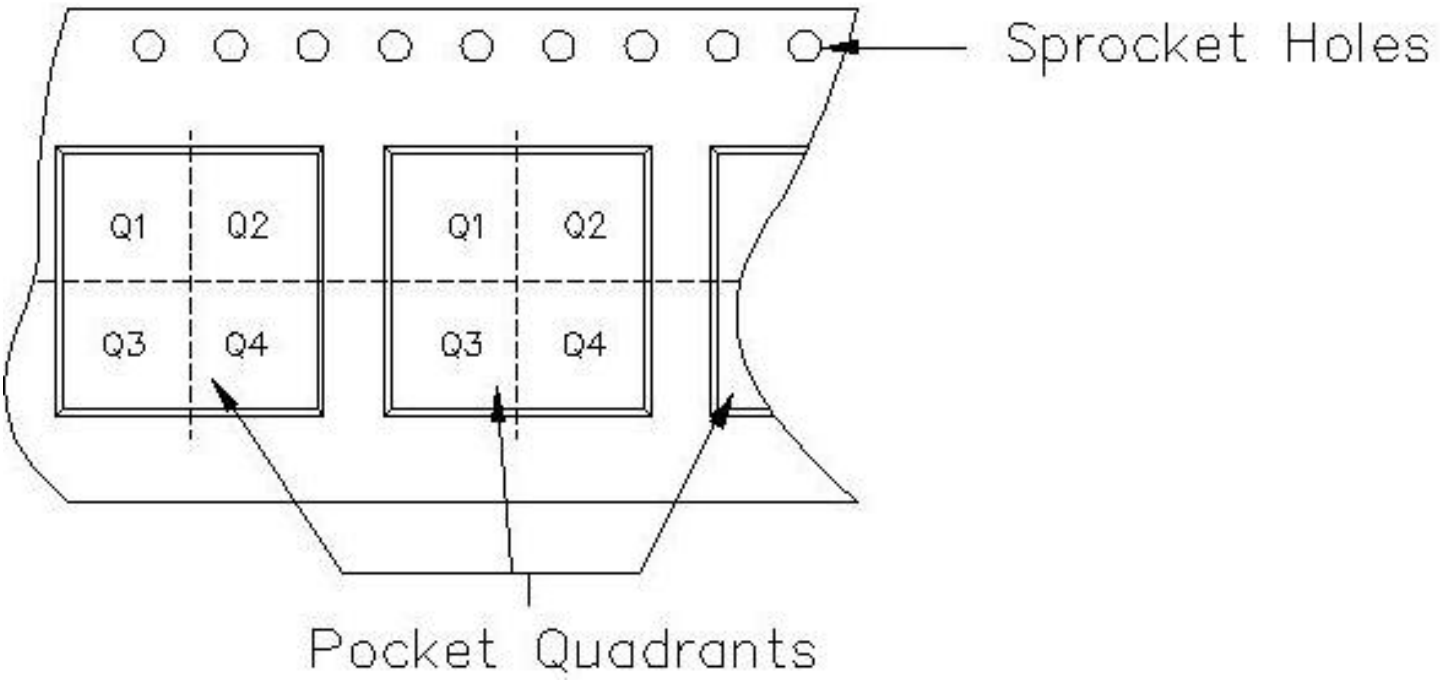
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



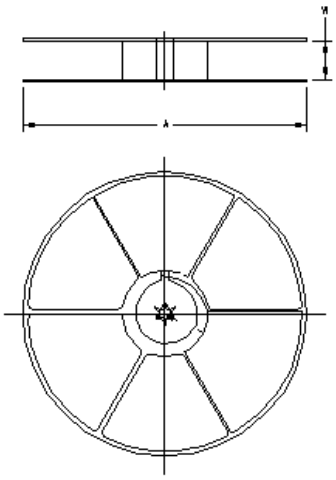
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



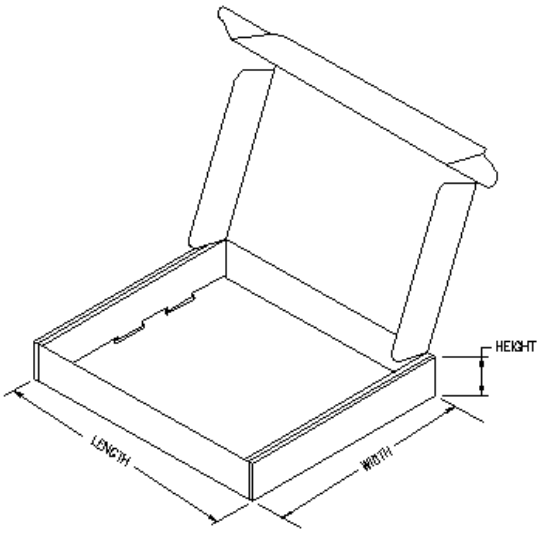
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT827ATQCT	DBQ	24	MLA	330	16	6.5	9.0	2.1	8	16	Q1
CY74FCT827ATSOCT	DW	24	TAI	330	24	10.75	15.7	2.7	12	24	Q1
CY74FCT827CTQCT	DBQ	24	MLA	330	16	6.5	9.0	2.1	8	16	Q1
CY74FCT827CTSOCT	DW	24	TAI	330	24	10.75	15.7	2.7	12	24	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CY74FCT827ATQCT	DBQ	24	MLA	0.0	0.0	0.0
CY74FCT827ATSOCT	DW	24	TAI	346.0	346.0	41.0
CY74FCT827CTQCT	DBQ	24	MLA	0.0	0.0	0.0
CY74FCT827CTSOCT	DW	24	TAI	346.0	346.0	41.0


HEIGHT
LENGTH
WIDTH

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