

SN54ALS843, SN54AS843, SN54ALS844, SN54AS844 SN74ALS843, SN74AS843, SN74ALS844, SN74AS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 — REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High Impedance
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

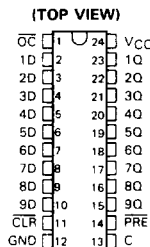
The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control (\overline{OC}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

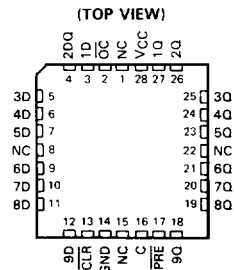
The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS843 and SN74ALS844 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS843 and SN54ALS844.

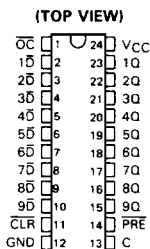
SN54ALS843, SN54AS843 . . . JT PACKAGE
SN74ALS843, SN74AS843 . . . DW OR NT PACKAGE



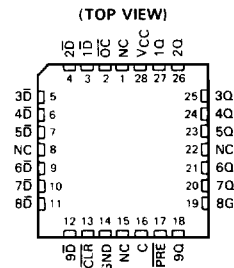
SN54ALS843, SN54AS843 . . . FK PACKAGE
SN74ALS843, SN74AS843 . . . FN PACKAGE



SN54ALS844, SN54AS844 . . . JT PACKAGE
SN74ALS844, SN74AS844 . . . DW OR NT PACKAGE



SN54ALS844, SN54AS844 . . . FK PACKAGE
SN74ALS844, SN74AS844 . . . FN PACKAGE



NC — No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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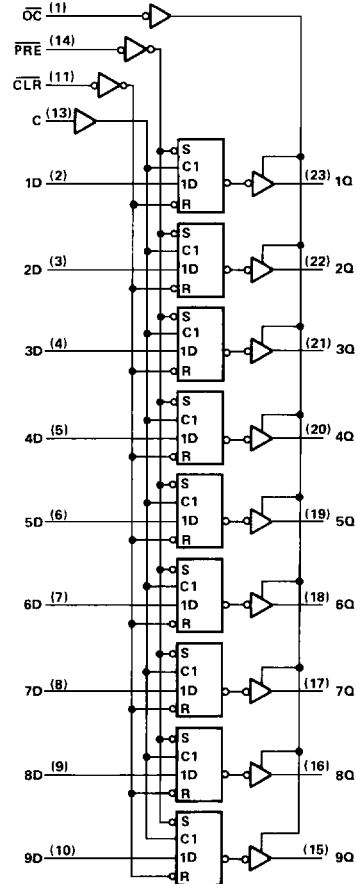
SN54ALS843, SN54AS843, SN54ALS844, SN54AS844
SN74ALS843, SN74AS843, SN74ALS844, SN74AS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0 °C to 70 °C.

'ALS843, 'AS843 FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OC	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q _O
X	X	H	X	X	Z

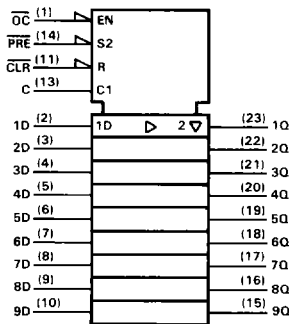
'ALS843, 'AS843 logic diagram (positive logic)



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'ALS843, 'AS843 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

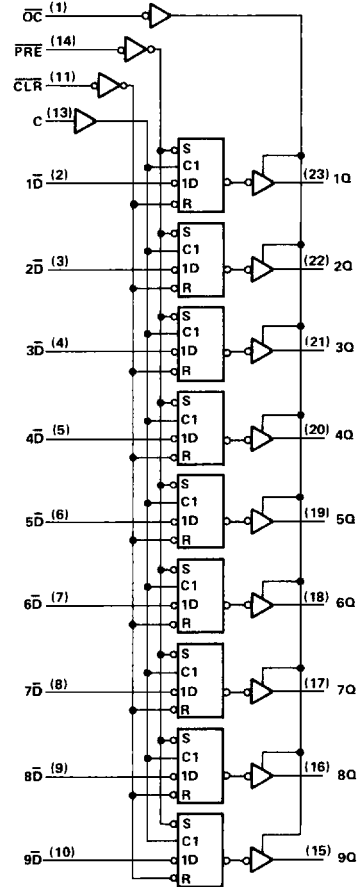
Pin numbers shown are for DW, JT, and NT packages.

**SN54ALS843, SN54AS843, SN54ALS844, SN54AS844
SN74ALS843, SN74AS843, SN74ALS844, SN74AS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

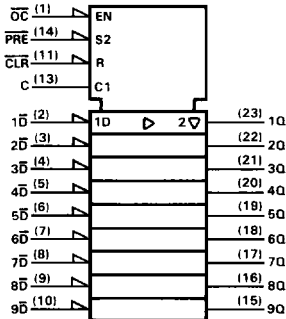
'ALS844, 'AS844 FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OC	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q _O
X	X	H	X	X	Z

'ALS844, 'AS844 logic diagram (positive logic)



'ALS844, 'AS844 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS', SN54AS'	-55 °C to 125 °C
SN74ALS', SN74AS'	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

SN54ALS843, SN54ALS844
SN74ALS843, SN74ALS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.7			0.8			V
I _{OH}	High-level output current	-1			-2.6			mA
I _{OL}	Low-level output current	12			24			mA
					48†			
t _w	Pulse duration	CLR or PRE low		40	35		ns	
		C high		25	20			
t _{SU}	Setup time, data before enable C↓	16			10			ns
t _H	Hold time, data after enable C↓	7			5			ns
T _A	Operating free-air temperature	-55	125		0	70	°C	

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V _{CC} - 2			V
		V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4			3.3			
		V _{CC} = 4.5 V, I _{OH} = -2.6 mA					2.4			
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25			0.4			V
		V _{CC} = 4.5 V, I _{OL} = 24 mA					0.35			
		V _{CC} = 4.75 V, I _{OL} = 48 mA (1 versions)					0.35			
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		20			20			μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V		-20			-20			μA
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V		-0.1			-0.1			mA
I _O §		V _{CC} = 5.5 V, V _O = 2.25 V		-30			-112			mA
I _{CC}	'ALS843	V _{CC} = 5.5 V	Outputs high	21	36	21	36	mA		
			Outputs low	41	67	41	67			
	Outputs disabled		25	42	25	42				
	'ALS844		Outputs high	21	36	21	36			
			Outputs low	41	72	41	72			
	Outputs disabled		28	48	28	48				

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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SN74ALS843, SN74ALS844

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX			UNIT	
			ALS843			SN54ALS843		SN74ALS843		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q		7	11	2	15	2	13	ns
t _{PHL}				11	15	4	20	4	18	
t _{PLH}	C	Q		12	18	5	25	5	21	ns
t _{PHL}				16	23	8	30	8	26	
t _{PLH}	PRE	Q		13	19	5	25	5	22	ns
t _{PHL}				19	26	4	35	6	30	
t _{PLH}	CLR	Q		19	26	4	35	6	30	ns
t _{PHL}				14	21	6	27	6	23	
t _{PZH}	OC	Q		7	10	2	14	2	12	ns
t _{PZL}				9	12	4	16	4	14	
t _{PHZ}	OC	Q		6	9	2	12	2	10	ns
t _{PLZ}				7	10	2	14	2	12	

ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX			UNIT	
			ALS844			SN54ALS844		SN74ALS844		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q		11	16	4	22	4	20	ns
t _{PHL}				9	13	3	17	3	15	
t _{PLH}	C	Q		17	24	8	32	8	29	ns
t _{PHL}				14	19	6	26	6	22	
t _{PLH}	PRE	Q		13	19	5	25	5	22	ns
t _{PHL}				19	26	4	35	6	30	
t _{PLH}	CLR	Q		19	26	4	35	6	30	ns
t _{PHL}				16	23	8	29	8	25	
t _{PZH}	OC	Q		10	15	2	19	4	17	ns
t _{PZL}				12	18	3	22	5	20	
t _{PHZ}	OC	Q		7	10	1	12	1	11	ns
t _{PLZ}				5	9	1	14	1	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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SN54AS843, SN54AS844
SN74AS843, SN74AS844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54AS843			SN74AS843			UNIT	
		SN54AS844			SN74AS844				
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage [§]	4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage		0.8			0.8		V	
I _{OH}	High-level output current			-24			-24	mA	
I _{OL}	Low-level output current			32			48	mA	
t _w	Pulse duration, enable C high	CLR or PRE low		5	4			ns	
		C high		5	4				
t _{su}	Setup time, data before enable C↓			3.5	2.5			ns	
t _h	Hold time, data after enable C↓			3.5	2.5			ns	
t _r	Recovery time	PRE		17	15			ns	
		CLR		16	14				
T _A	Operating free-air temperature			-55	125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS843			SN74AS843			UNIT
				SN54AS844			SN74AS844			
		MIN	TYP†	MAX	MIN	TYP†	MAX			
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -2 mA		V _{CC} -2		V _{CC} -2			V	
		V _{CC} = 4.5 V, I _{OH} = -15 mA		2.4	3.2	2.4	3.2			
		V _{CC} = 4.5 V, I _{OH} = -24 mA		2		2				
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 32 mA		0.25	0.5				V	
		V _{CC} = 4.5 V, I _{OL} = 48 mA				0.35	0.5			
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V			50		50		μA	
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V			-50		-50		μA	
I _I		V _{CC} = 5.5 V, V _I = 7 V			0.1		0.1		mA	
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V			20		20		mA	
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V			-0.5		-0.5		mA	
I _O [‡]		V _{CC} = 5.5 V, V _O = 2.25 V		-30	-112	-30	-112		mA	
I _{CC}	'AS843	V _{CC} = 5.5 V,	Outputs high	37	62	37	62	mA		
			Outputs low	56	92	56	92			
			Outputs disabled	56	92	56	92			
	'AS844		Outputs high	39	64	39	64			
			Outputs low	58	95	58	95			
			Outputs disabled	58	95	58	95			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS843		SN74AS843		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	O	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{\text{PRE}}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{\text{CLR}}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{\text{OC}}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{\text{OC}}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS844		SN74AS844		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	O	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{\text{PRE}}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{\text{CLR}}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{\text{OC}}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{\text{OC}}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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