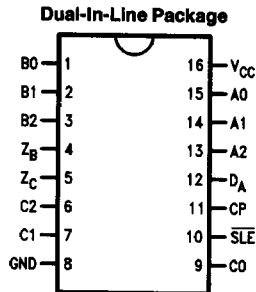


9338/DM9338 8-Bit Multiple Port Register

General Description

The DM9338 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously.

Connection Diagrams



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Order Number 9338DMQB, 9338FMQB or DM9338N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0-A2	Write Address Inputs
D _A	Data Input
B0-B2	B Read Address Inputs
C0-C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
SLE	Slave Enable Input (Active LOW)
Z _B	B Output
Z _C	C Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			-0.8			-0.8	mA
I _{OL}	Low Level Output Current			16			16	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C
t _s (H)	Setup Time HIGH or LOW	20			20			ns
t _s (L)	D _A to CP	12			12			ns
t _h (H)	Hold Time HIGH or LOW	0			0			ns
t _h (L)	D _A to CP	-8.0			-8.0			ns
t _s (H)	Setup Time HIGH or LOW	10			10			ns
t _s (L)	A _n to CP	10			10			ns
t _h (H)	Hold Time HIGH or LOW	0			0			ns
t _h (L)	A _n to CP	0			0			ns
t _w (H)	CP Pulse Width HIGH or LOW	23			23			ns
t _w (L)		13			13			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.4V			27	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-1.1	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	MIL -10 COM -10		-70 -70	mA
I _{CC}	Supply Current	V _{CC} = Max			135	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25^{\circ}C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15\text{ pF}$				Units
		9338 (MIL)		DM9338 (COM)		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay B_n or C_n to Z_n	40	35	13	40	ns
t_{PLH} t_{PHL}	Propagation Delay D_A to Z_n	45	50	25	45	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Z_n	35	30	18	30	ns

Functional Description

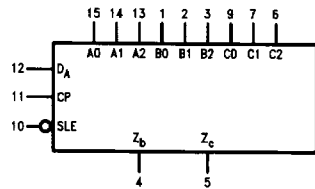
The 9338 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW (\overline{SLE}), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the

data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The method of parallel expansion is shown in *Figure a*. One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

Logic Symbol



$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

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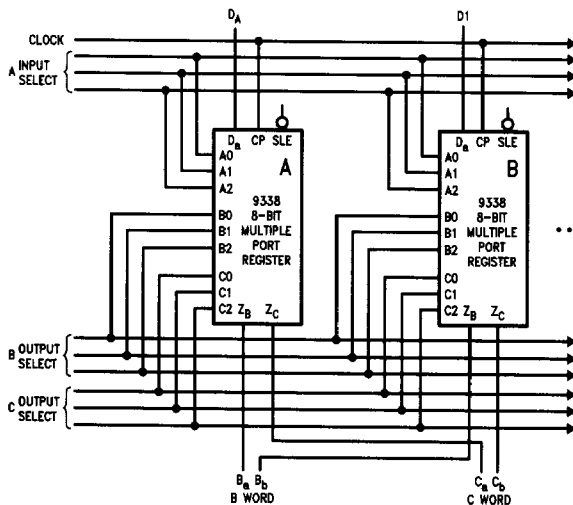
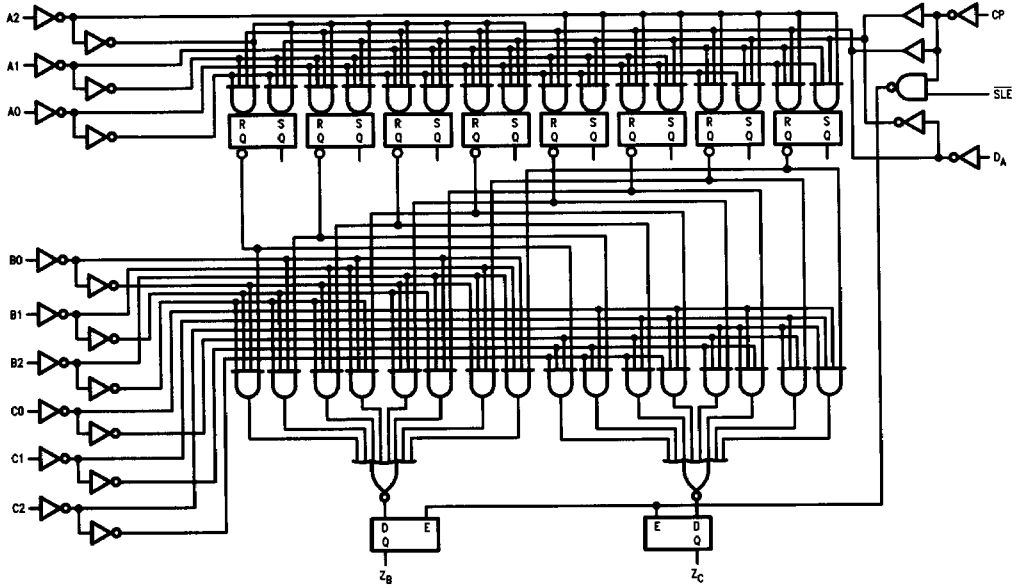


FIGURE a. Parallel Expansion

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Logic Diagram



TL/F/9794-3