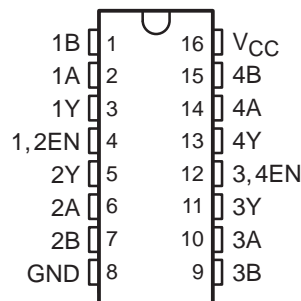


SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145B – OCTOBER 1990 – REVISED MAY 1995

- Meet or Exceed the Requirements of ANSI Standard EIA/TIA-422-B, RS-423-B, and RS-485
- Meet ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range –12 V to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 k Ω Min
- Operate From Single 5-V Supply
- Low-Power Requirements
- Plug-In Replacement for MC3486

D OR N PACKAGE
(TOP VIEW)



description

The SN65175 and SN75175 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485, and several ITU recommendations. These standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of ± 12 V. The SN65175 and SN75175 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN65175 is characterized for operation from -40°C to 85°C . The SN75175 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \geq -0.2$ V	H	L
X	L	Z
Open circuit	H	?

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

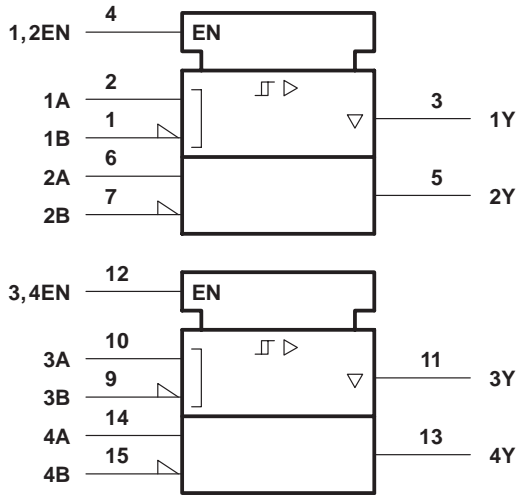
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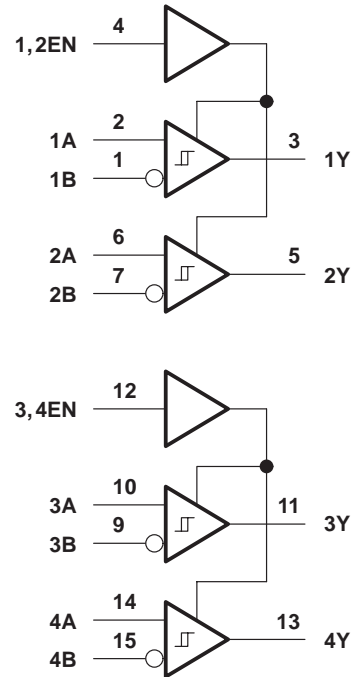
SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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logic symbol†

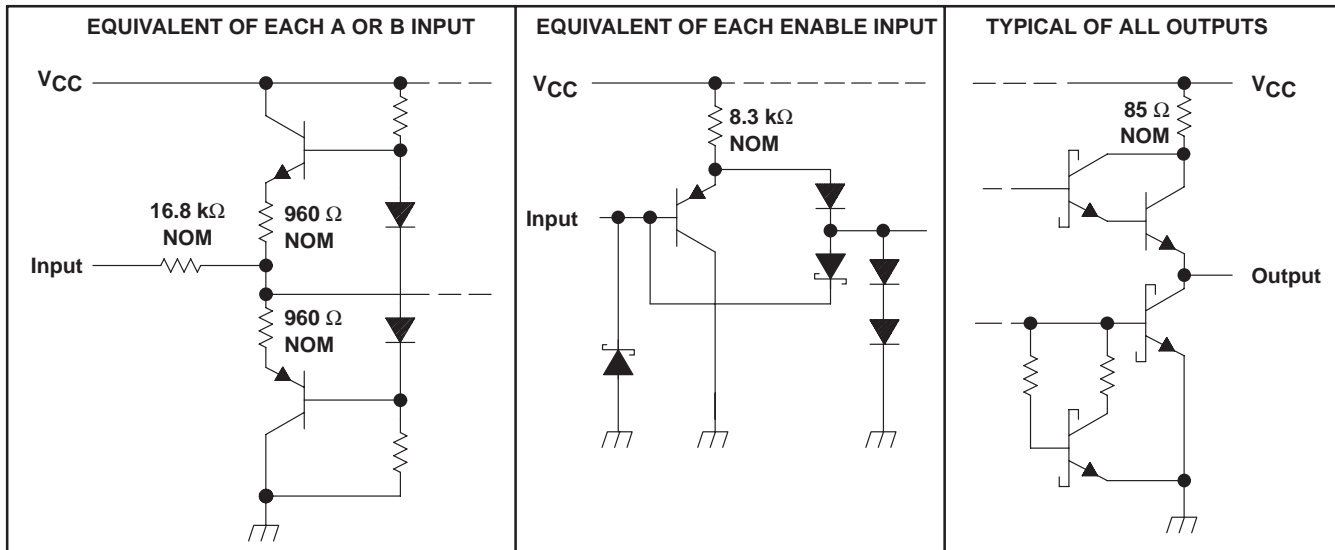


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage V_I , (A or B inputs)	± 25 V
Differential input voltage, V_{ID} (see Note 2)	± 25 V
Enable input voltage, V_I , EN	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN65175	–40°C to 85°C
SN75175	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 12	V
Differential input voltage, V_{ID}			± 12	V
High-level enable-input voltage, V_{IH}	2			V
Low-level enable-input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	SN65175	–40	85	°C
	SN75175	0	70	

SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IT+} Positive-going input threshold voltage	V _O = 2.7 V, I _O = -0.4 mA			0.2	V
V _{IT-} Negative-going input threshold voltage	V _O = 0.5 V, I _O = 16 mA	-0.2‡			V
V _{hys} Hysteresis voltage (V _{IT+} - V _{IT-})	See Figure 4		50		mV
V _{IK} Enable-input clamp voltage	I _I = -18 mA			-1.5	V
V _{OH} High-level output voltage	V _{ID} = 200 mV, I _{OH} = -400 μA, See Figure 1		2.7		V
V _{OL} Low-level output voltage	V _{ID} = -200 mV, See Figure 1			I _{OL} = 8 mA	0.45
				I _{OL} = 16 mA	0.5
I _{OZ} High-impedance-state output current	V _O = 0.4 V to 2.4 V			±20	μA
I _I Line input current	Other input at 0 V, See Note 3			V _I = 12 V	1
				V _I = -7 V	-0.8
I _{IH} High-level enable-input current	V _{IH} = 2.7 V			20	μA
I _{IL} Low-level enable-input current	V _{IL} = 0.4 V			-100	μA
r _i Input resistance			12		kΩ
I _{OS} Short-circuit output current§		-15		-85	mA
I _{CC} Supply current	Outputs disabled			70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low- to high-level output	See Figure 2		22	35	ns
t _{PHL} Propagation delay time, high- to low-level output			25	35	ns
t _{PZH} Output enable time to high level	See Figure 3		13	30	ns
t _{PZL} Output enable time to low level			19	30	ns
t _{PHZ} Output disable time from high level	See Figure 3		26	35	ns
t _{PLZ} Output disable time from low level			25	35	ns



PARAMETER MEASUREMENT INFORMATION

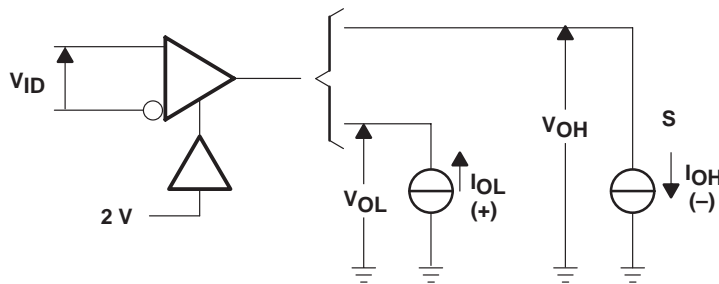
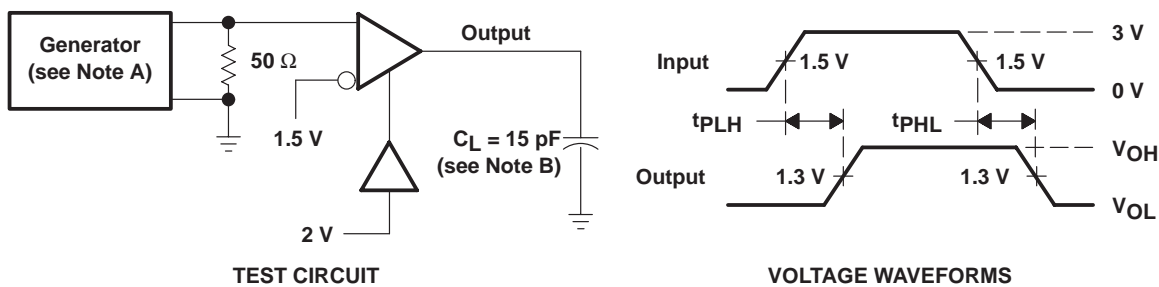


Figure 1. V_{OH} , V_{OL}



TEST CIRCUIT

VOLTAGE WAVEFORMS

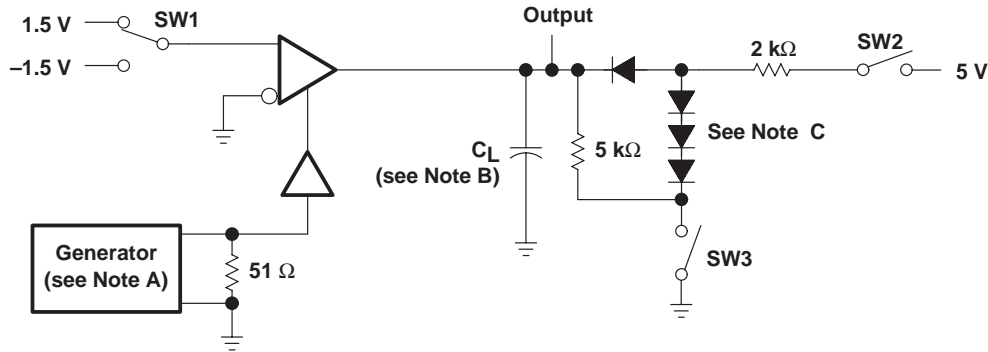
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 2. Test Circuit and Voltage Waveforms

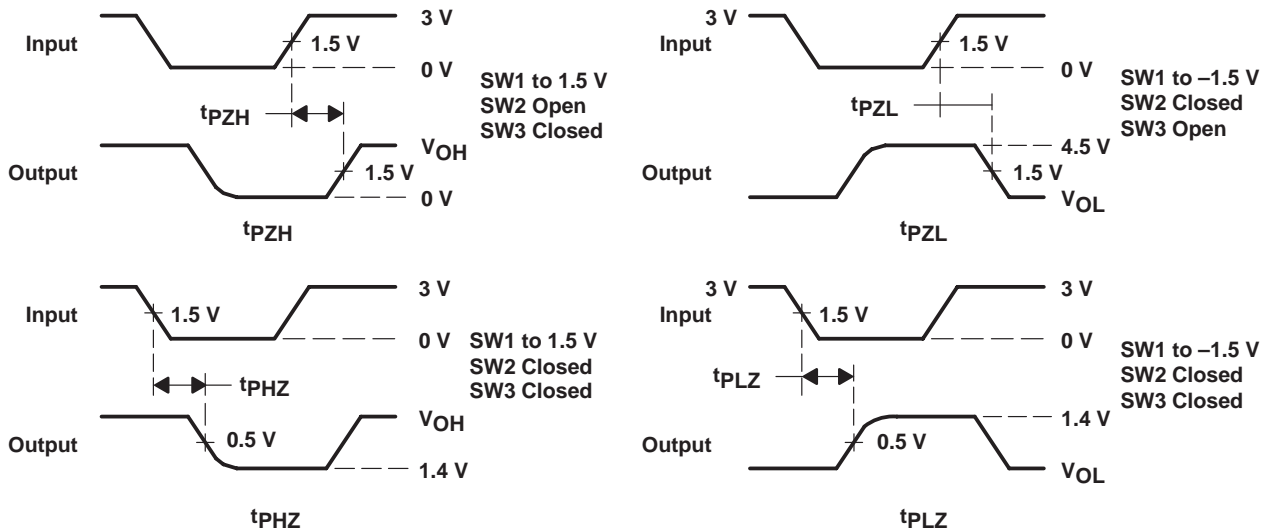
SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

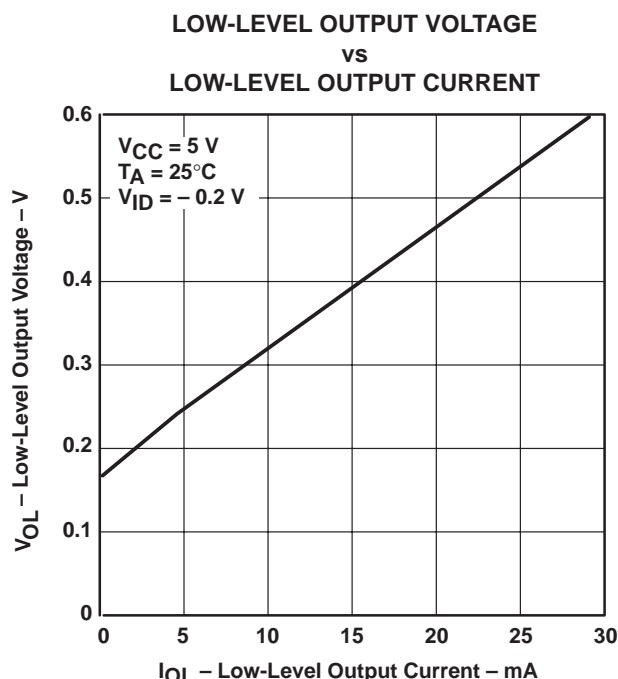
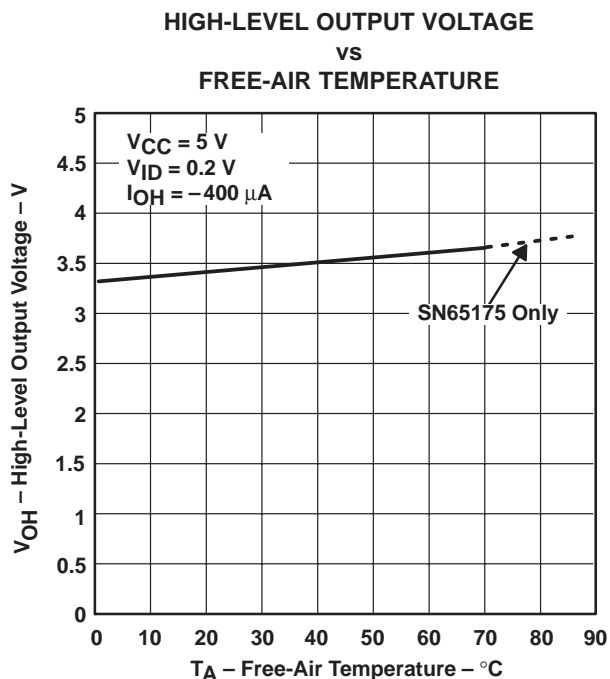
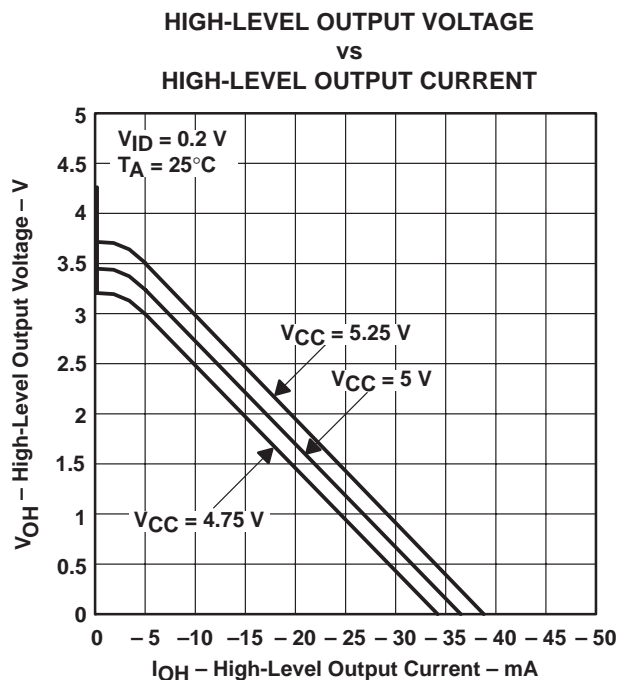
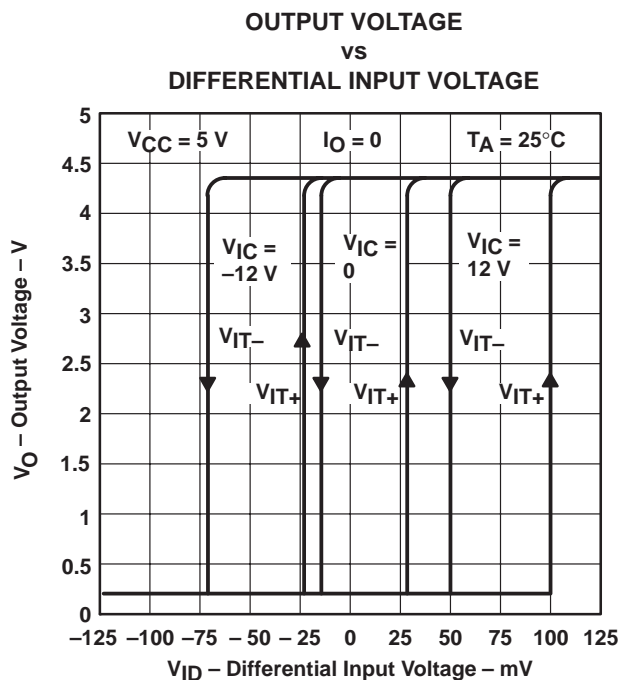


VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle = 50%, $t_f \leq 6 \text{ ns}$, $t_r \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.
 C. All diodes are 1N916 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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TYPICAL CHARACTERISTICS

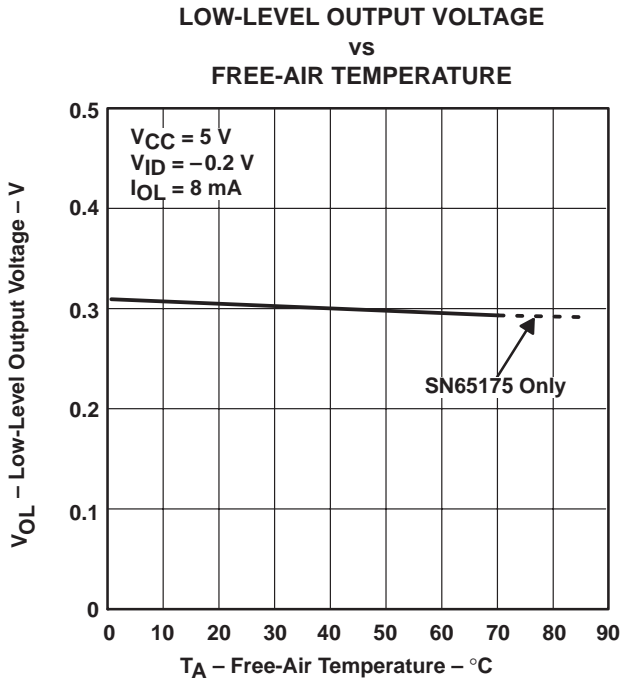


Figure 8

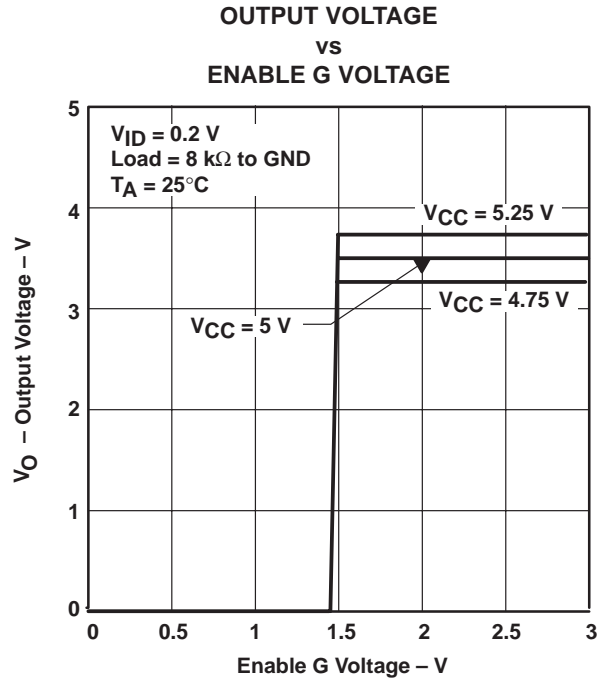


Figure 9

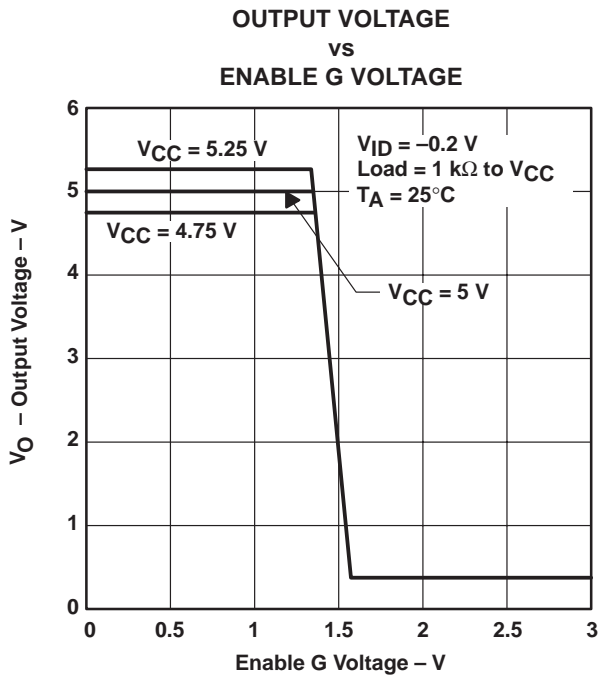


Figure 10

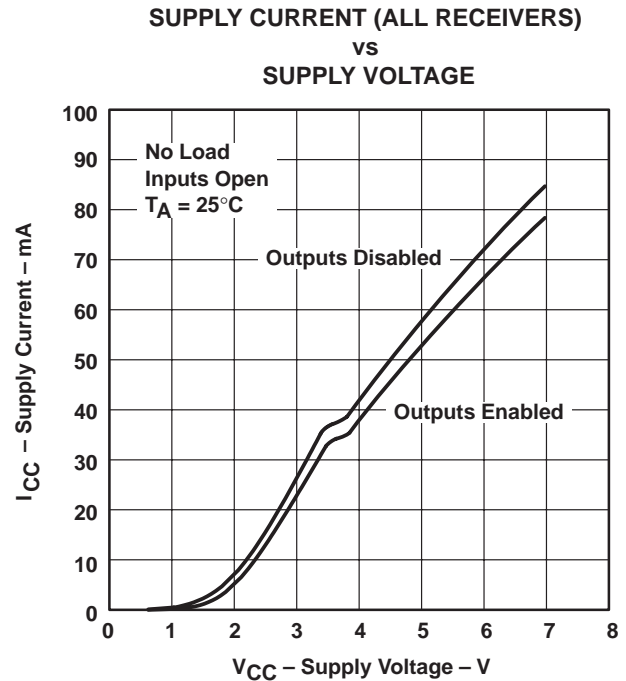
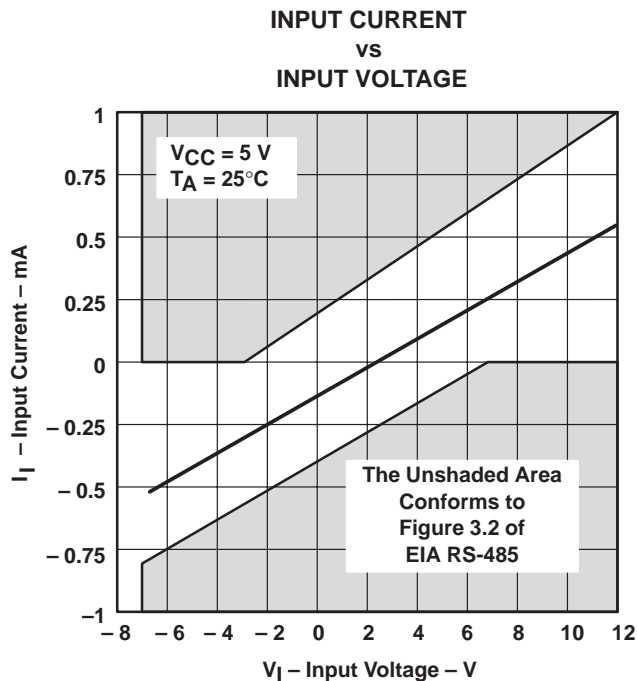
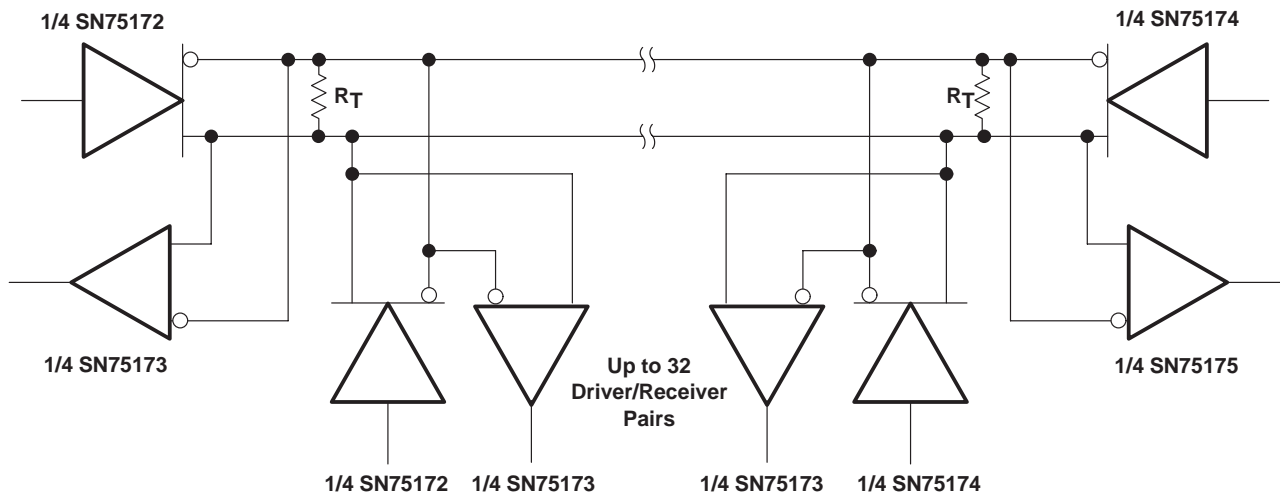


Figure 11

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 13. Typical Application Circuit

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SN75175, QUADRUPLE DIFFERENTIAL LINE RECEIVER

Device Status: Active

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- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Related Documents](#)
- > [Development Tools](#)
- > [Applications](#)

Parameter Name	SN75175
Receivers Per Package	4
Receiver tpd (ns)	35
Supply Voltage(s) (V)	5
ICC (max) (mA)	70
Footprint	MC3486

Description

The SN65175 and SN75175 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485, and several ITU recommendations. These standards are for balanced multipoint bus transmission at rates up to 10megabits per second. Each of the two pairs of receivers has a common active-high enable.

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H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

Features

- Meet or Exceed the Requirements of ANSI Standard EIA/TIA-422-B, RS-423-B, and RS-485
- Meet ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range
-12 V to 12 V

- Input Sensitivity...±200 mV
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- High Input Impedance...12 k Ω Min
- Operate From Single 5-V Supply
- Low-Power Requirements
- Plug-In Replacement for MC3486

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Datasheets

Full datasheet in Acrobat PDF: [slls145b.pdf](#) (152 KB)

Full datasheet in Zipped PostScript: [slls145b.psz](#) (133 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN75175D	D	16	0 TO 70	ACTIVE	2.54	40	Check stock or order
SN75175DR	D	16	0 TO 70	ACTIVE	2.12	2500	Check stock or order
SN75175J	J	16		OBSOLETE			
SN75175N	N	16	0 TO 70	ACTIVE	2.00	25	Check stock or order
SN75175NS	NS	16	0 TO 70	ACTIVE			Check stock or order

Application Reports

- [422 AND 485 OVERVIEW AND SYSTEM CONFIGURATIONS](#) (SLLA070 - Updated: 02/15/2000)
- [ANALOG APPLICATIONS JOURNAL, FEBRUARY 2000](#) (SLYT012A - Updated: 03/23/2000)
- [ANALOG APPLICATIONS JOURNAL, NOVEMBER 1999](#) (SLYT010A - Updated: 03/23/2000)
- [COMPARING BUS SOLUTIONS](#) (SLLA067 - Updated: 03/06/2000)
- [ELECTROSTATIC DISCHARGE APPLICATION NOTE](#) (SSYA008 - Updated: 05/05/1999)
- [INTERFACE CIRCUITS FOR TIA/EIA-485](#) (SLLA036 - Updated: 03/26/2000)
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- [SKEW DEFINITIONS](#) (SLLA060 - Updated: 08/13/1999)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS](#) (SZZA017A - Updated: 09/15/1999)

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- [A STATISTICAL SURVEY OF COMMON-MODE NOISE](#) (SLLA057, 131 KB - Updated: 12/23/1999)

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