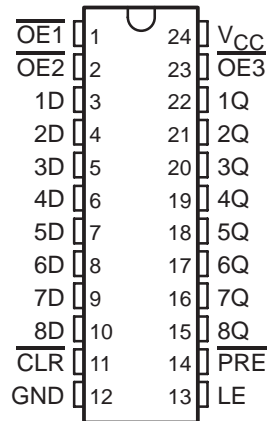


SN74ALS845 8-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SDAS233A – DECEMBER 1983 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs to Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

Because the clear ($\overline{\text{CLR}}$) and preset ($\overline{\text{PRE}}$) inputs are independent of the clock (CLK) input, taking $\overline{\text{CLR}}$ low causes the eight Q outputs to go low. Taking $\overline{\text{PRE}}$ low causes the eight Q outputs to go high. When both $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are taken low, the outputs follow the preset condition.

The buffered output-enable ($\overline{\text{OE1}}$, $\overline{\text{OE2}}$, and $\overline{\text{OE3}}$) inputs can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

The output enables do not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The -1 version of the SN74ALS845 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA.

The SN74ALS845 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

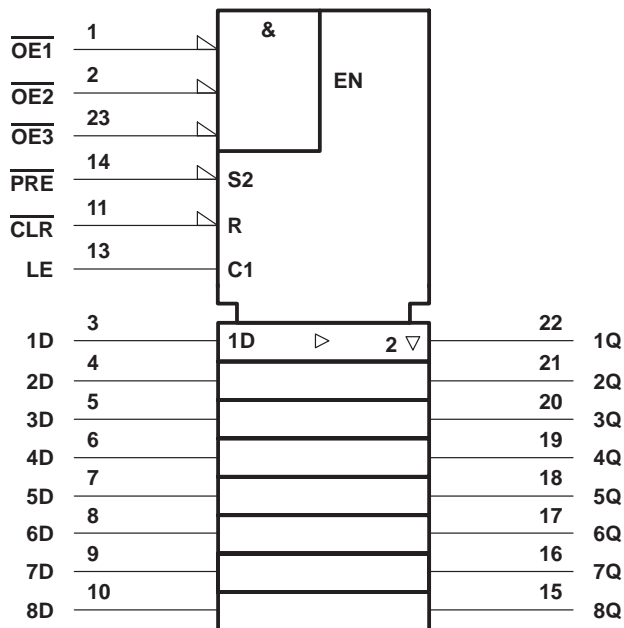
INPUTS							OUTPUT Q
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	$\overline{\text{OE3}}$	LE	D	
L	X	L	L	L	X	X	H
H	L	L	L	L	X	X	L
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	L	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

SN74ALS845

8-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

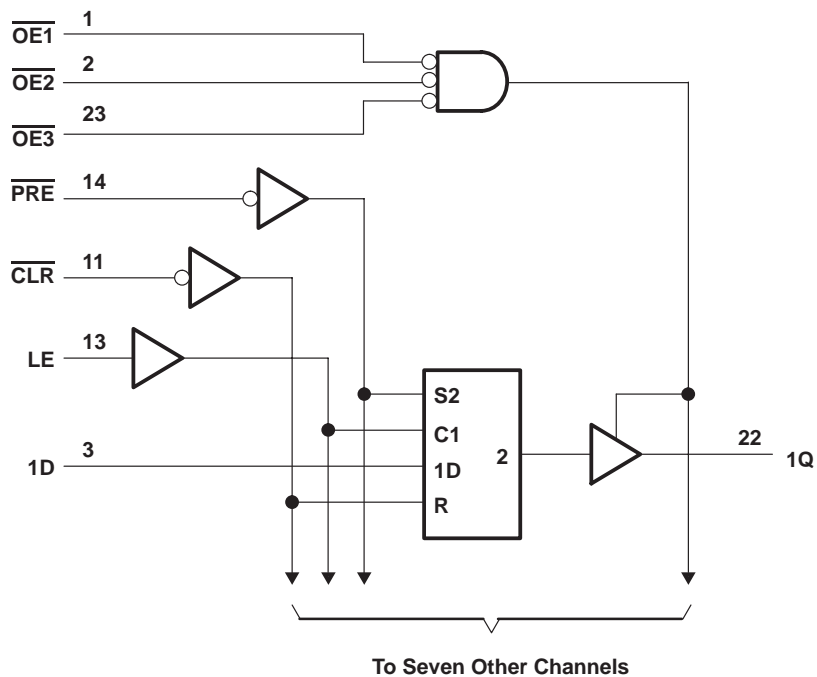
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74ALS845

8-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SDAS233A – DECEMBER 1983 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
				48‡	
t_w	Pulse duration	CLR or PRE low		35	ns
		LE high		20	
t_{su}	Setup time, data before LE↓	10			ns
t_h	Hold time, data after LE↓	5			ns
T_A	Operating free-air temperature	0		70	°C

‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -2.6$ mA	2.4	3.2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA	0.25	0.4	V
		$I_{OL} = 24$ mA	0.35	0.5	
		$I_{OL} = 48$ mA‡	0.35	0.5	
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			20	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–20	μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.1	mA
$I_O^¶$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high	21	36	mA
		Outputs low	41	67	
		Outputs disabled	25	42	

‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN74ALS845

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SDAS233A – DECEMBER 1983 – REVISED JANUARY 1995

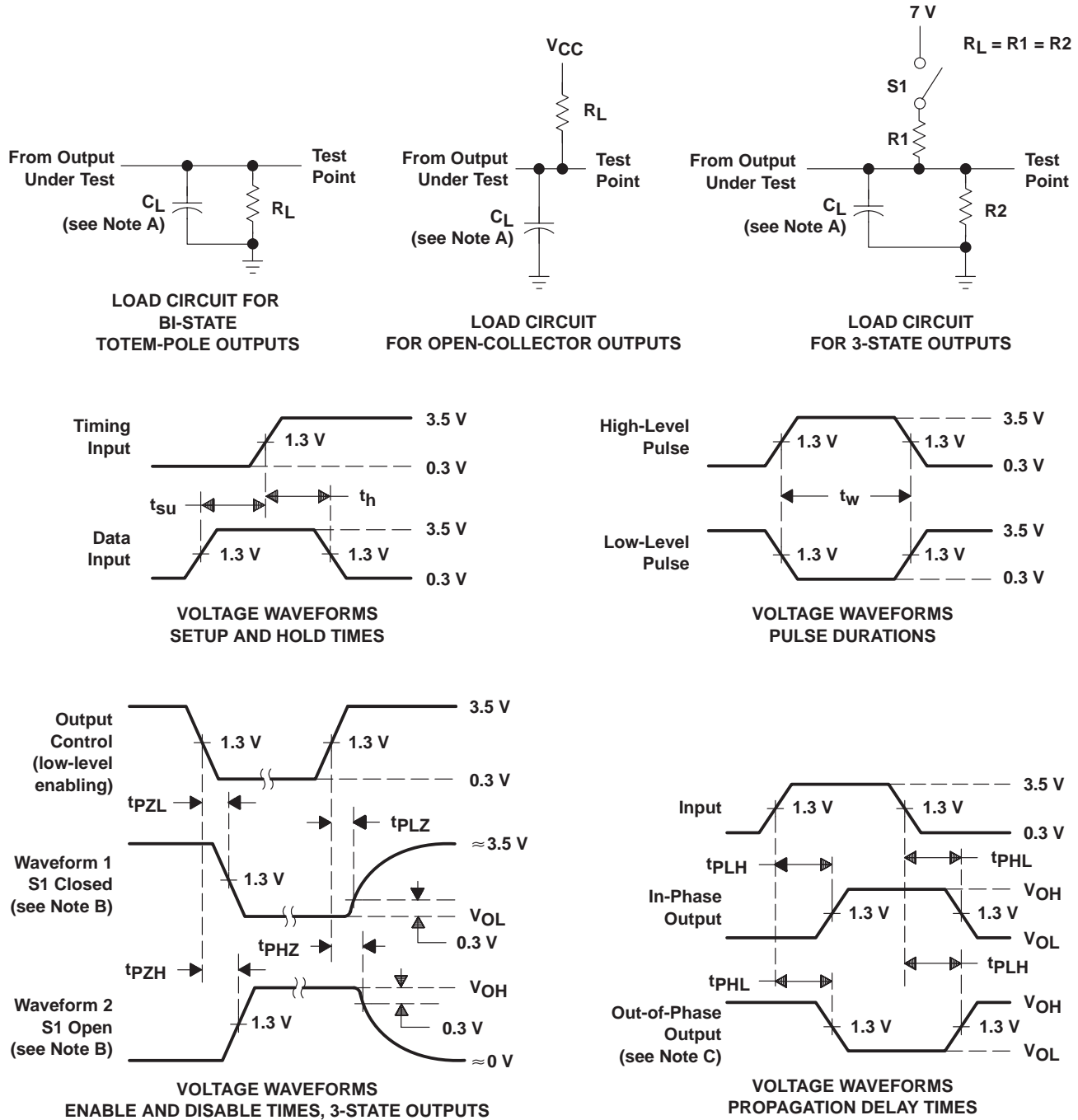
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			MIN	MAX	
t _{PLH}	D	Q	2	13	ns
t _{PHL}			4	18	
t _{PLH}	LE	Q	5	21	ns
t _{PHL}			8	26	
t _{PLH}	$\overline{\text{PRE}}$	Q	6	22	ns
t _{PHL}	$\overline{\text{CLR}}$		6	24	
t _{PZH}	$\overline{\text{OE}}$	Q	3	16	ns
t _{PZL}			5	18	
t _{PHZ}	$\overline{\text{OE}}$	Q	1	11	ns
t _{PLZ}			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS845-1NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS845DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS845NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS845NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

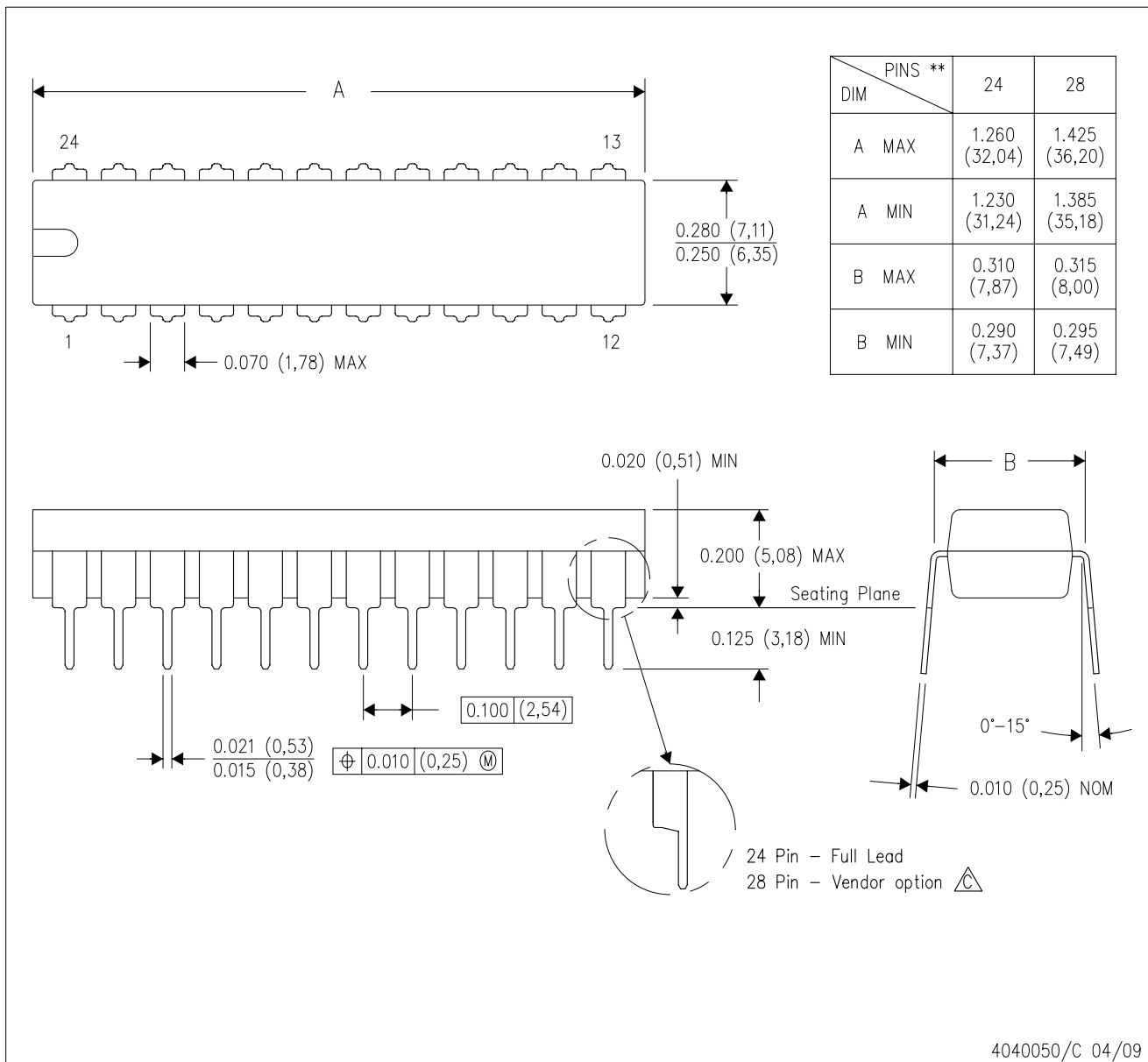
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MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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