SSI 32F8120
Low-Power Programmable Electronic Filter

January 1994

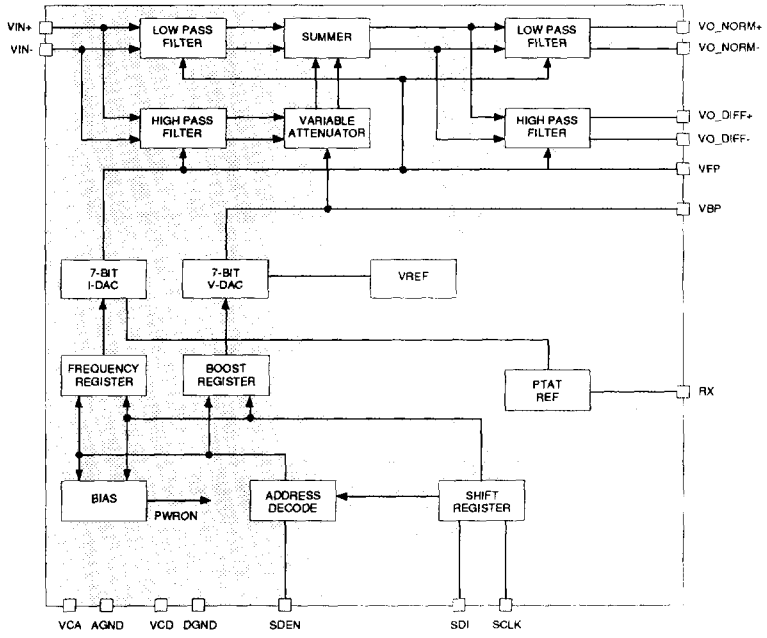
DESCRIPTION

The SSI 32F8120 is a continuous time, low pass filter with programmable bandwidth and high frequency boost. The low pass filter is a 2 zero / 7 pole 0.05° phase equiripple type, featuring excellent group delay characteristics. It features 1.5 - 8 MHz programmable bandwidth and 0-10 dB programmable boost. Both functions are controlled by 7-bit command words, which are input via a 3-line serial interface.

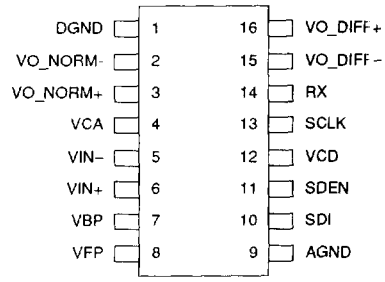
FEATURES

- **Programmable filter cutoff frequency (fc =1.5 to 8 MHz) with no external components**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **± 10% cutoff frequency accuracy**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device Idle mode**
- **+5V only operation**
- **No external filter components required**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



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CAUTION: Use handling procedures necessary for a static sensitive component.

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FUNCTIONAL DESCRIPTION

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8120 programmable electronic filter can be set to a filter cutoff frequency from 1.5 to 8 MHz. The cutoff frequency can be set by using the serial port through pins SDI, SDEN, and SCLK. SDI is the serial data input for an 8-bit control shift register, SDEN is the control register enable, and SCLK is the control register clock. The data packet is transmitted MSB (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. See Table 1.

fc is determined by the equation:

fc (MHz) = 0.061321 (F_Code) + 0.212264

1.5 MHz ≤ fc ≤ 8 MHz

21 ≤ F_ Code ≤ 127

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the V-DAC output, the boost can be determined. The amount of boost at the cutoff frequency is related to the V-DAC output by the following formula:

$$[\text{Output of V-DAC} = \text{VBP} = \text{VREF} \times \frac{\text{S\_Code}}{127}]$$

BOOST (dB) = 20•log [0.01703 (S_Code) +1].

TABLE 1

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
X	0	0	0	S-MSB REGISTER	X	S6	S5	S4
X	0	0	1	S-LSB REGISTER	S3	S2	S1	S0
X	0	1	0	F-MSB REGISTER	X	F6	F5	F4
X	0	1	1	F-LSB REGISTER	F3	F2	F1	F0
X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = 7-bit Boost (Slimming) Control
F = 7-bit Frequency (Bandwidth) Control
P = Power Down Control; PO = 1 for power up; PO = 0 for power down

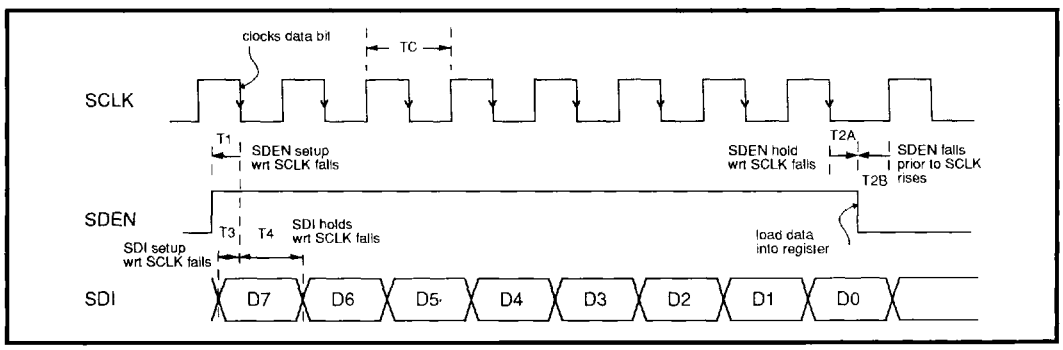

FIGURE 1: Serial Port Timing Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN–	I	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	O	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector.
VO_DIFF+ VO_DIFF–	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum pulse pairing, these outputs should be AC coupled to the pulse detector.
SDEN	I	SERIAL DATA ENABLE. A logic HIGH level allows SERIAL CLOCK to clock data into the control register via the SERIAL DATA input. A logic LOW level latches the register data and issues the information to the appropriate circuitry.
SCLK	I	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	I	SERIAL DATA INPUT.
RX	–	REFERENCE CURRENT SET. With an external resistor (Rx = 5 kΩ ±1%) to ground, this pin gives a voltage proportional to the absolute temperature, setting the range for VFP.
VCA	I	ANALOG +5 VOLT SUPPLY.
VCD	I	DIGITAL +5 VOLT SUPPLY.
AGND	I	ANALOG GROUND.
DGND	I	DIGITAL GROUND.
VBP	O	BOOST PROGRAMMING VOLTAGE. Output of V-DAC which programs the boost.
VFP	O	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. Output of I-DAC which programs the cutoff frequency.*

*A minimum load resistance of 150 kΩ should be used to avoid affecting the total minimum on-chip resistance of 1.35 kΩ.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Junction Operating Temperature, Tj	+130 °C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCC V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	0.5W
T1 Lead Temperature (1/16" from case for 10 seconds)	260 °C
* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.	

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.5V < VCC < 5.5V
Ambient Temperature	0 °C < Ta < 70 °C
Tj Junction Temperature	0 °C < Tj < 130 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Isupply	VCC = 5.5V, outputs unloaded		55	75	mA
Idle Mode Current			9	13	mA
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs

DC Characteristics

VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	−1.5			mA

Filter Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
fc Filter Cutoff Frequency	21 ≤ F_Code ≤ 127	1.5		8	MHz
FCA Filter *fc* Accuracy	F_Code = 127	-10		+10	%
	F_Code = 21	-15		+15	%
Cutoff Resolution	1.5 to 8 MHz	100			kHz
AO VO_NORM Diff Gain	F = 0.67 *fc*	0.7		1.1	V/V
AD VO_DIFF Diff Gain	F = 0.67 *fc*	0.90 AO		1.2 AO	V/V
FB Frequency Boost at *fc*	FB(dB) = 20 log [0.01703 (S_Code) +1]	0		10	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta < 22 °C	−1.5		+1.5	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta > 22 °C	−1		+1	dB
TGD0 Group Delay Variation Without Boost	0.2 *fc* - *fc*	−2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz gdm = group delay magnitude	*fc* - 1.75 *fc*	−3% gdm		+3% gdm	ns
TGDB Group Delay Variation With Boost	0.2 *fc* - *fc*	−2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz	*fc* - 1.75 *fc*	−3% gdm		+3% gdm	ns
Boost Resolution	1.5 to 8 MHz	.25			dB
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 1000 pF capacitor across Rx F_Code = 127	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 3.5% max, VBP = 0, VO_DIFF 1000 pF capacitor across Rx F_Code = 127	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 1000 pF capacitor across Rx F_Code = 21	1.0			Vppd
VOF Filter Output Dynamic Range	THD = 2.0% max, VBP = 0, VO_DIFF 1000 pF capacitor across Rx F_Code = 21	1.0			Vppd

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ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RIN Filter Diff Input Resistance		3.0			kΩ
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 0 dB Boost 50Ω input		1.8	3	mVRms
	f_c = 8 MHz 10 dB Boost		2.35	4	mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 0 dB Boost 50Ω input		4.2	6	mVRms
	f_c = 8 MHz 10 dB Boost		5.85	9	mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			60	Ω
TC Period, SCLK		100			ns
T1 SDEN Setup to SCLK Falls		10		TC/2-10	ns
T2A SDEN Hold wrt SCLK Falls		10		TC/4	ns
T2B SDEN Falls prior to SCLK Rises		25			ns
T3 SDI Setup to SCLK Falls		25			ns
T4 SDI Hold to SCLK Falls		25			ns
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCA, VCD	40	70		dB
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @5 MHz	30	50		dB
Bias: Vin+, Vin-	VCC = 5V	2.5	2.9	3.3	V
VO_NORM+, VO_NORM-	VCC = 5V	2.8	3.2	3.6	V
VO_DIFF+, VO_DIFF-	VCC = 5V	2.8	3.2	3.6	V
Output offset Normal and Differentiated		-150		+150	mV

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 2 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 4.40 MHz

$f$peak = 2.46 MHz

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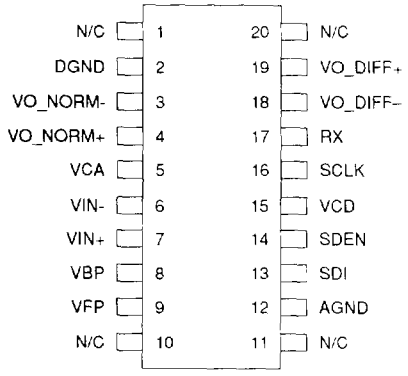
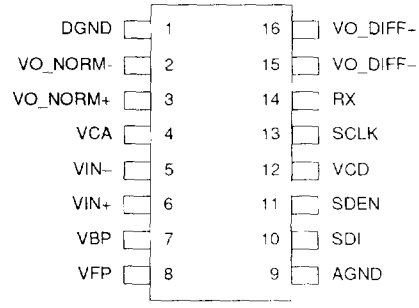
PACKAGE PIN DESIGNATIONS
(Top View)



20-Lead SOV



16-Lead SOL

THERMAL CHARACTERISTICS: θja

16-lead SOL	100° C/W
20-lead SOV	125° C/W

CAUTION: Use handling procecures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8120	16-Lead SOL	32F8120-CL	32F8120-CL
	20-Lead SOV	32F8120-CV	32F8120-CV

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Patent No. 5,063,309, Patent Pending 823,067