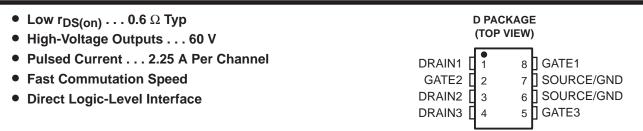
## TPIC2322L 3-CHANNEL COMMON-SOURCE LOGIC-LEVEL POWER DMOS ARRAY

SLIS036A - JUNE 1994 - REVISED OCTOBER 1994

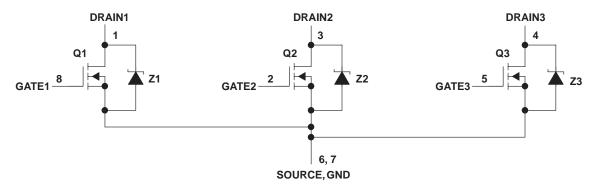


### description

The TPIC2322L is a monolithic logic-level power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains.

The TPIC2322L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of  $-40^{\circ}$ C to  $125^{\circ}$ C.

#### schematic



## absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V <sub>DS</sub>	
Drain-to-GND voltage	
Gate-to-source voltage, V <sub>GS</sub>	
Continuous drain current, each output, all outputs on, T <sub>C</sub> = 25°C	0.75 A
Continuous source-to-drain diode current, T <sub>C</sub> = 25°C	0.75 A
Pulsed drain current, each output, I <sub>max</sub> , T <sub>C</sub> = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E <sub>AS</sub> , T <sub>C</sub> = 25°C (see Figure 4)	30.4 mJ
Continuous total power dissipation at (or below) $T_C = 25^{\circ}C$ (see Figure 15)	0.95 W
Operating virtual junction temperature range, T <sub>J</sub>	–40°C to 150°C
Operating case temperature range, T <sub>C</sub>	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.



## TPIC2322L 3-CHANNEL COMMON-SOURCE LOGIC-LEVEL POWER DMOS ARRAY

SLIS036A - JUNE 1994 - REVISED OCTOBER 1994

## electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST COND	MIN	TYP	MAX	UNIT		
V <sub>(BR)</sub> DSX	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A},$	$V_{GS} = 0$	60			V	
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	I <sub>D</sub> = 1 mA, See Figure 5	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V	
V <sub>(BR)</sub>	Reverse drain to GND breakdown voltage	Drain to GND current	t = 250 μA	100			V	
V <sub>DS(on)</sub>	Drain-to-source on-state voltage	I <sub>D</sub> = 0.75 A, V <sub>GS</sub> = 5 V, See Notes 2 and 3			0.45	0.53	V	
V <sub>F</sub> (SD)	Forward on-state voltage, source-to-drain	Is = 0.75 A, See Notes 2 and 3 ar	I <sub>S</sub> = 0.75 A, V <sub>GS</sub> = 0 See Notes 2 and 3 and Figure 12		0.85	1	V	
		V <sub>DS</sub> = 48 V,	T <sub>C</sub> = 25°C		0.05	1	•	
IDSS	Zero-gate-voltage drain current	$V_{GS} = 0$	T <sub>C</sub> = 125°C		0.5	10	μΑ	
IGSSF	Forward gate current, drain short circuited to source	V <sub>GS</sub> = 16 V,	$V_{DS} = 0$		10	100	nA	
IGSSR	Reverse gate current, drain short circuited to source	$V_{SG} = 16 V$ ,	$V_{DS} = 0$		10	100	nA	
	Lookaga aurrant drain to CND	\/p a \ p = 49 \/	T <sub>C</sub> = 25°C		0.05	1^	^	
l <sub>lkg</sub>	Leakage current, drain-to-GND	V <sub>DGND</sub> = 48 V	T <sub>C</sub> = 125°C		0.5	10	μΑ	
<b>#</b>	Static drain-to-source on-state resistance	$V_{GS} = 5 \text{ V},$ $I_{D} = 0.75 \text{ A},$	T <sub>C</sub> = 25°C		0.6	0.7	Ω	
<sup>r</sup> DS(on)	Static drain-to-source on-state resistance	See Notes 2 and 3 and Figures 6 and 7	T <sub>C</sub> = 125°C		0.94	1	22	
9fs	Forward transconductance	V <sub>DS</sub> = 15 V, See Notes 2 and 3 a	I <sub>D</sub> = 0.5 A, nd Figure 9	0.75	0.9		S	
C <sub>iss</sub>	Short-circuit input capacitance, common source					115	145	
Coss	Short-circuit output capacitance, common source	$V_{DS} = 25 \text{ V},$	$V_{GS} = 0$ ,		60	75	pF	
C <sub>rss</sub>	Short-circuit reverse transfer capacitance, common source	f = 1 MHz,	See Figure 11		30	40	ы	

# source-to-drain diode characteristics, $T_{C}$ = 25°C (see schematic diagram)

	PARAMETER	TEST C	MIN	TYP	MAX	UNIT	
t <sub>rr</sub>	Reverse-recovery time	I <sub>F</sub> = 0.375 A,	V <sub>DS</sub> = 48 V,		85		ns
Q <sub>RR</sub>	Total diode charge	di/dt = 100 A/μs,	See Figures 1 and 14		0.19		μС

NOTES: 2. Technique should limit T<sub>J</sub> – T<sub>C</sub> to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

## resistive-load switching characteristics, T<sub>C</sub> = 25°C

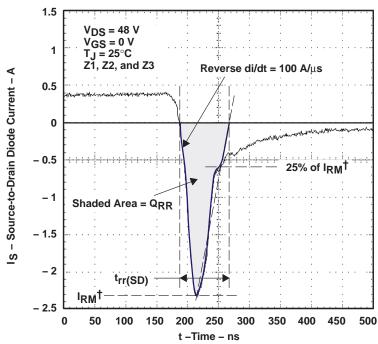
	PARAMETER TEST CONDITIONS			MIN	TYP	MAX	UNIT								
td(on)	Turn-on delay time					21	42								
td(off)	Turn-off delay time	$V_{DD} = 25 \text{ V},$	$R_L = 67 \Omega$ ,	$t_{en} = 10 \text{ ns},$		26	52								
t <sub>r</sub>	Rise time	$t_{dis} = 10 \text{ ns},$				14	28	ns							
t <sub>f</sub>	Fall time	1				13	26								
Qg	Total gate charge	1				1.8	2.3								
Q <sub>gs(th)</sub>	Threshold gate-to-source charge	V <sub>DS</sub> = 48 V,					VDS = 48 V, See Figure 3			$I_D = 0.375 A,$	$V_{GS} = 5 V$ ,		0.4	0.5	nC
Q <sub>gd</sub>	Gate-to-drain charge	Gee Figure 3				1.1	1.4								
LD	Internal drain inductance					5		al I							
LS	Internal source inductance				5		nΗ								
Rg	Internal gate resistance					0.25		Ω							

## thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		°C/W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

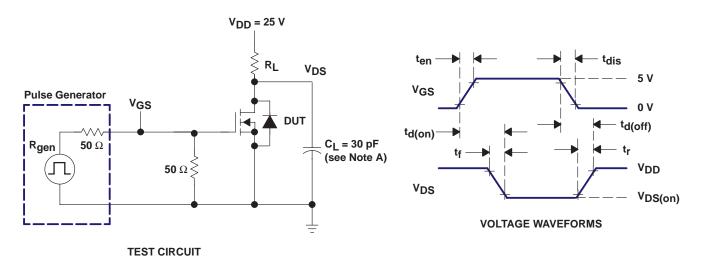
## PARAMETER MEASUREMENT INFORMATION



† I<sub>RM</sub> = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

## PARAMETER MEASUREMENT INFORMATION



NOTE A: C<sub>I</sub> includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

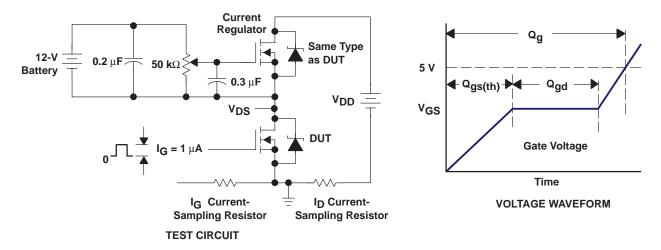
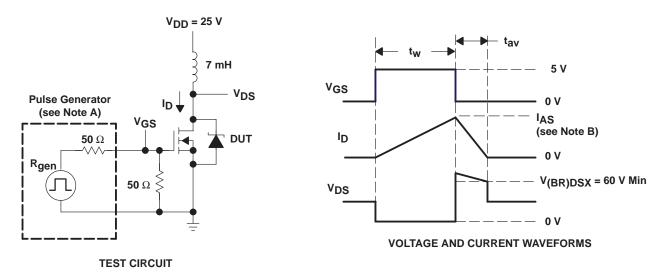


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:  $t_f \le 10$  ns,  $t_f \le 10$  ns,  $Z_O = 50$   $\Omega$ .

B. Input pulse duration  $(t_w)$  is increased until peak current  $I_{AS} = 2.25 \text{ A}$ .

Energy test level is defined as  $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2}$ 

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

## TYPICAL CHARACTERISTICS

# **JUNCTION TEMPERATURE** 2.5 VGS(th) - Gate-to-Source Threshold Voltage - V $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ 1.5 $I_D = 100 \mu A$ 0.5 -40 -20 0 40 60 80 100 120 140 160 20 T<sub>.I</sub> - Junction Temperature - °C

Figure 5

**GATE-TO-SOURCE THRESHOLD VOLTAGE** 

## STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

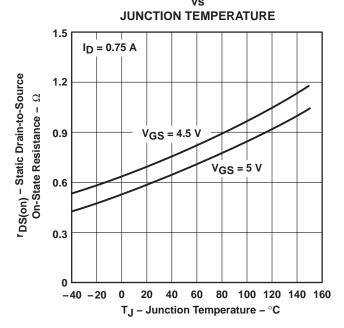


Figure 6

#### TYPICAL CHARACTERISTICS

#### STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

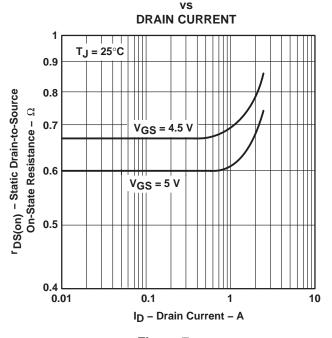


Figure 7

## **DRAIN-TO-SOURCE VOLTAGE** 2.25 △V<sub>GS</sub> = 0.2 V $T_J = 25^{\circ}C$ 2 1.75 V<sub>GS</sub> = 5 V V<sub>GS</sub> = 4 V D- Drain Current - A 1.5 1.25 1 0.75 V<sub>GS</sub> = 3 V 0.5 0.25 0 V<sub>DS</sub> - Drain-to-Source Voltage - V

**DRAIN CURRENT** 

Figure 8

# DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

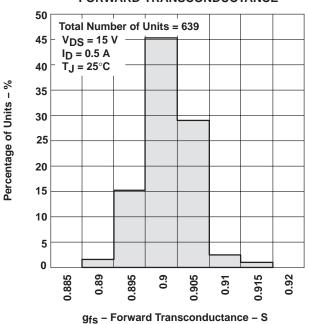


Figure 9

# DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

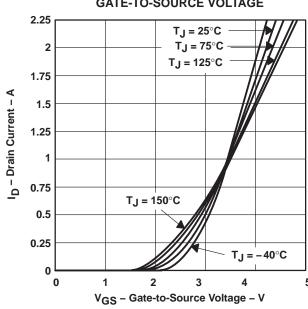


Figure 10

## **TYPICAL CHARACTERISTICS**

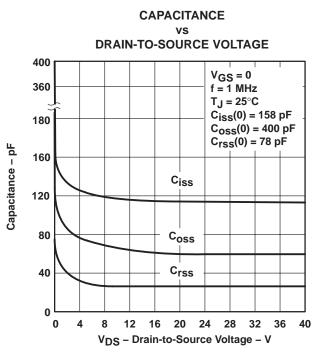


Figure 11

**DRAIN-TO-SOURCE VOLTAGE AND** 

**GATE-TO-SOURCE VOLTAGE** 

#### **GATE CHARGE** 70 14 $I_D = 0.375 A$ T<sub>.1</sub> = 25°C 60 12 See Figure 3 VDS - Drain-to-Source Voltage - V VGS - Gate-to-Source Voltage -10 50 $V_{DD} = 20 V$ 40 8 $V_{DD} = 30 V$ 6 30 20 $V_{DD} = 48 V$ 2 10

 $V_{DD} = 20 V$ 

1.5

0

Figure 13

Q<sub>q</sub> - Gate Charge - nC

0.5

0

0

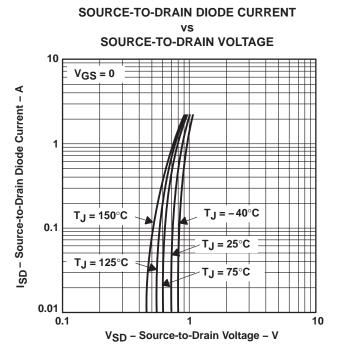


Figure 12

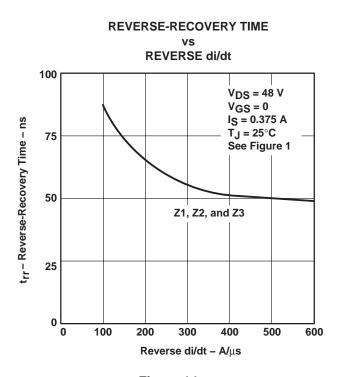
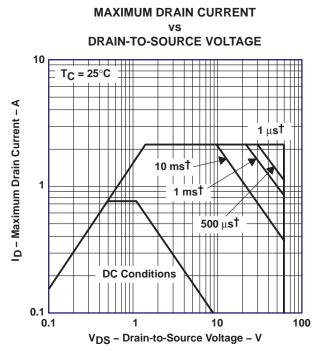


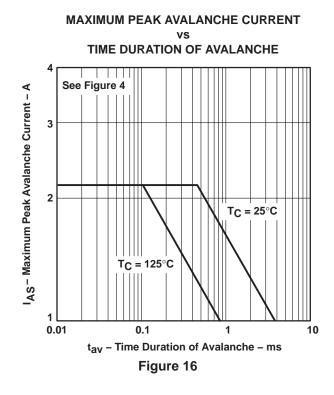
Figure 14

## THERMAL INFORMATION



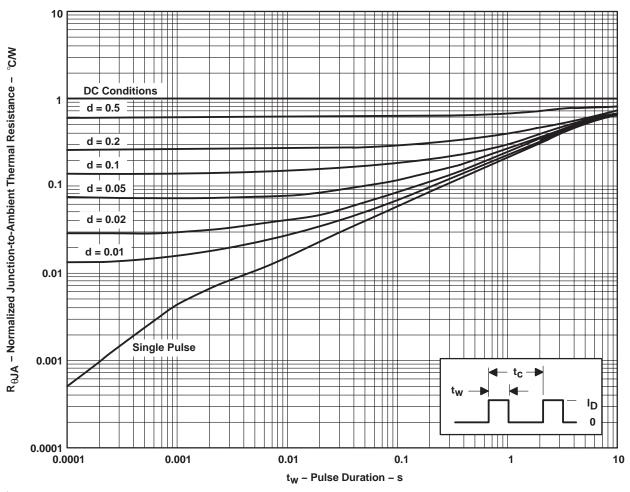
† Less than 2% duty cycle

Figure 15



## THERMAL INFORMATION

# D PACKAGE<sup>†</sup> NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTES:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   $t_W = \text{pulse duration}$   $t_C = \text{cycle time}$  $d = \text{duty cycle} = t_W/t_C$ 

Figure 17





## PACKAGE OPTION ADDENDUM

8-Apr-2005

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC2322LD	OBSOLETE	SOIC	D	8	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

#### Products Applications

Audio www.ti.com/audio Automotive and Transportation www.ti.com/automotive **Amplifiers** amplifier.ti.com Communications and Telecom www.ti.com/communications **Data Converters** dataconverter.ti.com Computers and Peripherals www.ti.com/computers **DLP® Products** www.dlp.com Consumer Electronics www.ti.com/consumer-apps DSP dsp.ti.com **Energy and Lighting** www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical Logic Security www.ti.com/security logic.ti.com

Power Mgmt power.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID www.ti-rfid.com

OMAP Applications Processors www.ti.com/omap TI E2E Community e2e.ti.com

Wireless Connectivity www.ti.com/wirelessconnectivity