

# SN54HC173, SN74HC173 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982 — REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Gated Output-Control Lines for Enabling or Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

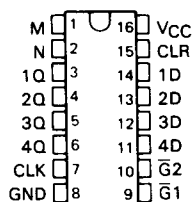
## description

The 'HC173 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased drive provide these flip-flops with the capability of being connected directly to and driving the lines in a bus-organized system without need for interface or pull-up components.

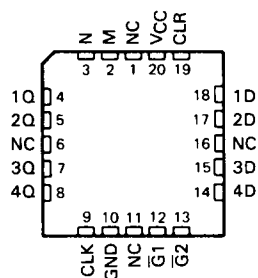
Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Gate output-control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54HC173 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC173 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC173 . . . J PACKAGE  
SN74HC173 . . . D OR N PACKAGE  
(TOP VIEW)



SN54HC173 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CLEAR	CLOCK	INPUTS			OUTPUT Q
		DATA ENABLE		DATA D	
		$\bar{G}1$	$\bar{G}2$		
H	X	X	X	X	L
L	L	X	X	X	$Q_0$
L	↑	H	X	X	$Q_0$
L	↑	X	H	X	$Q_0$
L	↑	L	L	L	L
L	↑	L	L	H	H

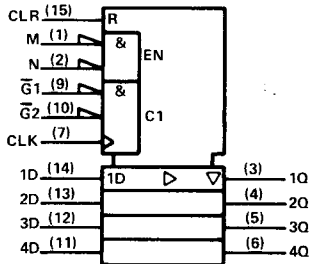
When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

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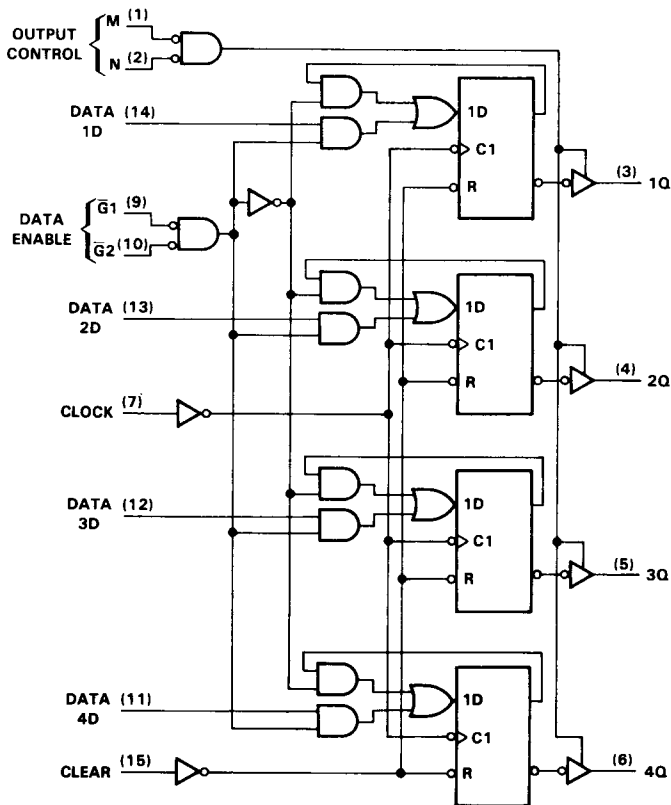
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

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## absolute maximum ratings over operating free-air temperature range<sup>†</sup>

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}(V_I < 0 \text{ or } V_I > V_{CC})$ .....	$\pm 20$ mA
Output clamp current, $I_{OK}(V_O < 0 \text{ or } V_O > V_{CC})$ .....	$\pm 20$ mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$ .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package .....	300 °C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package .....	260 °C
Storage temperature range .....	-65 °C to 150 °C

<sup>†</sup>Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## recommended operating conditions

			SN54HC173			SN74HC173			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage		2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0	0.3		0	0.3		V
		$V_{CC} = 4.5$ V	0	0.9		0	0.9		
		$V_{CC} = 6$ V	0	1.2		0	1.2		
$V_I$	Input voltage		0	$V_{CC}$		0	$V_{CC}$		V
$V_O$	Output voltage		0	$V_{CC}$		0	$V_{CC}$		V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000		0	1000		ns
		$V_{CC} = 4.5$ V	0	500		0	500		
		$V_{CC} = 6$ V	0	400		0	400		
$T_A$	Operating free-air temperature		-55	125		-40	85		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC173		SN74HC173		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}, I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
		4.5 V	3.98	4.30		3.7		3.84		
$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = -7.8 \text{ mA}$	2 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		6 V		0.001	0.1		0.1	0.1		
		4.5 V		0.17	0.26		0.4	0.33		
$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 6 \text{ mA}$	4.5 V		0.15	0.26		0.4	0.33	V	
		6 V		0.15	0.26		0.4	0.33		
$I_I$	$V_I = V_{CC} \text{ or } 0$	6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$	$\pm 1000$	nA	
$I_{OZ}$	$V_O = V_{CC} \text{ or } 0$	6 V		$\pm 0.01$	$\pm 0.5$		$\pm 10$	$\pm 5$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC} \text{ or } 0, I_O = 0$	6 V				8	160	80	$\mu\text{A}$	
$C_i$		2 to 6 V		3	10		10	10	pF	

**SN54HC173, SN74HC173**  
**4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC173		SN74HC173		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Input clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80	120	100	ns		
			4.5 V	16	24	20			
			6 V	14	20	17			
	CLR high	2 V	80	120	100	ns			
		4.5 V	16	24	20				
		6 V	14	20	17				
t <sub>su</sub>	Setup time before CLK1	$\overline{G}1$ and $\overline{G}2$	2 V	100	150	125	ns		
			4.5 V	20	30	25			
			6 V	17	25	21			
		Data	2 V	100	150	125	ns		
			4.5 V	20	30	25			
			6 V	17	25	21			
	CLR inactive	2 V	90	135	115	ns			
		4.5 V	18	27	23				
		6 V	15	23	19				
t <sub>h</sub>	Hold time after CLK1	$\overline{G}1$ and $\overline{G}2$	2 V	0	0	0	ns		
			4.5 V	0	0	0			
			6 V	0	0	0			
	Data	2 V	0	0	0	ns			
		4.5 V	0	0	0				
		6 V	0	0	0				

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## SN54HC173, SN74HC173 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC173		SN74HC173		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	8		4.2		5	MHz	
			4.5 V	31	46		21		25		
			6 V	36	55		25		29		
t <sub>PHL</sub>	CLR	Any	2 V		78	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		20	26		38		32	
t <sub>pd</sub>	CLK	Any	2 V		78	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		20	26		38		32	
t <sub>en</sub>	M or N	Any	2 V		78	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		15	26		38		32	
t <sub>dis</sub>	M or N	Any	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t <sub>t</sub>		Any	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C <sub>pd</sub>	Power dissipation capacitance	No load, T <sub>A</sub> = 25°C	29 pF typ
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 150$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC173		SN74HC173		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PHL</sub>	CLR	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t <sub>pd</sub>	CLR	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t <sub>en</sub>	M or N	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t <sub>t</sub>		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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