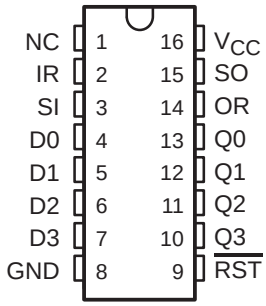
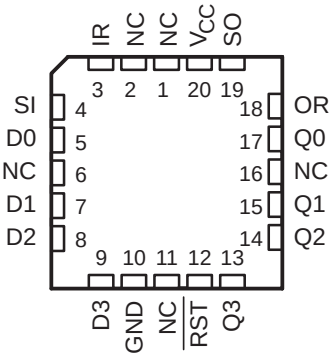
- **Asynchronous Operation**
- **Organized as 64 Words by 4 Bits**
- **Data Rates up to 30 MHz**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Package (DW), Plastic J-Leaded Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74ALS236 is a 256-bit memory utilizing advanced low-power Schottky IMPACT™ technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALS236 is designed to process data at rates up to 30 MHz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the shift-in (SI) input. When SI goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional shift-in pulses have no effect. Data is shifted out of memory on the falling edge of the shift-out (SO) input (see Figure 2). When the FIFO is empty, additional SO pulses have no effect. The last data word remains at the outputs until a new word falls through or reset ($\overline{RST}$) goes low.

Status of the SN74ALS236 FIFO memory is monitored by the output-ready (OR) and input-ready (IR) flags. When OR is high, valid data is available at the outputs. OR is low when SO is high and stays low when the FIFO is empty. IR is high when the inputs are ready to receive more data. IR is low when SI is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when SI goes low. If SO is held high during this time, the OR flag pulses high, indicating valid data at the outputs (see Figure 3).

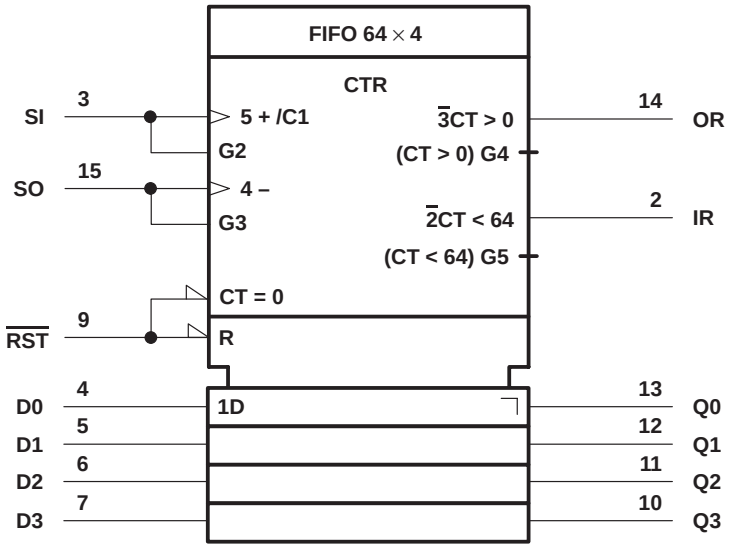
When the FIFO is full, data is shifted in automatically by holding SI high and taking SO low. One propagation delay after SO goes low, IR goes high. If SI is still high when IR goes high, data at the inputs is automatically shifted in. Since IR is normally low when the FIFO is full and SI is high, only a high-level pulse is seen on the IR output (see Figure 4).

description (continued)

The FIFO must be reset after power up with a low-level pulse on the master reset ($\overline{RST}$) input. This sets IR high and OR low, signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If SI is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until SI goes low. If SI goes low before $\overline{RST}$ goes high, the input data is not shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

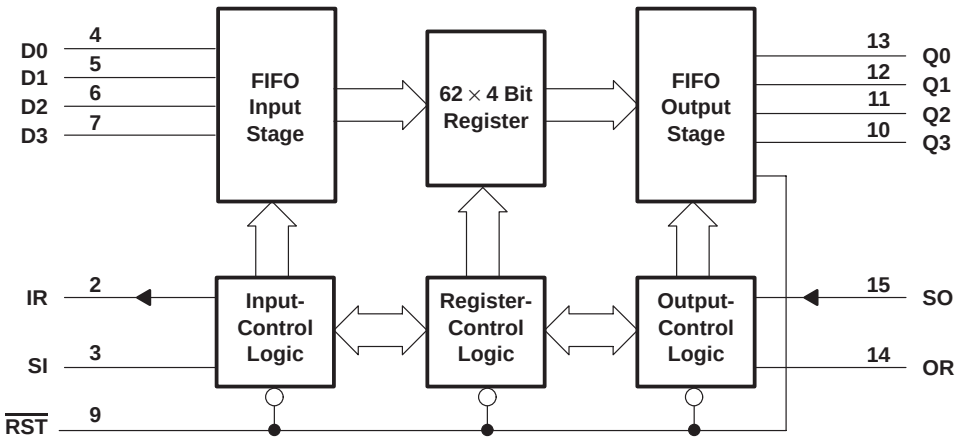
The SN74ALS236 is characterized for operation from 0°C to 70°C.

logic symbol†



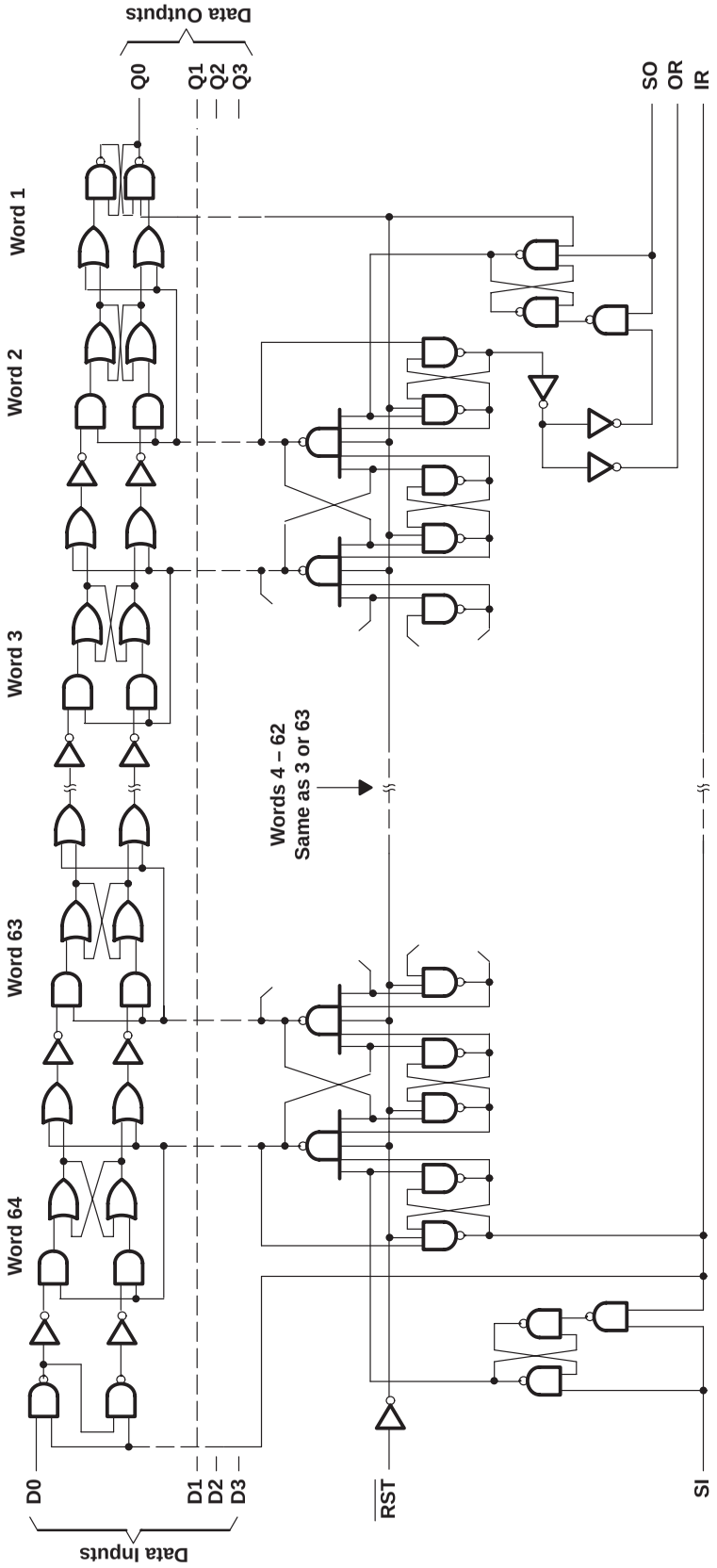
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW and N packages.

functional block diagram

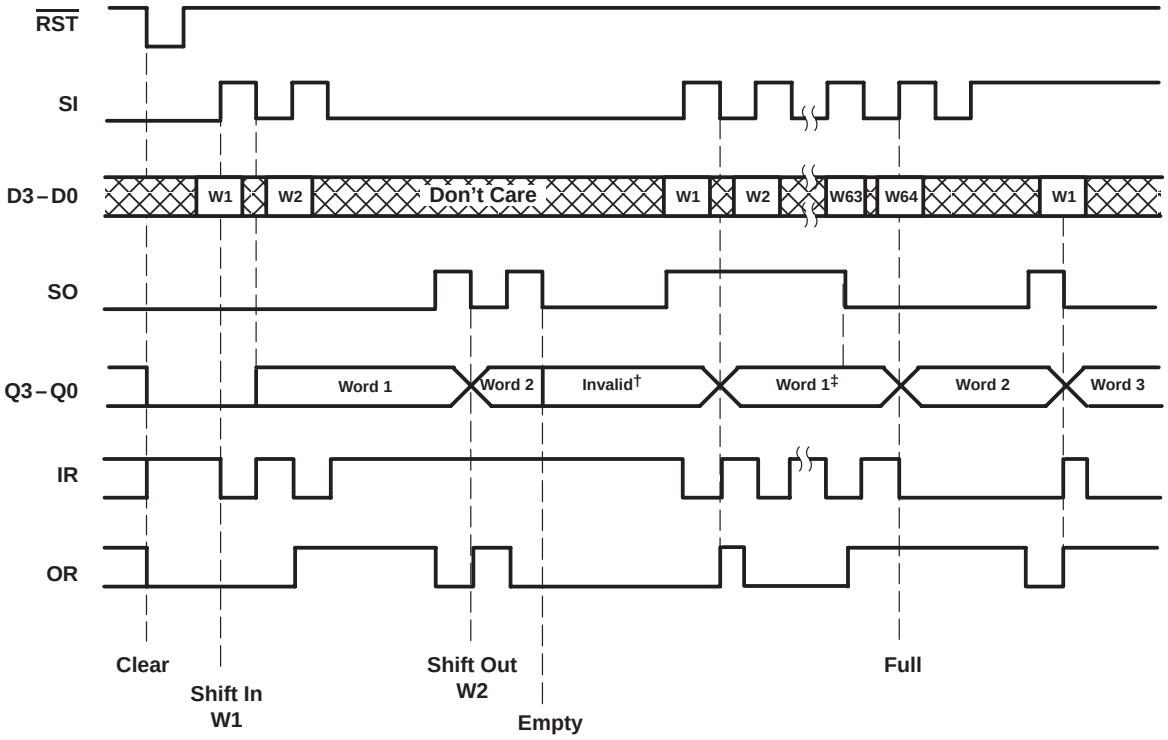


Pin numbers shown are for the DW and N packages.

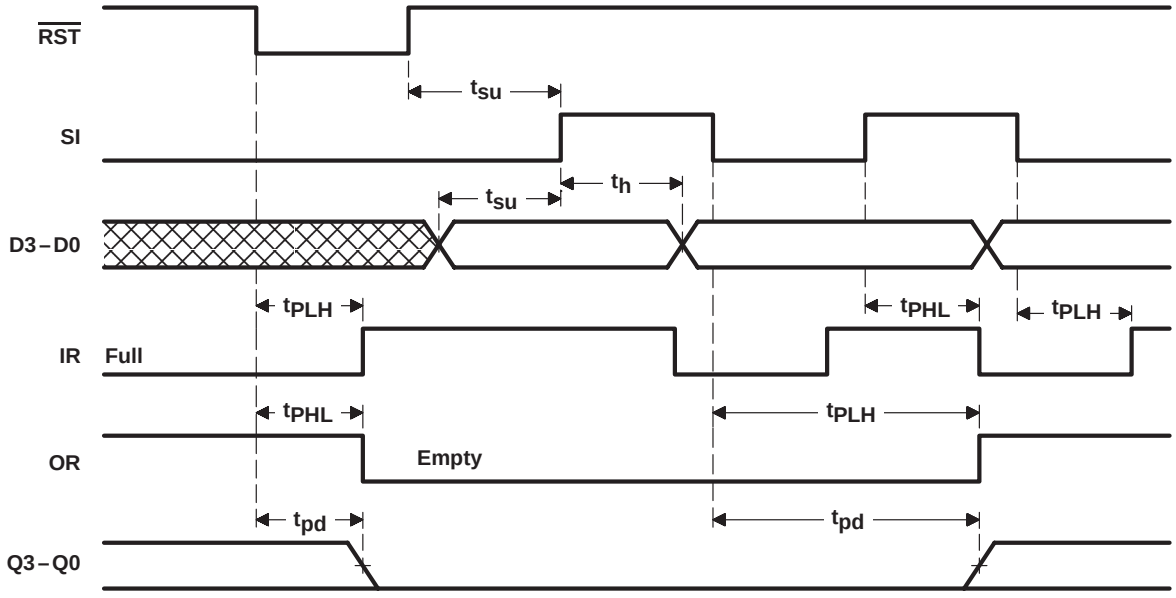
logic diagram (positive logic)



timing diagram

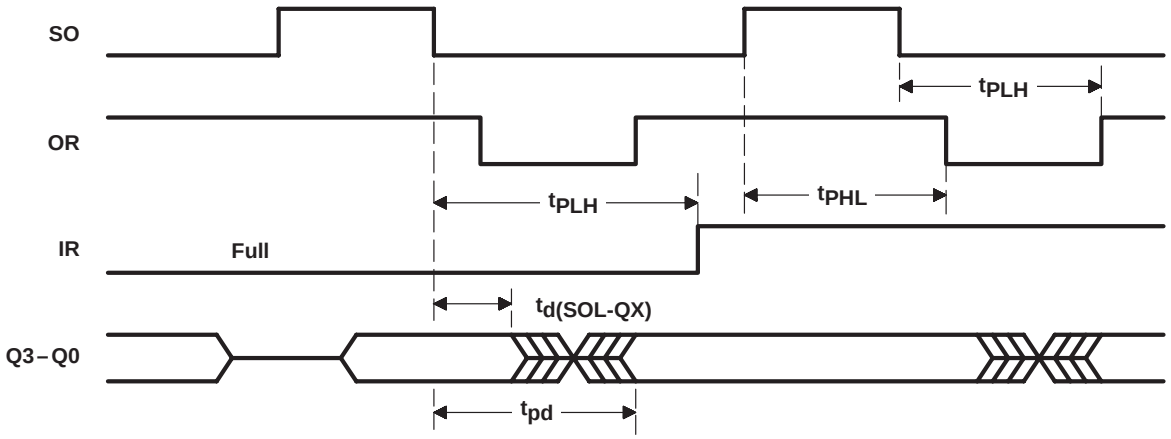


† The last data word shifted out of the FIFO remains at the output until a new word falls through or an $\overline{\text{RST}}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the outputs. Any additional words written into the FIFO stack up behind the first word and do not appear at the output until SO is taken low.



NOTE A: SO is low.

Figure 1. Master Reset and Data-In Waveforms



NOTE A: SI is low.

Figure 2. Data-Out Waveforms

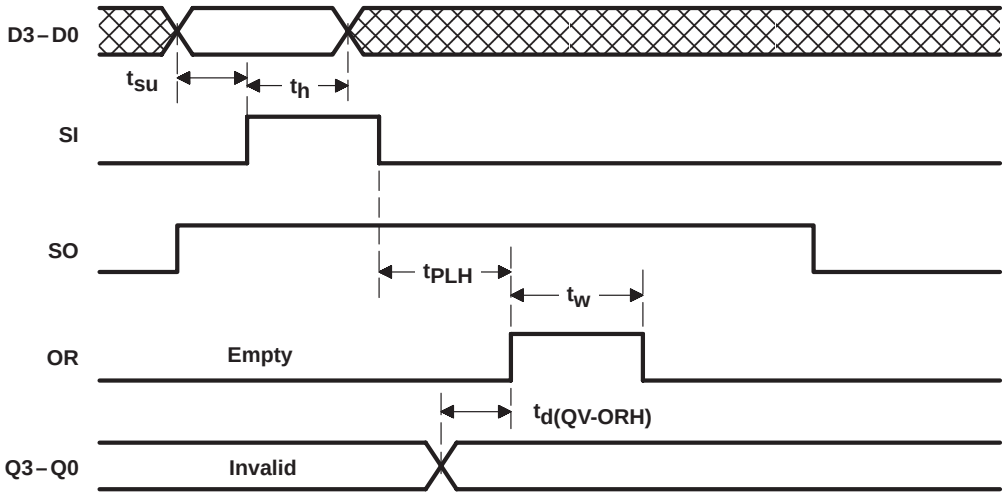


Figure 3. Data Fall-Through Waveforms

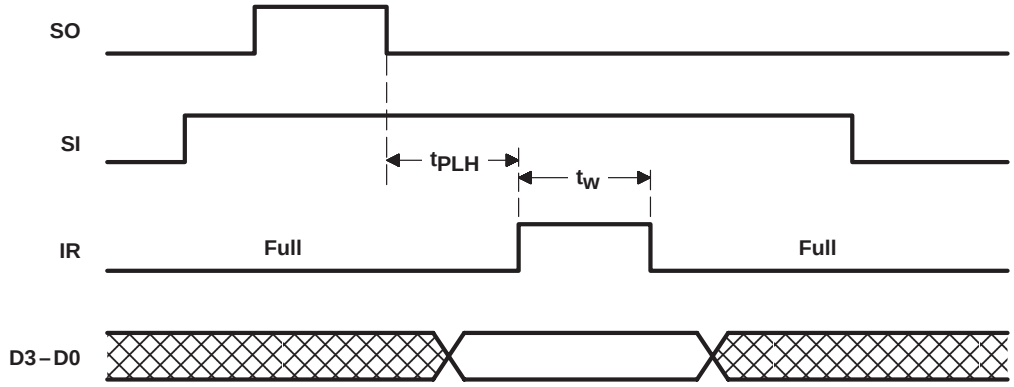


Figure 4. Automatic Data-In Waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 105°C/W
FN package . . . . . 83°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			– 2.6	mA
		IR and OR			– 0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		IR and OR			8	
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	Any Q	V_{CC} = 4.5 V	I_{OH} = –1 mA				V
			I_{OH} = –2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = –0.4 mA	2.7	3.4		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Low		100	145	mA
			High		97	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 5)

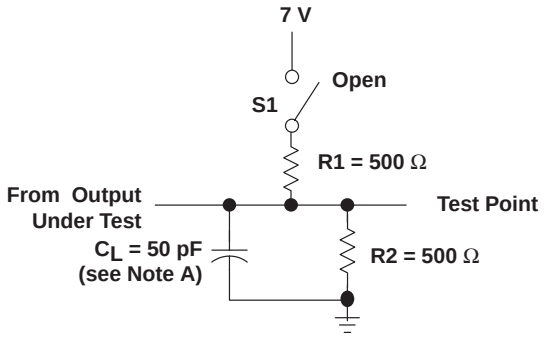
				MIN	MAX	UNIT
f_{clock}	Clock frequency	SI or SO			30	MHz
t_w	Pulse duration	SI or SO	High or low	15		ns
		$\overline{RST}$	Low	15		
t_{su}	Setup time before SI↑	Data		0		ns
		$\overline{RST}$	High (inactive)	15		
t_h	Hold time, data after SI↑			17		ns

switching characteristics (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	MIN	MAX	UNIT
f_{max}	SI			35		30		MHz
	SO			35		30		
t_w‡	IR high			15		8		ns
t_w§	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR↑			6	9	–5	12	ns
$t_{d(SOL-QX)}$	Q valid after SO↓			13		4		ns
t_{pd}	SI↓	Q		600	800	350	1000	ns
t_{PHL}	SI↑	IR		20	26	8	30	ns
t_{PLH}	SI↓			16	21	6	25	
t_{PLH}¶	SI↓	OR		600	800	350	1000	ns
t_{pd}	SO↓	Q		13	17	4	22	ns
t_{PHL}	SO↑	OR		23	27	7	33	ns
t_{PLH}	SO↓			20	24	6	30	
t_{PLH}¶	SO↓	IR		600	800	350	1000	ns
t_{PHL}	RST↓	OR		22	26	10	34	ns
t_{PLH}		IR		17	21	6	27	
t_{PHL}	RST↓	Q	14	14	17	5	19	ns

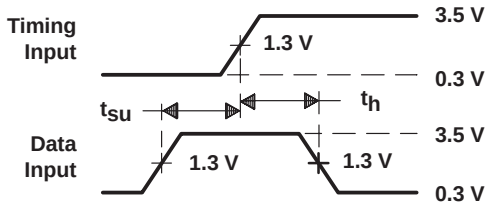
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The IR output pulse occurs when the FIFO is full, SI is high, and SO is pulsed (see Figure 4).
§ The OR output pulse occurs when the FIFO is empty, SO is high, and SI is pulsed (see Figure 3).
¶ Data throughput or fall-through times

PARAMETER MEASUREMENT INFORMATION

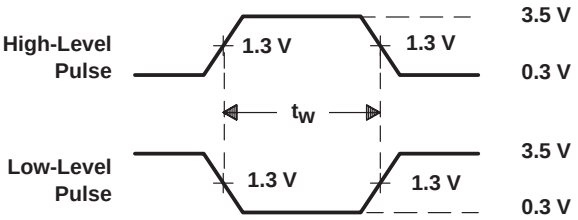


LOAD CIRCUIT FOR 3-STATE OUTPUTS

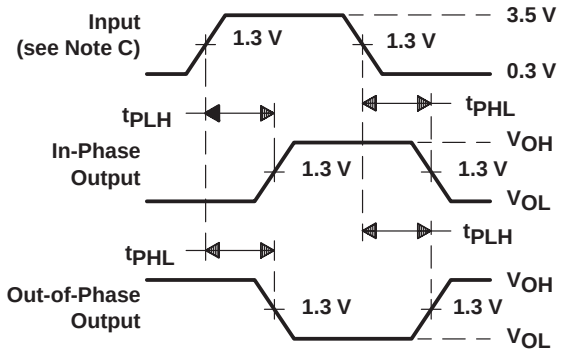
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



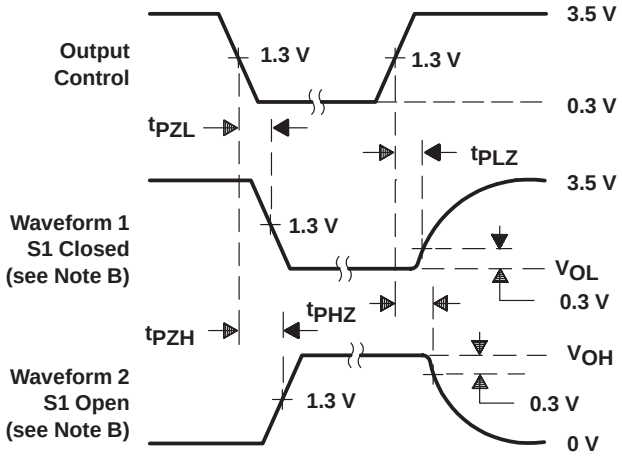
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 5. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

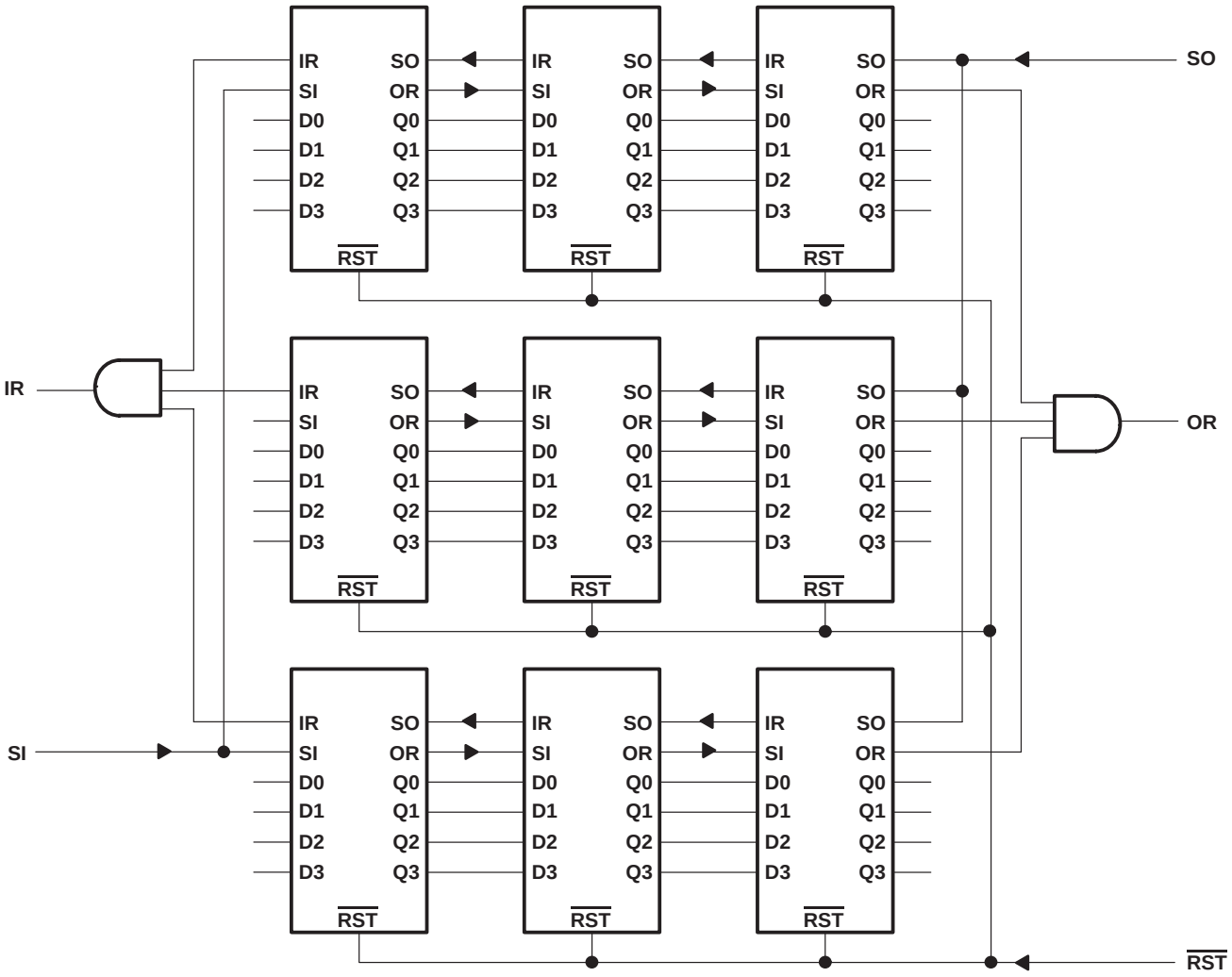


Figure 6. Word-Width Expansion: 192 × 12 Bits

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ALS236N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

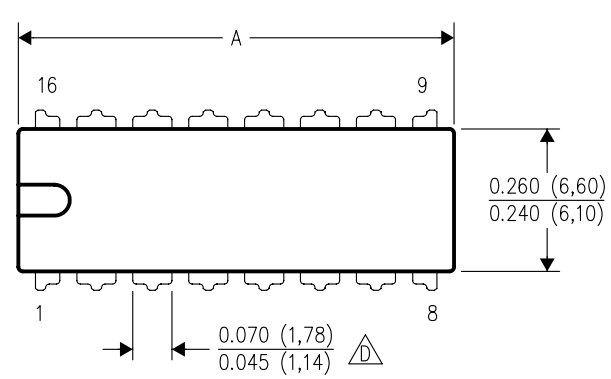
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

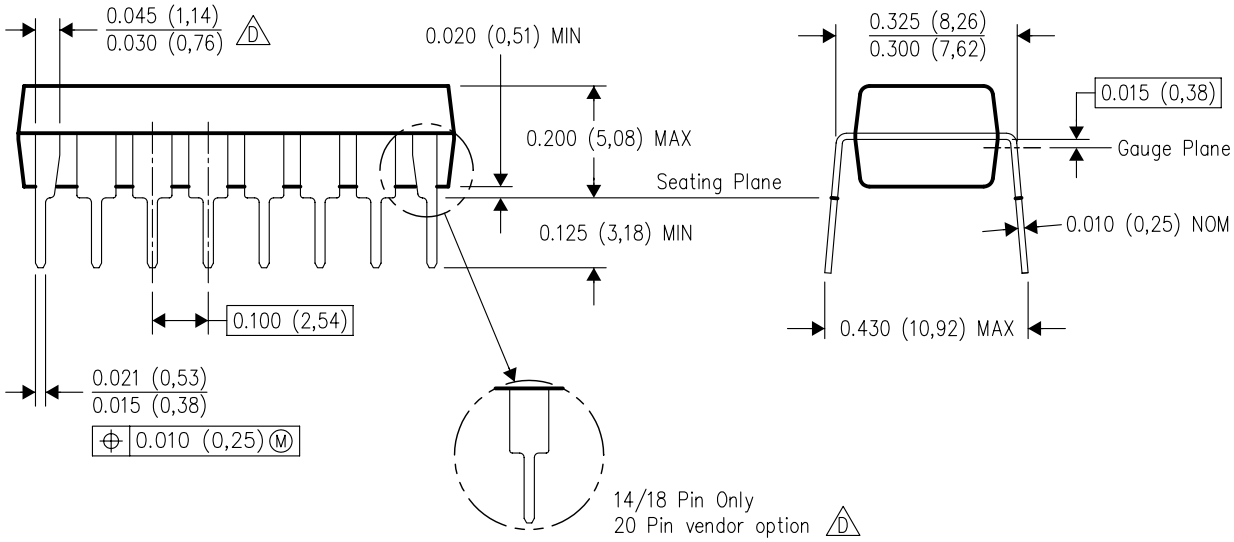
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265