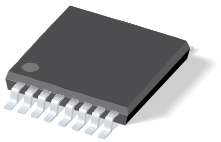


ENHANCED, LOW-INPUT VOLTAGE-MODE SYNCHRONOUS BUCK CONTROLLER

FEATURES

- **Operating Input Voltage 2.25 V to 5.5 V**
- **Output Voltage as Low as 0.7 V**
- **1% Internal 0.7 V Reference**
- **Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency**
- **Externally Adjustable Soft-Start and Overcurrent Limit**
- **Programmable Fixed-Frequency 100 KHz-to-1 MHz Voltage-Mode Control**
- **Source-Only Current or Source/Sink Current**
- **Quick Response Output Transient Comparators with Power Good Indication Provide Output Status**
- **16-Pin PowerPAD™ Package ($_{JA}$ = 2°C/W)**

APPLICATIONS

- **Networking Equipment**
- **Telecom Equipment**
- **Base Stations**
- **Servers**
- **DSP Power**

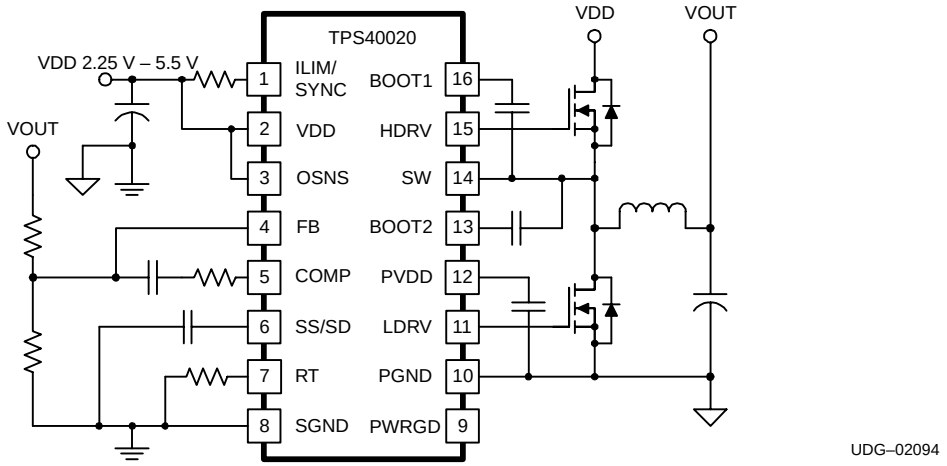
DESCRIPTION

The TPS4002x family of dc-to-dc controllers are designed for non-isolated synchronous buck regulators, providing enhanced operation and design flexability through user programmability.

The TPS4002x utilizes a proprietary Predictive Gate Drive™ technology to minimize the diode conduction losses associated with the high-side and synchronous rectifier N-channel MOSFET transistions. The integrated charge pump with boost circuit provides a regulated 5-V gate drive for both the high side and synchronous rectifier N–channel MOSFETs. The use of the Predictive Gate Drive™ technology and charge pump/boost circuits combine to provide a highly efficient, smaller and less expensive converter.

Design flexibility is provided through user programmability of such functions as: operating frequency, overcurrent detection thresholds, soft-start ramp time, and external synchronization frequency. The operating frequency is programmable using a single resistor over a frequency range of 100 kHz to 1 MHz. Higher operating frequencies yield smaller component values for a given converter power level as well as faster loop closure.

PRODUCT PREVIEW



UDG–02094

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PowerPAD™ and Predictive Gate Drive™ are trademarks of Texas Instruments.

DESCRIPTION (CONTINUED)

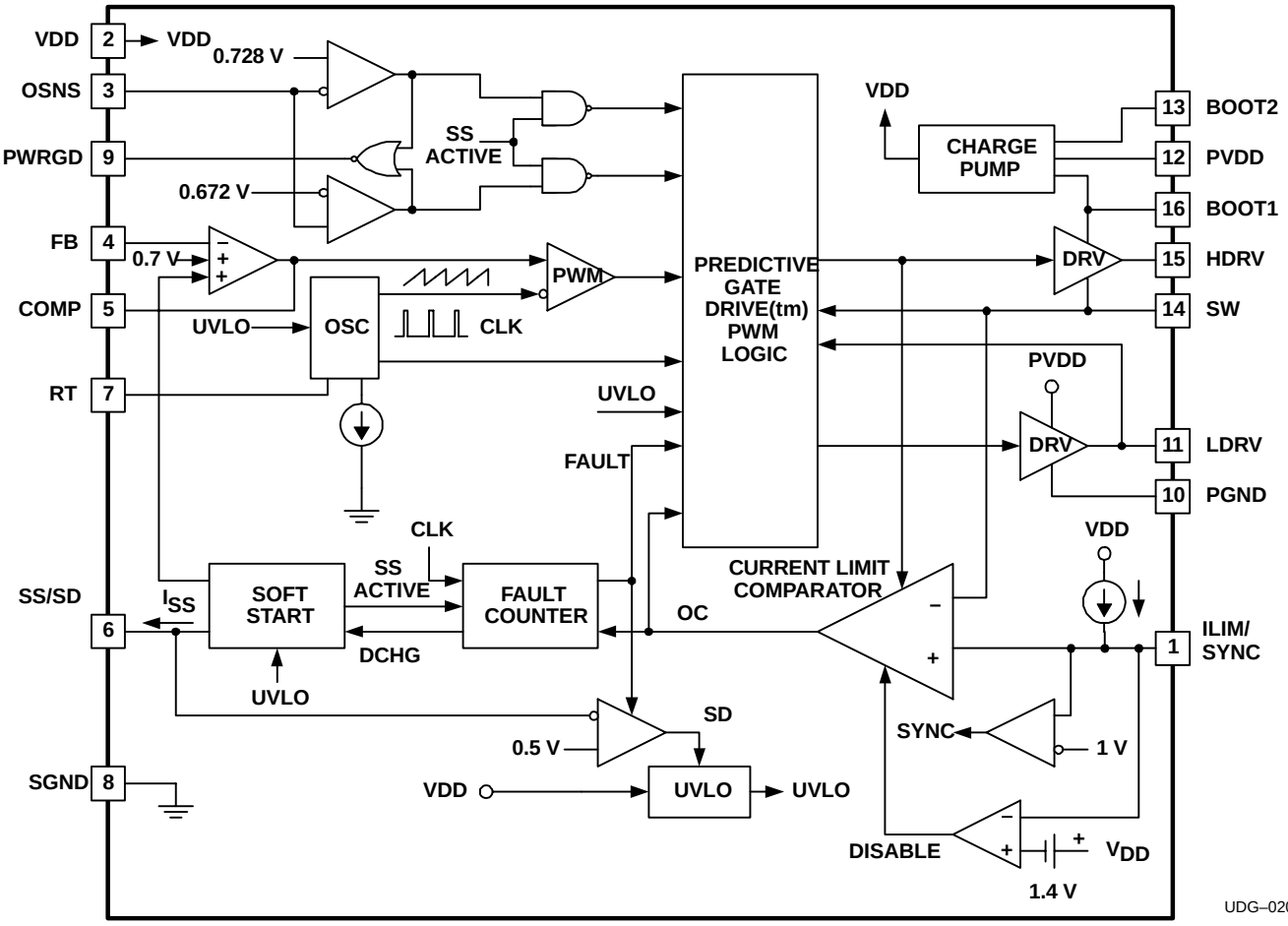
The overcurrent detection is programmable through a single resistor. Programmable overcurrent limit allows the detection threshold to be easily tailored to accommodate different size ($R_{DS(on)}$) MOSFETs. The overcurrent function provides pulse-by-pulse current limiting during soft-start and short term transient conditions as well as a fault counter to handle longer duration overcurrent conditions. If a fault is detected the controller shuts down for a period of time determined by six (6) consecutive soft-start cycles. The controller automatically retries the output every seventh (7^{th}) soft-start cycle.

In addition to determining the off time during a fault condition, the soft-start ramp provides a closed loop controlled ramp of the converter output during startup. Programmability allows the ramp rate to be adjusted for a wide variety of output L-C component values.

The output voltage transient comparators provide a quick response , first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin. If an overvoltage condition is detected the HDRV gate drive is shut-off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. In either case, the PowerGood open drain output pulls low to indicate an output voltage out of regulation condition. The PowerGood output can be daisy-chained to the SS/SD pin or enable pin of other controllers or converters. The transient comparators can be disabled by simply tying the OSNS pin to VDD.

The TPS4002X can be externally synchronized through the ILIM/SYNC pin up to 1.5× the free-running frequency. This allows multiple contollers to be synchronized to eliminate EMI concerns due to input beat frequencies between controllers.

INTERNAL BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	LOAD CURRENT	PACKAGE	PART NUMBER
–40°C to 85°C	SOURCE	Plastic HTSSOP (PWP)(1)	TPS40020PWP
	SOURCE/SINK	Plastic HTSSOP (PWP)(1)	TPS40021PWP
	SOURCE/SINK(2)	Plastic HTSSOP (PWP)(1)	TPS40022PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS40020PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

(2) Source only conduction mode (DCM) enabled during soft-start only. Source/sink during normal operation.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

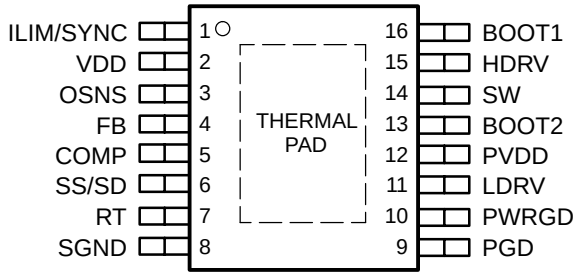
		TPS4002X	UNIT
Input voltage range, VI	SS/SD, VDD, PVDD, OSNS	–0.3 to 6	V
	BOOT2, BOOT1	–0.3 to V_{SW} + 6	
	SW	–0.3 to 10.5	
	FB, ILIM	–0.3 to 6.0	
Output voltage range, V_O	COMP, PWRGD, RT	–0.3 to 6	
Sink current, I_S	PWRGD	10	mA
Operating virtual junction temperature range, T_J		–40 to 125	°C
Storage temperature, T_{stg}		–55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	2.25		5.5	V
Operating junction temperature, T_J	–40		85	°C

PWP PACKAGE(3)(4)
(TOP VIEW)



(3) For more information on the PWP package, refer to TI Technical Brief, Literature No. SLMA002.
(4) PowerPAD™ heat slug must be connected to SGND (Pin 8), or electrically isolated from all other pins.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 85°C, T_J = T_A, V_{DD} = 5.0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{DD}	Input voltage range, VDD		2.25		5.50	V
V_{PVDD}	PVDD pin voltage	V_{DD} = 3.3 V	4.6	4.9	5.2	V
I_{DD}	Switching current	500 kHz, No load on HDRV, LDRV		3.5	5.0	mA
	Quiescent current	FB = 0.8 V		2.0	2.5	mA
	Shutdown current	SS/SD = 0 V, Outputs OFF		0.38	0.50	mA
V_{UVLO}	Minimum on-voltage		1.95	2.05	2.15	V
	Hysteresis		80	140	200	mV
OSCILLATOR						
f_{OSC}	Accuracy	2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 69.8 kΩ	425	500	575	kHz
		2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 34.8 kΩ	850	1000	1150	kHz
V_{RAMP}	Ramp voltage	V_{PEAK}–V_{VAL}	0.80	0.93	1.07	V
V_{VAL}	Ramp valley voltage		0.24	0.31	0.41	V
PWM						
d_{MAX}	Maximum duty cycle	OSNS = V_{DD}, RT = 34.8 kΩ, V_{DD} = 3.3 V, FB = 0 V	85%	94%	97%	
d_{MIN}	Minimum duty cycle				0%	
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage	–40°C ≤ T_A ≤ 0°C, 2.25 V ≤ V_{DD} ≤ 5.00 V	0.693	0.700	0.707	V
		0°C ≤ T_A ≤ 85°C, 2.25 V ≤ V_{DD} ≤ 5.00 V	0.689	0.700	0.711	V
I_{BIAS}	Input bias current			30	130	nA
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA, V_{FB} = GND	2.0	2.5		V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA, V_{FB} = V_{DD}		0.08	0.15	V
I_{OH}	High-level output source current	V_{COMP} = 0.7 V, V_{FB} = GND	3	7		mA
I_{OL}	Low-level output sink current	V_{COMP} = 0.7 V, V_{FB} = V_{DD}	3	8		mA
G_{BW}	Gain bandwidth(1)		5	10		MHz
A_{OL}	Open loop gain		55	85		dB
CURRENT LIMIT						
I_{SINK}	Current limit sink current	2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 69.8 kΩ	170	195	215	µA
V_{OS}	Current limit offset voltage		–16	0	16	mV
t_{ON}	Minimum HDRV on–time in overcurrent	V_{DD} = 3.3 V		200	300	ns
t_{ON}	Switch leading-edge blanking pulse time(1)			140		ns
t_{SS}	Soft-start cycle time			6		
V_{ILIM}	Current limit input voltage range		2		VDD	V
SOFT START						
I_{SS}	Soft-start source current	Outputs = OFF	2.0	3.7	5.4	µA
V_{SS}	Soft-start clamp voltage		1.1	1.5	1.9	V

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 85°C, $T_J = T_A$, V_{DD} = 5.0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHUTDOWN						
V_{SD}	Shutdown threshold voltage		0.09	0.13	0.18	V
V_{EN}	Device active threshold voltage		0.14	0.17	0.21	
OUTPUT DRIVER						
R_{HDHI}	High-side driver pull-up resistance	$V_{(BOOT1)} - V_{(SW)}$ = 3.3 V, I_{SOURCE} = 100mA	1.0	2.5	5.0	Ω
R_{HDLO}	High-side driver pull-down resistance	$V_{(BOOT1)} - V_{(SW)}$ = 3.3 V, I_{SINK} =100mA	0.8	1.5	3.0	
R_{LDHI}	Low-side driver pull-up resistance	P_{VDD} = 3.3 V, I_{SOURCE} =100 mA	1.0	2.5	5.0	
R_{LDLO}	Low-side driver pull-down resistance	P_{VDD} = 3.3 V, I_{SINK} =100 mA	0.5	0.8	1.5	
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 1 nF		15	35	ns
t_{LFALL}	Low-side driver fall time			10	25	
t_{HRISE}	High-side driver rise time			15	35	
t_{HFALL}	High-side driver fall time			10	25	
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(1)			165		°C
	Hysteresis(1)			15		
CHARGE PUMP						
R_{VB2}	$R_{DS(on)}$ VDD to BOOT2	V_{DD} = 5.0 V, I_{SOURCE} =10 mA	3.8	7.6	11.4	Ω
R_{B2P}	$R_{DS(on)}$ BOOT2 to PVDD	V_{DD} = 5.0 V, I_{SOURCE} =10 mA	2.8	5.6	8.4	
R_{PB1}	$R_{DS(on)}$ PVDD to BOOT1	V_{DD} = 5.0 V, I_{SOURCE} =10 mA	2.9	5.9	8.9	
POWER GOOD						
V_{PGD}	Pull-down voltage	V_{OSNS} = 0.8 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V	60	90	150	mV
t_{ONHPL}	Output sense high to power good low delay time	0.7 V ≤ V_{OSNS} ≤ 0.8 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V	6	10	14	µs
t_{ONLPL}	Output sense low to power good low delay time	0.6 V ≤ V_{OSNS} ≤ 0.7 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V	6	10	14	
t_{SDHPH}	Shutdown high to power good high delay time	V_{OSNS} = 0.7 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V, 0.0 V ≤ V_{SS_SDB} ≤ 0.4 V	2	4	6	
t_{SDLPL}	Shutdown low to power good low delay time	V_{OSNS} = 0.7 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V, 0.0 V ≤ V_{SS_SDB} ≤ 0.4 V	0.5	1.5	2.0	
t_{ONHPH}	Output sense high (N) to power good high delay time	0.7 V ≤ V_{OSNS} ≤ 0.8 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V	140	500	1000	ns
t_{ONLPH}	Output sense low (N) to power good high delay time	0.6 V ≤ V_{OSNS} ≤ 0.7 V, I_{PWRGD} =0.5 mA, V_{DD} = 3.3 V	140	500	1000	
TRANSIENT COMPARATORS						
V_{OV}	Overvoltage output threshold voltage	Referenced to V_{FB}	25	29	37	mV
	Hysteresis		8	15	22	
V_{UV}	Undervoltage output threshold voltage		–37	–31	–25	
	Hysteresis		8	15	22	
V_{DIS}	OSNS minimum disable voltage	Referenced to V_{DD}	0.5			V

(1) Ensured by design. Not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 85°C, T_J = T_A, V_{DD} = 5.0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONIZATION							
V_{ENSY}	Synchronization enable low threshold voltage					0.7	V
V_{BLNK}	Synchronization current limit enable threshold voltage		Referenced to VDD	–0.7			V
t_{MIN}	Minimum synchronization input pulse width			50	35		ns
PREDICTIVE DELAY							
V_{SWP}	Sense voltage to modulate delay time				–350		mV
t_{LDHD}	Maximum delay modulation		LDRV OFF-to-HDRV ON	40	65	90	ns
	Counter delay/bit time		LDRV OFF-to-HDRV ON	3.0	4.5	6.2	
t_{HDLD}	Maximum delay modulation		HDRV OFF-to-LDRV ON	35	60	85	
	Counter delay/bit time		HDRV OFF-to-LDRV ON	2.4	4.0	5.6	
RECTIFIER ZERO CURRENT COMPARATOR							
V_{SW}	Sense voltage to turn off rectifier MOSFET	TPS40020 TPS40022	LDRV output = OFF	–5	–2.5	2	mV
t_{ZBLNK}	Zero current blanking time(1)				150		ns

(1) Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOT1	16	I	This pin provides a bootstrapped supply for the high side FET driver, enabling the gate of the high side FET to be driven above the input supply rail. Connect a capacitor from this pin to the SW pin.
BOOT2	13	I	This pin provides a secondary bootstrapping necessary for generation of PVDD. Connect a capacitor from this pin to SW.
COMP	5	O	Output of the error amplifier. Refer to *Electrical Characteristics* table for loading constraints.
FB	4	I	Inverting input of the error amplifier. In normal operation, V_{FB} is equal to the internal reference level of 700 mV.
HDRV	15	O	The gate drive output for the high side N-channel MOSFET switch is bootstrapped to near PVDD for good enhancement of the high-side switch. The HDRV switches from BOOT1 to SW.
ILIM/SYNC	1	I	The current limit pin is used to set the current limit threshold. A current sink from this pin to GND sets the threshold voltage for overcurrent across a resistor connected to VDD. Synchronization is accomplished by pulling IMAX to less than 1 V for a period greater than the minimum pulse width and then releasing. An open collector or drain device should be used. These pulses must be of higher frequency than the free running frequency of the local oscillator.
LDRV	11	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET. LDRV switches from PVDD to PGND.
OSNS	3	O	The output sense pin is connected to a resistor divider from VOUT to GND (identical to the main feedback loop) and is used to sense power good condition and provides reference for the transient comparators.
PGND	9	O	Power (high-current) ground used by LDRV.
PWRGD	10	–	Power good. This is an open-drain output which connects to the supply via an external resistor.
PVDD	12	O	This pin is the regulated output of the charge-pump and provides the supply voltage for the LDRV driver stage. PVDD also drives the bootstrap circuit which generates the voltage on BOOT1.
RT	7	I	External pin for programming the oscillator frequency.
SGND	8	–	Signal ground
SS/SD	6	I	The soft-start/shutdown pin provides user programmable soft-start timing and shutdown capability for the controller.
SW	14	I	This pin, used for overcurrent, zero-current, and in the anti-cross conduction sensing is connected to the switched node on the converter. Overcurrent is detected by sensing the voltage at this pin with respect to VDD while the high-side switch is on. Zero current is detected by sensing the pin voltage with respect to ground when the low-side rectifier MOSFET is on.
VDD	2	I	Power input for the device. Maximum voltage is 5.5 V. De-coupling of this pin is required.

APPLICATION INFORMATION

The TPS4002X series of devices are low-input voltage, synchronous, voltage mode-buck controllers. A typical application circuit is shown in Figure 1. These controllers are designed to allow construction of high-performance dc-to-dc converters with input voltages from 2.25 V to 5.5 V, and output voltages as low as 700 mV. Using a top side N-channel MOSFET for the primary buck switch results in lower switch resistance for a given gate charge.

The device controls the delays from main switch off to rectifier turn on and from rectifier turn off to main switch turn on in a way that minimizes diode losses (both conduction and recovery) in the synchronous rectifier. The reduction in these losses is significant and can mean that for a given converter power level, smaller FETs can be used, or that heat sinking can be reduced or even eliminated.

The controller provides for a coarse current-limit function that provides pulse-by-pulse current limiting, as well as integrates overcurrent pulses to determine the existence of a persistant fault state at the converter output. If a fault is detected, the converter shuts down for a period of time (determined by six soft-start cycles) and then restarts. The current-limit threshold is adjustable with a single resistor connected from VDD to the ILIM/SYNC pin. This overcurrent function is designed to protect against catastrophic faults only, and cannot be guaranteed to protect against all overcurrent conditions.

The controller implements a closed-loop soft start function. Startup ramp time is set by a single external capacitor connected to the SS pin. The SS pin also doubles as a shutdown function.

VOLTAGE REFERENCE

The bandgap cell is designed with a trimmed, curvature corrected (< 1%) 0.700-V output, allowing output voltages as low as 700 mV to be obtained.

Oscillator

The ramp waveform is a saw-tooth form at the PWM frequency with a peak voltage of 1.25 V, and a valley of 0.3 V. The PWM duty cycle is limited to a maximum of 97%, allowing the bootstrap and charge pump capacitors to charge during every cycle.

Bootstrap/Charge Pump

The TPS4002X series includes a charge pump to boost the drive voltage to the power MOSFET's to higher levels when the input supply is low. A capacitor connected from PVDD to PGND is the storage cap for the pump. A capacitor connected from SW to BOOT2 gets charged every switching cycle while SW is low and its charge is dumped on the PVDD capacitor when SW goes high. An internal switch disables the charge pump when the voltage on PVDD reaches approximately 4.8 V and enables pumping when PVDD falls to approximately 4.6 V. The high-side driver uses the capacitor from SW to BOOT1 as its power supply. When SW is low, this capacitor charges from the PVDD capacitor. When the SW pin goes high, this capacitor provides above-rail drive for the high-side N-channel FET.

Drivers

The HDRV and LDRV MOSFET drivers are capable of driving gate-to-source voltages up to 5.0 V. At 5 V V_{IN}, and using appropriate MOSFETs, a 20-A converter can be achieved. The LDRV driver switches between VDD and ground, while the HDRV driver is referenced to SW and switches between BOOT1 and SW. The maximum voltage between BOOT1 and SW is 5.0 V.

APPLICATION INFORMATION

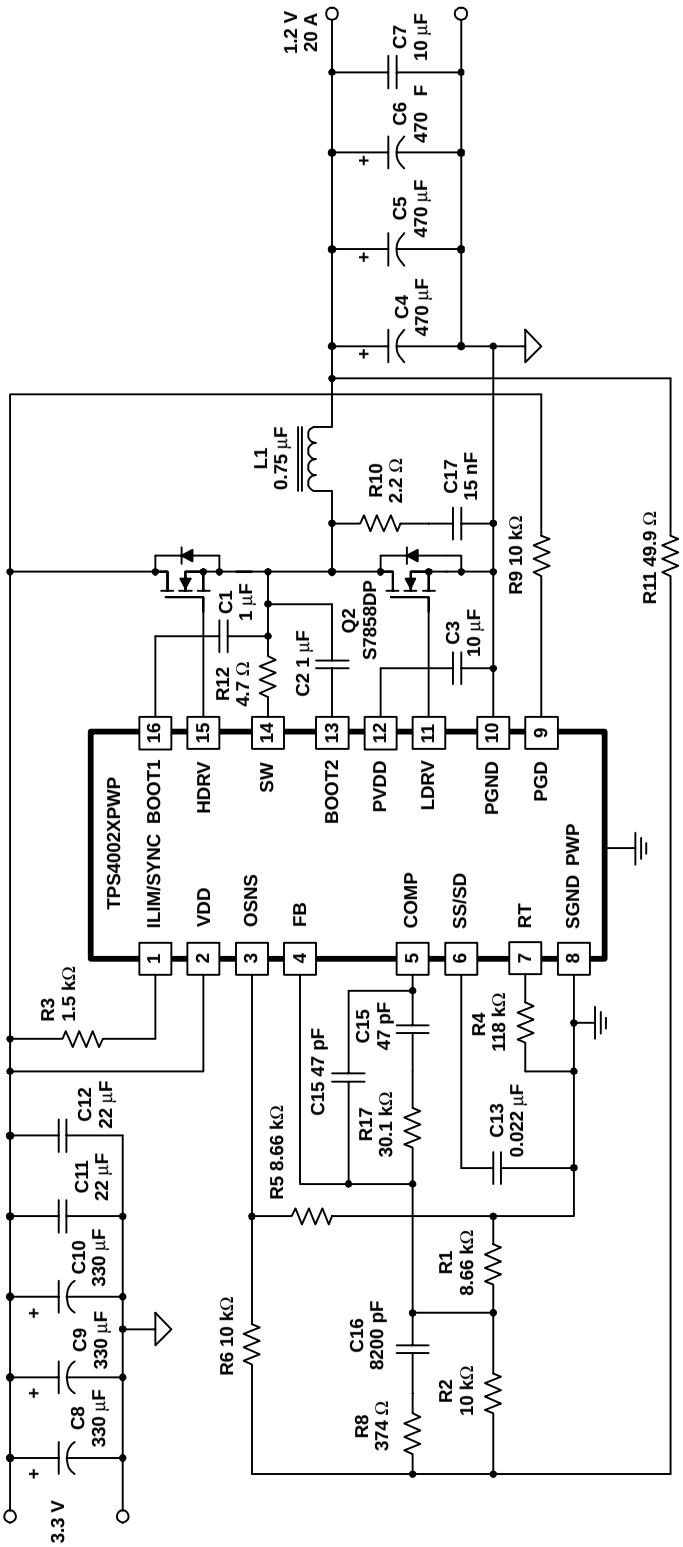


Figure 1. Typical Application

APPLICATION INFORMATION

Synchronous Rectification and Predictive Delay

In a normal buck converter, when the main switch turns off, current is flowing to the load in the inductor. This current cannot be stopped immediately without using infinite voltage. To give this current a path to flow and maintain voltage levels at a safe level, a rectifier or catch device is used. This device can be either a plain diode, or it can be a controlled active device if a control signal is available to drive it. The TPS4002X provides a signal to drive an N–channel MOSFET as a rectifier. This control signal is carefully coordinated with the drive signal for the main switch so that there is absolute minimum dead time from the time that the rectifier FET turns off and the main switch turns on, and minimum delay from when the main switch turns off and the rectifier FET turns on. This TI–patented function, predictive delay, uses information from the current switching cycle to adjust the delays that are used for the next cycle. Figure 1 shows the switch-node voltage waveform for a synchronously rectified buck converter. Illustrated are the relative effects of a fixed delay drive scheme (constant, pre-set delays for the turnoff to turn on intervals), an adaptive delay drive scheme (variable delays based upon voltages sensed on the current switching cycle) and the predictive delay drive scheme. Note that the longer the time spent in diode conduction during the rectifier conduction period, the lower the efficiency. Also, not shown in the figure, is the fact that the predictive delay circuit can actually prevent the body diode from becoming forward biased at all while at the same time avoiding cross conduction or shoot through. This results in a significant power savings when the main FET turns on. There is no reverse recovery loss in the body diode of the rectifier FET.

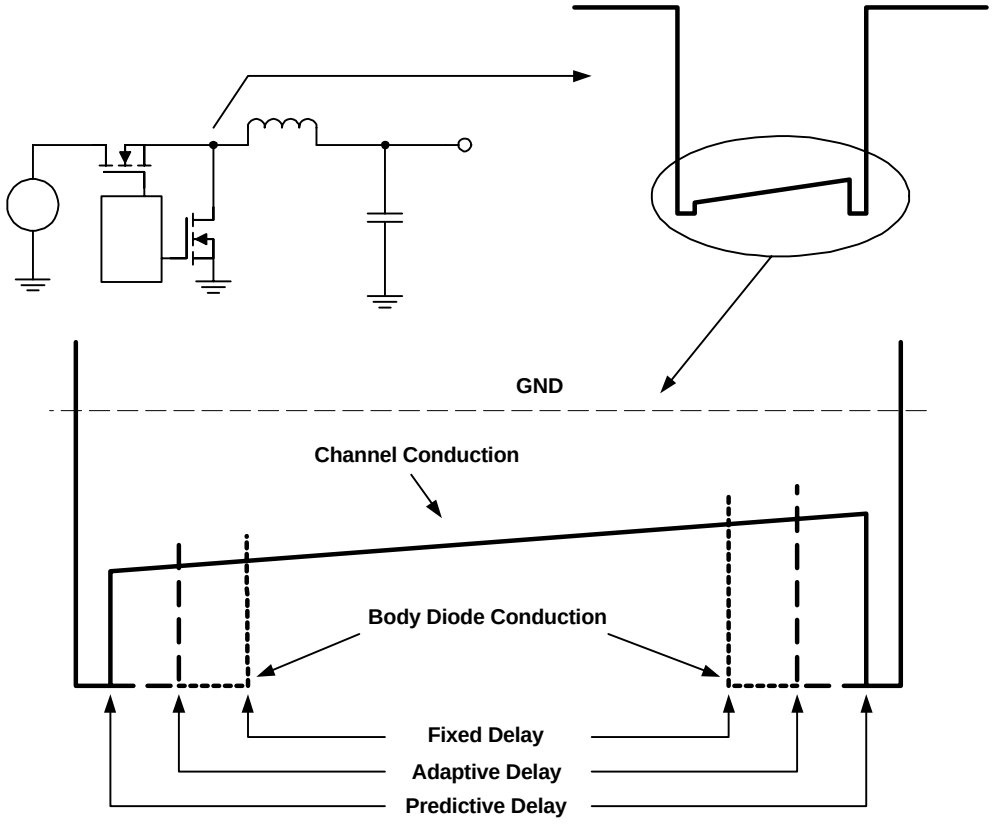


Figure 2. Switch Node Waveforms for Synchronous Buck Converter

APPLICATION INFORMATION

Overcurrent

Overcurrent in the TPS4002X is sensed by looking at the voltage across the main FET while it is on. If the voltage exceeds a pre-set threshold, the current pulse is terminated, and a counter inside the device is incremented. If this counter fills up, a fault condition is declared and the chip disables switching for a period of time and then attempts to restart the converter with a full soft-start cycle. The more detailed explanation follows.

In each switching cycle, a comparator looks at the voltage across the top side FET while it is on. If the voltage across that FET exceeds a programmable threshold voltage, then the current switching pulse is terminated and a 3-bit counter (eight counts) is incremented by one count. If during the switching cycle the top side FET voltage does not exceed a preset threshold, then this counter is decremented by one count. (The counter does not wrap around from seven to zero or from zero to seven). If the counter reaches a full count of seven, the device declares that a fault condition exists at the output of the converter. In this state, switching stops and the soft-start capacitor is discharged. The counter is decremented by one by the soft start cap discharge. When the soft-start capacitor is fully discharged, the discharge circuit is turned off and the cap is allowed to charge up at the nominal charging rate, When the soft-start capacitor reaches about 700 mV, it is discharged again and the overcurrent counter is decremented by one count. The capacitor is charged and discharged, and the counter decremented until the count reaches zero (a total of six times). When this happens, the outputs are again enabled as the soft-start capacitor generates a reference ramp for the converter to follow while attempting to restart. During this soft-start interval (whether or not the controller is attempting to do a fault recovery or starting for the first time), pulse-by-pulse current limiting is in effect, but overcurrent pulses are not counted to declare a fault until the soft-start cycle has been completed. It is possible to have a supply try to bring up a short circuit for the duration of the soft start period plus seven switching cycles. Power stage designs should take this into account if it makes a difference thermally. Figure 3 shows the details of the overcurrent operation.

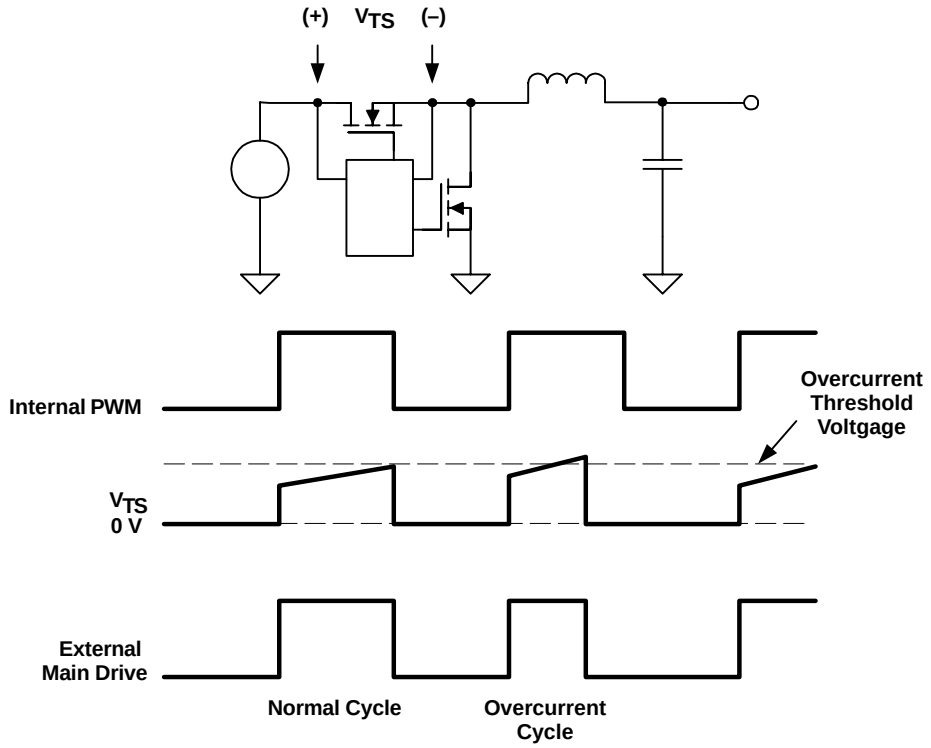


Figure 3. Switch Node Waveforms for Synchronous Buck Converter

APPLICATION INFORMATION

Figure 4 shows the behavior of key signals during initial startup, during a fault and a successfully fault recovery. At time t0, power is applied to the converter. The voltage on the soft-start capacitor (V_{CSS}) begins to ramp up and acts as the reference until it passes the internal reference voltage plus about one diode drop – t1. At this point the soft-start period is over and the converter is regulating its output at the desired voltage level. From t0 to t1, pulse-by-pulse current limiting was in effect, and from t1 onward, overcurrent pulses are counted for purposes of determining if a fault exists. At t2, a heavy overload is applied to the converter. This overload is in excess of the overcurrent threshold, the converter starts limiting current and the output voltage falls to some level depending on the overload applied. During the period from t2 to t3, the counter is counting overcurrent pulses and at time t3 reaches a full count of 7. The soft-start capacitor is then discharged, the outputs are disabled, the counter decremented, and a fault condition is declared.

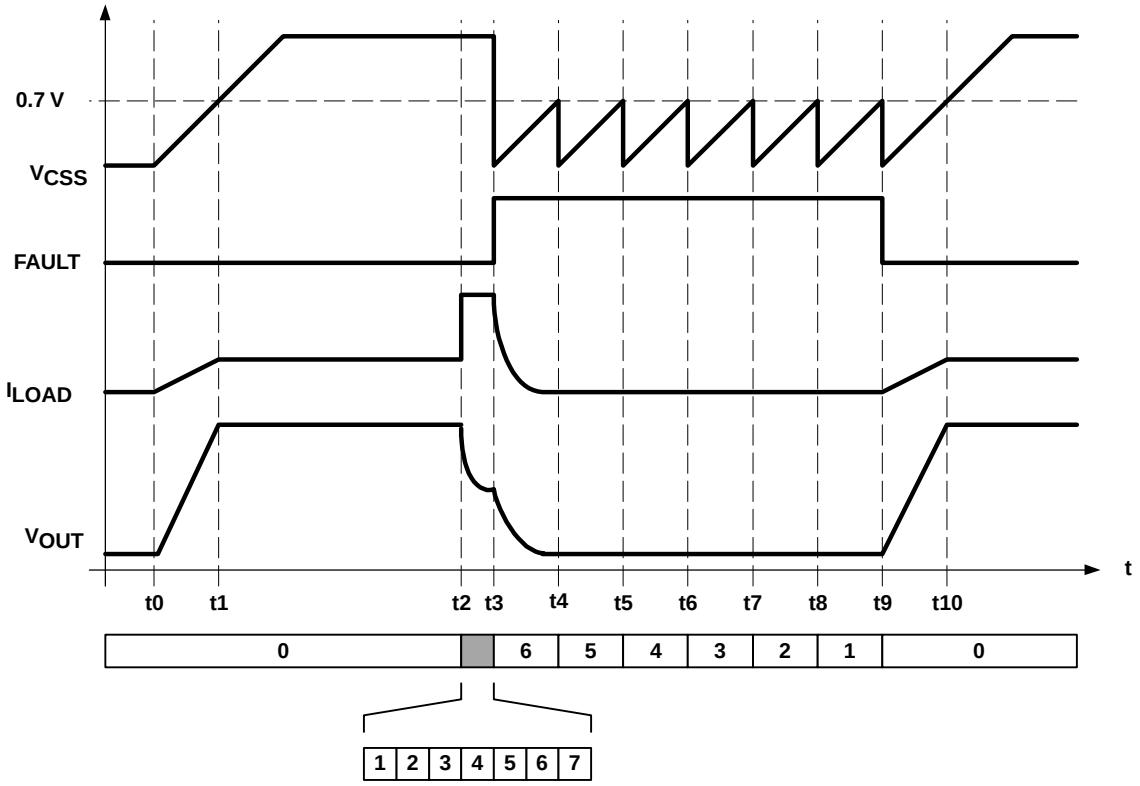


Figure 4. Overcurrent/Fault Waveforms

When the soft-start capacitor is fully discharged, it begins charging again at the same rate that it does on startup, with a nominal 3-µA current source. As the capacitor voltage reaches full charge, it is discharged again and the counter is decremented by one count. These transitions occur at t3 through t9. At t9, the counter has been decremented to zero. Now the fault logic is cleared, the outputs are enabled and the converter attempts to restart with a full soft-start cycle. The converter comes into regulation at t10.

Setting the Current Limit

Connecting a resistor from VDD to ILIM sets the current limit. A current sink in the chip causes a voltage drop across the resistor connected to ILIM. This voltage drop is the overcurrent threshold for the part. The current that the ILIM pin sinks is dependent on the value of the resistor connected to RT and is given by:

$$I_{ILIM} = 19.0 \times \frac{0.7\ V}{R_T} \quad (1)$$

The tolerance of the current sink is too loose to do an accurate current limit. The main purpose is for hard fault protection of the power switches. Given the tolerance of the ILIM sink current, and the $R_{DS(on)}$ range for a MOSFET, it is generally possible to apply a load that thermally damages the converter. This device is intended for embedded converters where load characteristics are defined and can be controlled.

APPLICATION INFORMATION

Soft-Start and Shutdown

The soft-start and shutdown functions are common to the SS/SD pin. The voltage at this pin is the controlling voltage sent to the error amplifier during startup. This reduces the transient current required to charge the output capacitor at startup, and allows for a smooth startup with no overshoot of the output voltage. A shutdown feature can be implemented as shown in Figure 5.

Switching Frequency

The switching frequency is programmed by a resistor from RT to SGND. Nominal switching frequency can by calculated by:

$$R_T = \frac{37.736}{f_{OSC}(kHz)} - 5.09\ (k\Omega) \quad (2)$$

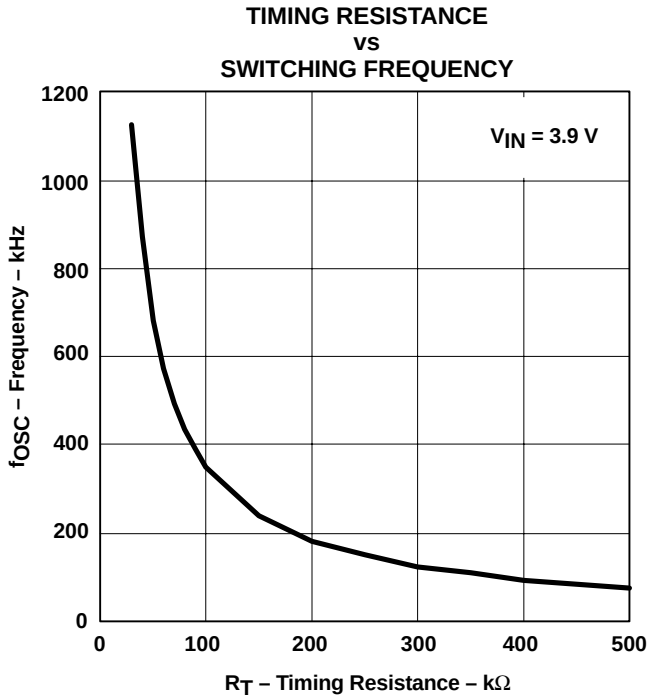


Figure 5.

APPLICATION INFORMATION

Synchronization

The TPS4002x can be synchronized to an external reference frequency higher than the free running oscillator frequency. The recommended method is to use a diode and a push pull drive signal as shown in Figure 5.

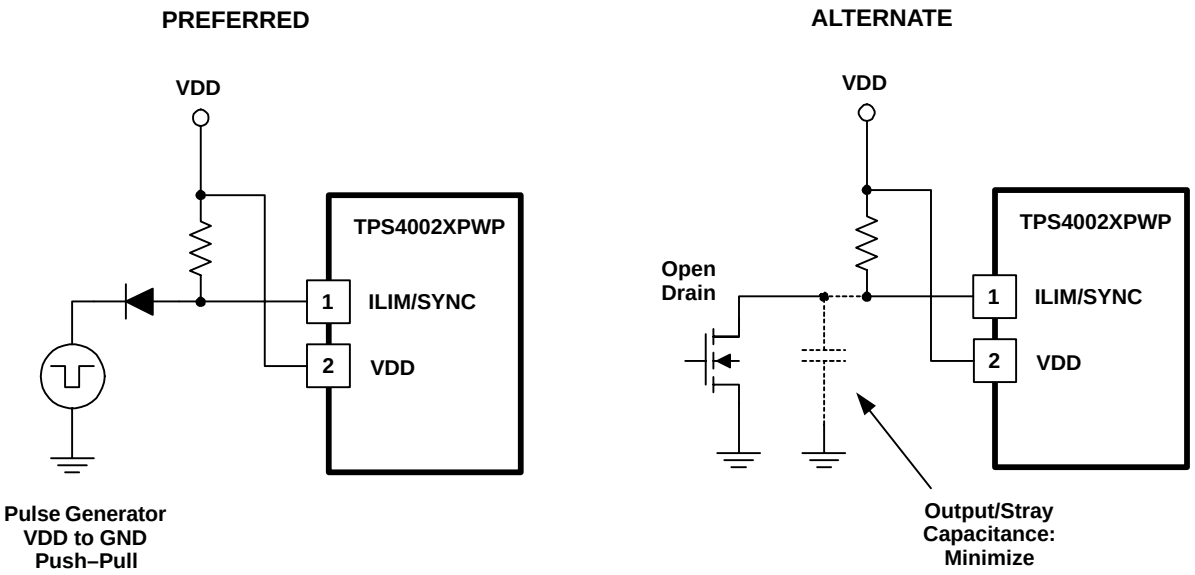


Figure 6. Synchronization Methods

This design allows synchronization up to the maximum operating frequency of 1 MHz. For best results the nominal operating frequency of a converter that is to be synchronized should be kept as close as practicable to the synchronization frequency to avoid excessive noise induced pulse width jitter. A good target is to shoot for the free run frequency to be 80% of the synchronized frequency. This ensures that the synchronization source is the frequency determining element in the system and not to adversely affect noise immunity.

Other methods of implementing the synchronization function include using an open collector or open drain output device directly, or discreet devices to pull the ILIM/SYNC pin down. These do work but performance can suffer at high frequency because the ILIM/SYNC pin must rise to (V_{DD} – 1.0 V) before the next switching cycle begins. Any time that this requires is directly subtracted from the maximum pulse width available and should be considered when choosing devices to drive ILIM/SYNC. Consequently, the lowest output capacitance devices work best.

During a synchronization cycle, the current sink on the ILIM/SYNC pin becomes disabled when ILIM/SYNC is pulled below 1.0 V. The ILIM/SYNC current sink remains disabled until ILIM/SYNC reaches (V_{DD} –1.0 V) This removes the load on the ILIM/SYNC pin to allow the voltage to slew rapidly depending on the ILIM resistor and any stray capacitance on the pin.

APPLICATION INFORMATION

Transient Comparators and Power Good

The TPS4002x makes use of a separate pin, OSNS, to monitor output voltage for these two functions. In normal operation, OSNS is connected to the output of a voltage divider at the output. It is important to make this divider the same ratio as the divider for the feedback network so that in normal operation the voltage at OSNS is the same as the voltage at FB, 0.7 V nominal.

The PWRGD pin is an open drain output that is pulled low when the device senses that power is NOT good. PWRGD is released only when the voltage at OSNS falls within 0.7 V ±4.5% (approximately). If this condition is not met, PWRGD is then pulled low. A delay has been purposely built into the PWRGD pin pulling low in response to an out of band voltage on OSNS. This is to minimize the need for filtering the signal in the event of a noise glitch causing a brief out of band OSNS voltage. The PWRGD signal goes high when the OSNS signal returns to approximately ±1% of nominal (0.7 V ±1%).

The transient comparators provide an improvement in load transient recovery time if used properly. In some situations, recovery time may be one half of the time required without transient comparators. Keep in mind that the transient comparator concept is a double-edged sword. While they provide improved transient recovery time, they can also lead to instability if incorrectly applied. For proper functionality, the first thing to do is design a feedback loop for the converter that places the open loop unity gain frequency higher than the resonant frequency of the output L-C filter. If not, the feedback loop cannot respond to the ring of the L-C on a transient event. The ring is likely to be large enough to disturb the transient comparators and the result is a power oscillator. Another helpful action is to ground the feedback loop divider and the OSNS divider at the SGND pin. Make sure both dividers measure the same physical location on the output bus. These help avoid problems with resistive drops at higher loads causing problems.

Connecting OSNS to VDD disables the transient comparators. This also disables the PWRGD function. Alternatively, OSNS and FB can be tied together. This connection allows a proper PWRGD at startup, though transient performance of the PWRGD signal diminishes.

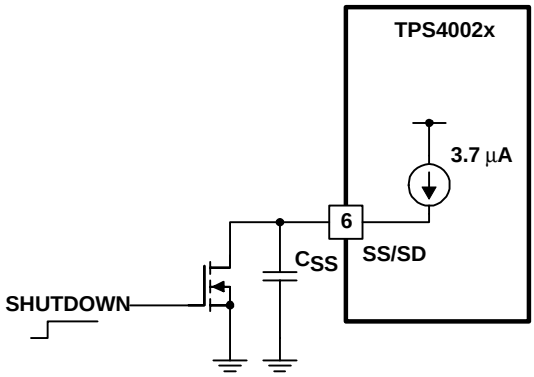


Figure 7. Shutdown Implementation

APPLICATION INFORMATION

PowerPAD™ Package

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package the area is 5 mm x 3.4 mm [3].

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to *PowerPAD Thermally Enhanced Package*[3] for more information on the PowerPAD package.

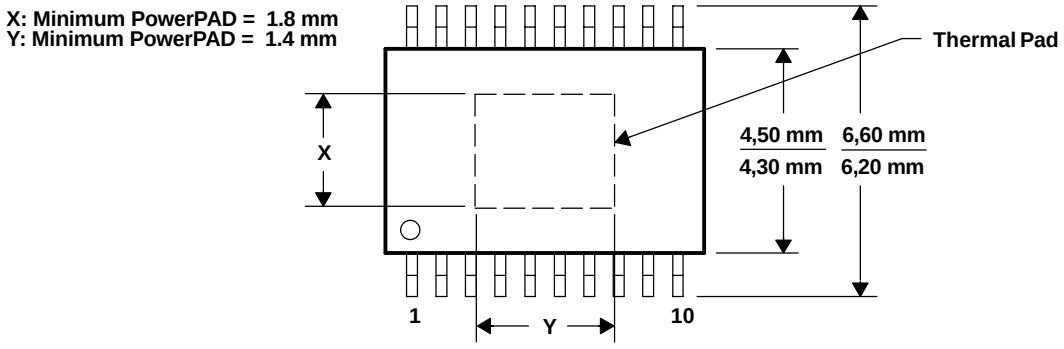


Figure 8. PowerPAD Dimensions

REFERENCE DESIGN

This design used the TPS40020 PWM controller to facilitate a step-down application from 3.3-V to 1.5 V. (see Figure 6) Design specifications include:

- Input voltage: $2.5\ V \le V_{IN} \le 5.0\ V$
- Nominal voltage: 3.3 V
- Output voltage V_{OUT}: 1.5 V
- Output current I_{OUT}: 20 A
- Switching frequency: 300 kHz

DESIGN PROCEDURE

Setting the Frequency

Choosing the optimum switching frequency is complicated. The higher the frequency, the smaller the inductance and capacitance needed, so the smaller the size, but then the the switching losses are higher, the efficiency is poorer. For this evaluation module, 300 kHz is chosen for reasonable efficiency and size.

A resistor R4, which is connected from pin 7 to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (3)

$$f_{OSC}\ (\text{MHz}) = \frac{35.4}{\text{R4}\ (\text{k}\Omega)} \approx 118\ \text{k}\Omega \tag{3}$$

Therefore, a 118-kΩ resistor is chosen for 300 kHz operation.

Inductance Value

The inductance value can be calculated by equation (2).

$$L_{(min)} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \tag{4}$$

where I_{RIPPLE} is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses.

Based on 20% ripple current and 300 kHz, the inductance value is calculated to 0.76 µH and a 0.75-µH inductor (part number is CDEP149–0R7) is chosen. The ESR of this inductor is 1.1 mΩ and the loss is 440 mW, which is approximately 1.5% of output power.

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \tag{5}$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \tag{6}$$

With 1% output voltage ripple, the needed capacitance is at least 114 µF and its ESR should be less than 3.7 mΩ. Three 2-V, 470-µF, POSCAP capacitors from Sanyo are used. The ESR is 10 mΩ each.

The required input capacitance is calculated in equation (5). The calculated value is approximately 348 µF. Three 6.0-V, 330-µF POSCAP capacitors with 10 mΩ ESR are used to handle 10 A of RMS input current. Additionally, two ceramic capacitors are used to reduce the switching ripple current.

$$C_{IN(min)} = I_{OUT(max)} \times D_{(max)} \times \frac{T_S}{V_{RIPPLE}} \tag{7}$$

REFERENCE DESIGN

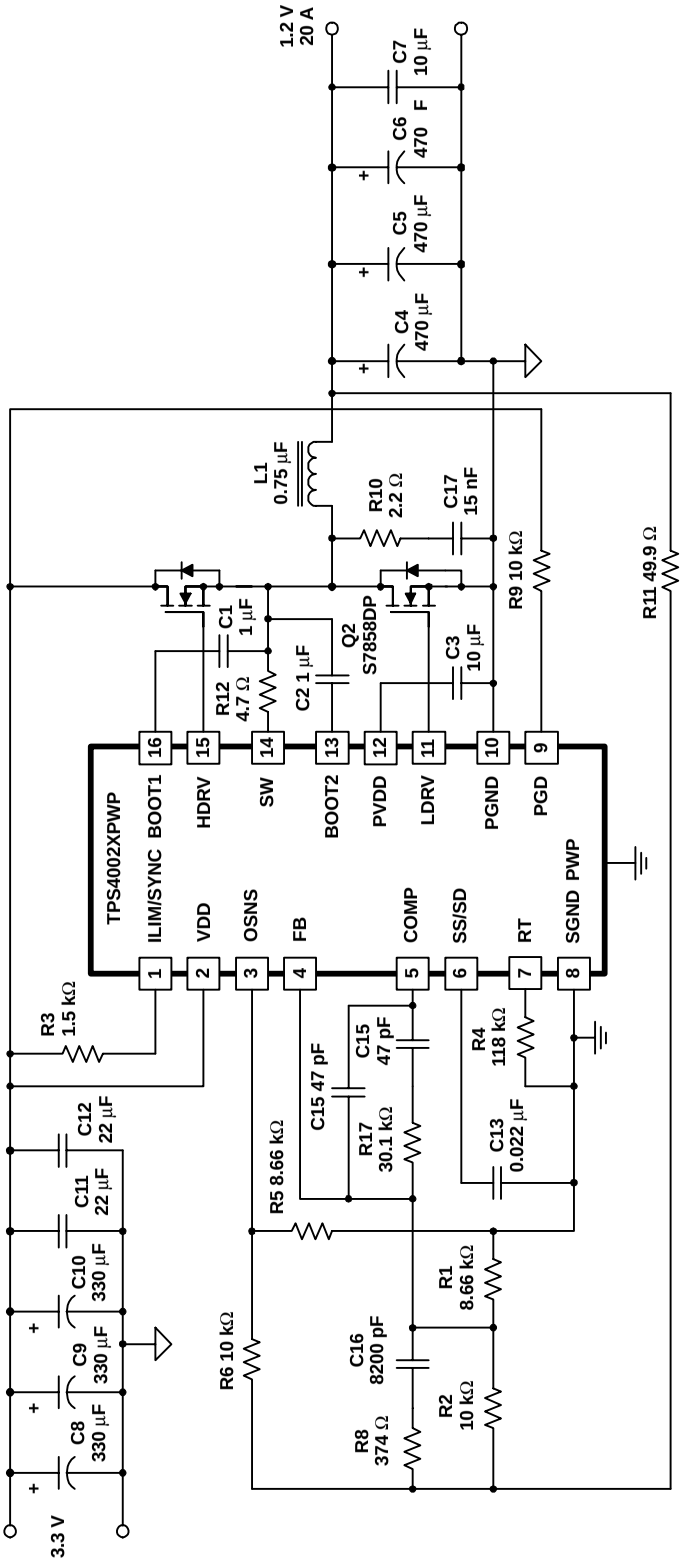


Figure 9. Reference Design Schematic

REFERENCE DESIGN

Input and Output Capacitors

The output capacitance and its ESR needed are calculated in equations (5) and (6).

Compensation Design

Voltage-mode control is used in this evaluation module, using R2, R7, R8, C14, C15, and C16 to form a Type-III compensator network. The L-C frequency of the power stage is approximately 4.9-kHz and the ESR-zero is around 34 kHz. The overall crossover frequency, f_{0db}, is chosen at 43-kHz for reasonable transient response and stability. Two zeros f_{Z1} and f_{Z2} from the compensator are set at 2.4 kHz and 1.9 kHz. The two poles, f_{P1} and f_{P2} are set at 52 kHz and 115 kHz. The frequency of poles and zeros are defined by the following equations:

$$f_{Z1} = \frac{1}{2\pi \times R7 \times C14} \quad (8)$$

$$f_{Z2} = \frac{1}{2\pi \times R2 \times C11} \quad \text{(assuming } R2 \gg R8\text{)} \quad (9)$$

$$f_{P1} = \frac{1}{2\pi \times R8 \times C11} \quad (10)$$

$$f_{P2} = \frac{1}{2\pi \times R7 \times C12} \quad \text{(assuming } C14 \gg C12\text{)} \quad (11)$$

The transfer function for the compensator is calculated in equation (10).

$$A(s) = \frac{(1 + s \times C14 \times R7) \times [1 + s \times C11 \times (R2 + R3)]}{s \times R2 \times C14 \times \left[\left(1 + \frac{C12}{C14}\right) + s \times R7 \times C12\right] \times (1 + s \times R8 \times C11)} \quad (12)$$

Figure 15 shows the close loop gain and phase. The overall crossover frequency is approximately 43 kHz. The phase margin is 60°.

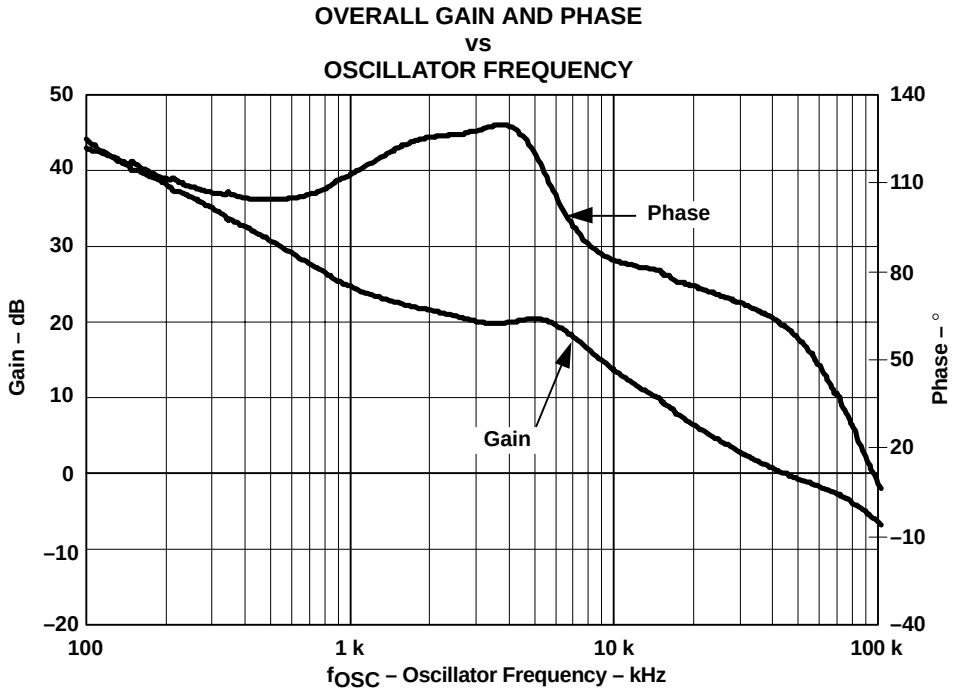


Figure 10.

REFERENCE DESIGN

MOSFETs and Diodes

For a 1.5-V output voltage, the lower the $R_{DS(on)}$ of the MOSFET, the higher the efficiency. Due to the high current and high conduction loss, the MOSFET should have very low conduction resistance ($R_{DS(on)}$) and thermal resistance. Si7858DP is chosen for its low $R_{DS(on)}$ (between 3 mΩ and 4 mΩ) and Power-Pak package.

Current Limiting

Resistor R3 sets the over current limit threshold. The $R_{DS(on)}$ of the upper MOSFET is used as a current sensor. The current limit is initialized at 40% above the maximum output current, $I_{OUT(max)}$, which is 28 A. Then R3 can be calculated in equation (11) and yields a value of 1.43 kΩ.

$$I_{LIM} = \left(20 \times \frac{V_{REF}}{R4}\right) = \left(20 \times \frac{0.7\ V}{118\ k\Omega}\right) = 118.6\ (\mu A) \tag{13}$$

$$R3 = \frac{K \times R_{DS(on)} \times I_{OUT}}{I_{LIM}\ (\mu A)} = \frac{1.5 \times 4\ (\mu\Omega) \times 28\ A}{I_{LIM}\ (\mu A)} = 1.43\ (k\Omega) \tag{14}$$

where

- $R_{DS(on)}$ is the on-resistor of Q1 (4 mΩ)
- Temperature coefficient, K=1.5
- V_{REF}=0.7 V
- R4=118 kΩ

Voltage Sense Regulator

R1 and R2 operate as the output voltage divider. The internal reference voltage (V_{REF}) is 0.7 V. The relationship between the output voltage and divider is described in equation (8). Using a 10-kΩ resistor for R2 and 1.5-V output regulation, R1 is calculated as 8.66 kΩ.

$$\frac{V_{REF}}{R1} = \frac{V_{OUT}}{R1 + R2} = \frac{0.7\ V}{R1} = \frac{1.5\ V}{R1 + 10\ k\Omega} = 8.66\ k\Omega \tag{15}$$

Transient Comparator

The output voltage transient comparators provide a quick response, first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin, using R5 and R6 shown in Figure 6. If an overvoltage condition is detected, the HDRV gate drive is shut off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed, the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. The voltage divider should keep same ratio as the output voltage sensor for the PWM comparator. Resistor R5=8.66 kΩ and R6=10 kΩ in this evaluation module.

REFERENCE DESIGN

TEST RESULTS

Efficiency Curves

The tested efficiency at different loads and input voltages are shown in Figure 16. The maximum efficiency is as high as 92.4% at 1.5-V output. The efficiency is around 87.7% when the load current (I_{LOAD}) is 20 A.

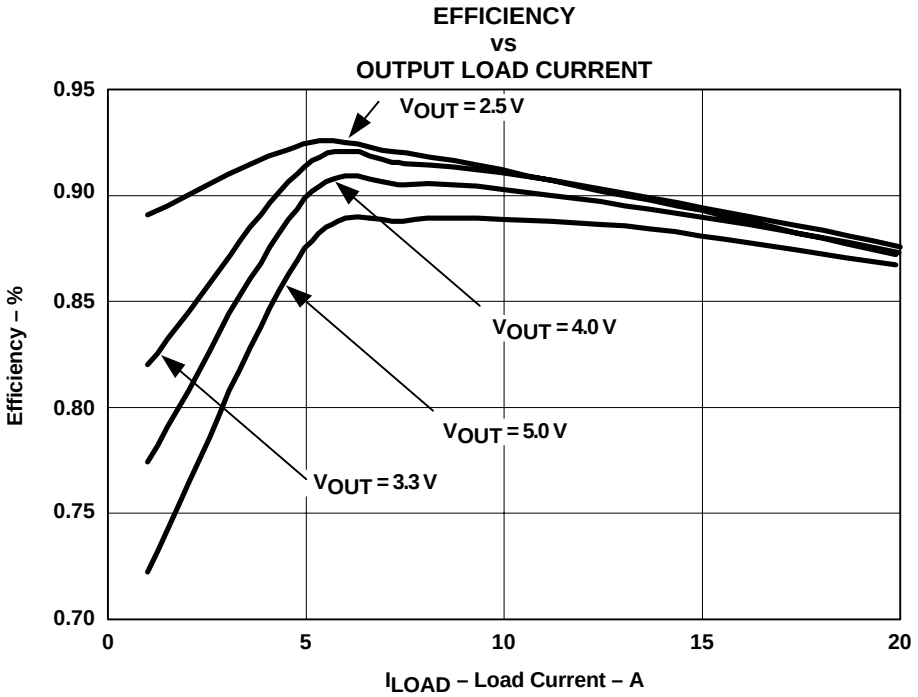


Figure 11.

Typical Operating Waveforms

Typical operating waveforms are shown in Figure 17 and 18.

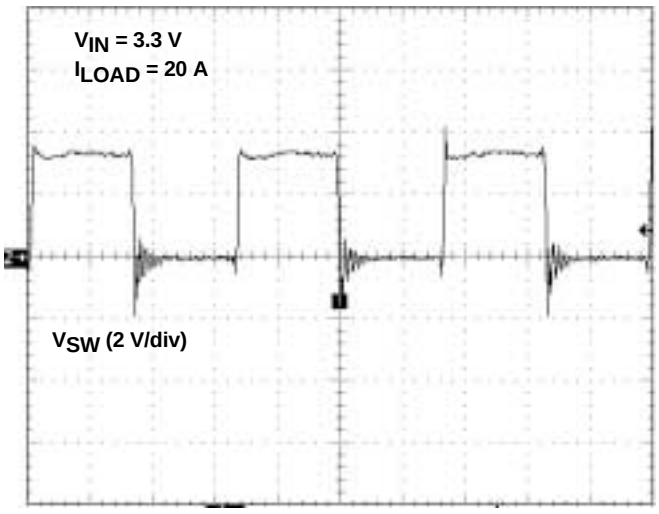


Figure 12

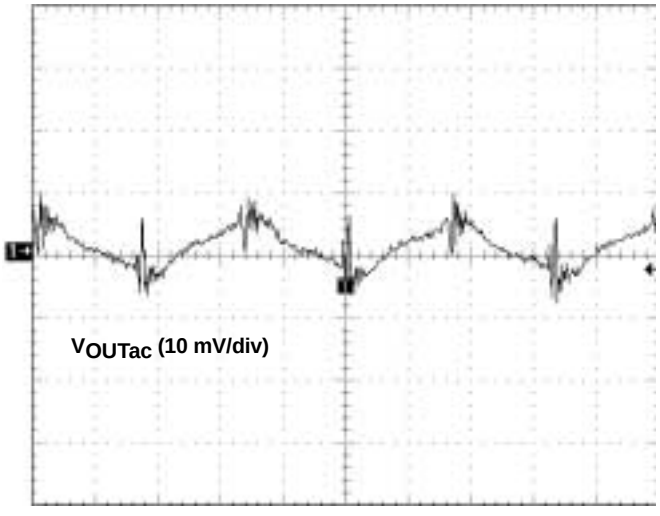


Figure 13

REFERENCE DESIGN

Transient Response and Output Ripple Voltage

The output ripple is about 15 V_{P_P} at 20-A output. When the load changes from 4 A to 20 A, the overshooting voltage is about 35 mV.

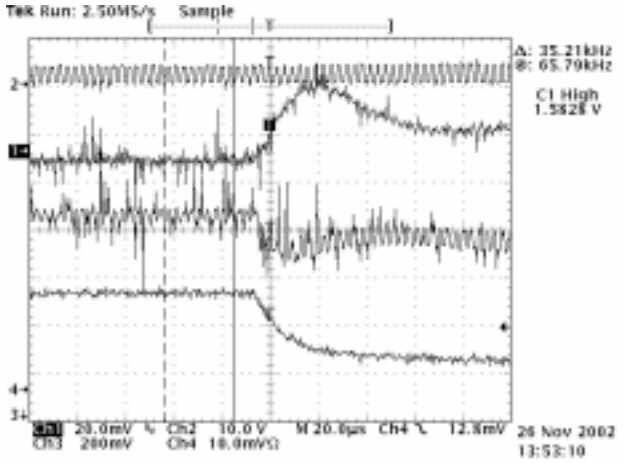


Figure 14

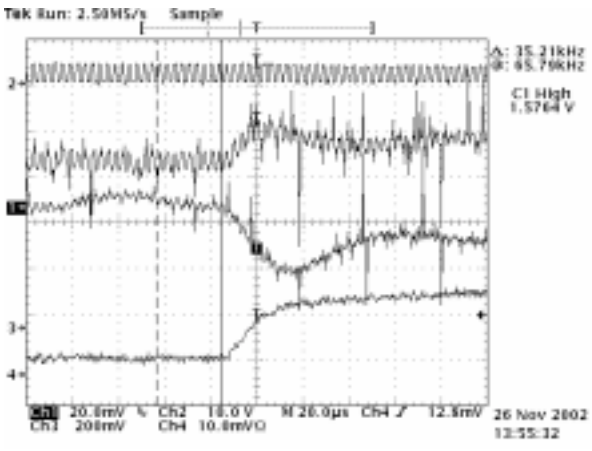
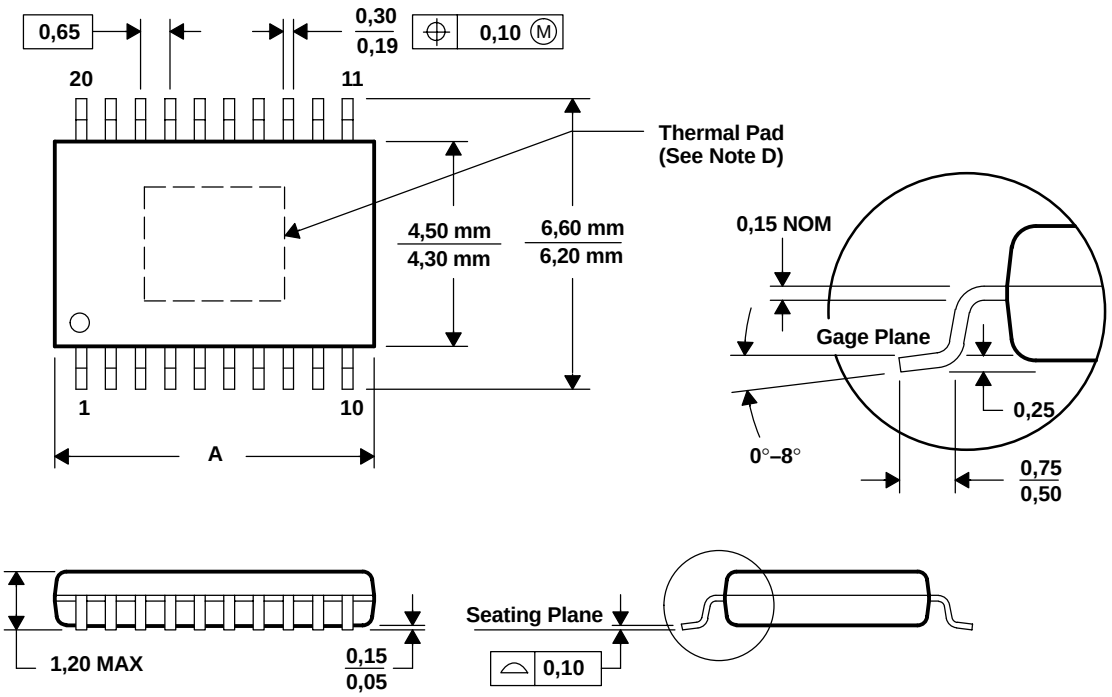


Figure 15

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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Mailing Address:

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Post Office Box 655303
Dallas, Texas 75265

TPS40021, Enhanced Low Input Voltage (2.25V-5.5V) Buck

DEVICE STATUS: **PREVIEW**

FEATURES

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- Operating Input Voltage 2.25 V to 5.5 V
- Output Voltage as Low as 0.7 V
- 1% Internal 0.7 V Reference
- Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency
- Externally Adjustable Soft-Start and Overcurrent Limit
- Programmable Fixed-Frequency
  100 KHz-to-1 MHz Voltage-Mode Control
- Source-Only Current or Source/Sink Current
- Quick Response Output Transient Comparators with Power Good Indication Provide Output Status
- 16-Pin PowerPAD™ Package ($_{JA}$ = 2°C/W)
- APPLICATIONS
  - Networking Equipment
  - Telecom Equipment
  - Base Stations
  - Servers
  - DSP Power

DESCRIPTION

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The TPS4002x family of dc-to-dc controllers are designed for non-isolated synchronous buck regulators, providing enhanced operation and design flexability through user programmability.

The TPS4002x utilizes a proprietary Predictive Gate Drive™ architecture to minimize the diode conduction losses associated with the high-side and synchronous rectifier N-channel MOSFET transistions. The integrated charge pump with boost circuit provides a regulated 5-V gate drive for both the high side and synchronous rectifier N-channel MOSFETs. The use of the Predictive Gate Drive™ and charge pump/boost circuits combine to provide a highly efficient, smaller and less expensive converter.

Design flexibility is provided through user programmability of such functions as: operating frequency, overcurrent detection thresholds, soft-start ramp time, and external synchronization frequency. The operating frequency is programmable using a single resistor over a frequency range of 100 kHz to 1 MHz. Higher operating frequencies yield smaller component values for a given converter power level as well as faster loop closure.

The overcurrent detection is programmable through a single resistor. Programmable overcurrent limit allows the detection threshold to be easily tailored to accommodate different size ($R_{DS(on)}$) MOSFETs. The overcurrent function provides pulse-by-pulse current limiting during soft-start and short term transient conditions as well as a fault counter to handle longer duration overcurrent conditions. If a fault is detected the controller shuts down for a period of time determined by six (6) consecutive soft-start cycles. The controller automatically retries the output every seventh (7^{th}) soft-start cycle.

In addition to determining the off time during a fault condition, the soft-start ramp provides a closed loop controlled ramp of the converter output during startup. Programmability allows the ramp rate to be adjusted for a wide variety of output L-C component values.

The output voltage transient comparators provide a quick response, first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin. If an overvoltage condition is detected the HDRV gate drive is shut-off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. In either case, the PowerGood open drain output pulls low to indicate an output voltage out of regulation condition. The PowerGood output can be daisy-chained to the SS/SD pin or enable pin of other controllers or converters. The transient comparators can be disabled by simply tying the OSNS pin to VDD.

The TPS4002X can be externally synchronized through the ILIM/SYNC pin up to 1.5× the free-running frequency. This allows multiple contollers to be synchronized to eliminate EMI concerns due to input beat frequencies between controllers.

Product Folder: TPS40021, Enhanced Low Input Voltage (2.25V-5.5V) Buck

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: tps40021.pdf (199 KB) (Updated: 07/01/2002)

APPLICATION NOTES

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- Analog Applications Journal (Rev. A) (SLYT010A - Updated: 03/17/2000)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Portable/System Power Sales Tool Brochure 3Q 2002 (SLPB006, 153 KB - Updated: 08/23/2002)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
TPS40021PWP	PREVIEW	HTSSOP (PWP) | 16		View Contents	1KU |	
TPS40021PWPR	PREVIEW	HTSSOP (PWP) | 16		View Contents	1KU |	

TI INVENTORY STATUS
As Of 10:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*		Call**
0*		Call**

REPORTED DISTRIBUTOR INVENTORY
As Of 10:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		

Table Data Updated on: 4/17/2003

TPS40020, Enhanced Low Input Voltage (2.25V-5.5V) Buck

DEVICE STATUS: **PREVIEW**

FEATURES

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- Operating Input Voltage 2.25 V to 5.5 V
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- 1% Internal 0.7 V Reference
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  100 KHz-to-1 MHz Voltage-Mode Control
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The overcurrent detection is programmable through a single resistor. Programmable overcurrent limit allows the detection threshold to be easily tailored to accommodate different size ($R_{DS(on)}$) MOSFETs. The overcurrent function provides pulse-by-pulse current limiting during soft-start and short term transient conditions as well as a fault counter to handle longer duration overcurrent conditions. If a fault is detected the controller shuts down for a period of time determined by six (6) consecutive soft-start cycles. The controller automatically retries the output every seventh (7^{th}) soft-start cycle.

In addition to determining the off time during a fault condition, the soft-start ramp provides a closed loop controlled ramp of the converter output during startup. Programmability allows the ramp rate to be adjusted for a wide variety of output L-C component values.

The output voltage transient comparators provide a quick response, first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin. If an overvoltage condition is detected the HDRV gate drive is shut-off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. In either case, the PowerGood open drain output pulls low to indicate an output voltage out of regulation condition. The PowerGood output can be daisy-chained to the SS/SD pin or enable pin of other controllers or converters. The transient comparators can be disabled by simply tying the OSNS pin to VDD.

The TPS4002X can be externally synchronized through the ILIM/SYNC pin up to 1.5× the free-running frequency. This allows multiple contollers to be synchronized to eliminate EMI concerns due to input beat frequencies between controllers.

Product Folder: TPS40020, Enhanced Low Input Voltage (2.25V-5.5V) Buck

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To view the following documents, Acrobat Reader 4.0 is required.
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DATASHEET

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Full datasheet in Acrobat PDF: tps40020.pdf (199 KB) (Updated: 07/01/2002)

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- Analog Applications Journal (Rev. A) (SLYT010A - Updated: 03/17/2000)

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Portable/System Power Sales Tool Brochure 3Q 2002 (SLPB006, 153 KB - Updated: 08/23/2002)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

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DEVICE INFORMATION Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
TPS40020PWP	PREVIEW	HTSSOP (PWP) | 16		View Contents	1KU |	
TPS40020PWPR	PREVIEW	HTSSOP (PWP) | 16		View Contents	1KU |	

TI INVENTORY STATUS As Of 10:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*		Call**
0*		Call**

REPORTED DISTRIBUTOR INVENTORY As Of 10:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		

Table Data Updated on: 4/17/2003

TPS40022, Enhanced Low Input Voltage (2.25V-5.5V) Buck

DEVICE STATUS: **PREVIEW**

FEATURES

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- Operating Input Voltage 2.25 V to 5.5 V
- Output Voltage as Low as 0.7 V
- 1% Internal 0.7 V Reference
- Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency
- Externally Adjustable Soft-Start and Overcurrent Limit
- Programmable Fixed-Frequency
  100 KHz-to-1 MHz Voltage-Mode Control
- Source-Only Current or Source/Sink Current
- Quick Response Output Transient Comparators with Power Good Indication Provide Output Status
- 16-Pin PowerPAD™ Package ($_{JA}$ = 2°C/W)
- APPLICATIONS
  - Networking Equipment
  - Telecom Equipment
  - Base Stations
  - Servers
  - DSP Power

DESCRIPTION

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The TPS4002x family of dc-to-dc controllers are designed for non-isolated synchronous buck regulators, providing enhanced operation and design flexability through user programmability.

The TPS4002x utilizes a proprietary Predictive Gate Drive™ architecture to minimize the diode conduction losses associated with the high-side and synchronous rectifier N-channel MOSFET transistions. The integrated charge pump with boost circuit provides a regulated 5-V gate drive for both the high side and synchronous rectifier N-channel MOSFETs. The use of the Predictive Gate Drive™ and charge pump/boost circuits combine to provide a highly efficient, smaller and less expensive converter.

Design flexibility is provided through user programmability of such functions as: operating frequency, overcurrent detection thresholds, soft-start ramp time, and external synchronization frequency. The operating frequency is programmable using a single resistor over a frequency range of 100 kHz to 1 MHz. Higher operating frequencies yield smaller component values for a given converter power level as well as faster loop closure.

The overcurrent detection is programmable through a single resistor. Programmable overcurrent limit allows the detection threshold to be easily tailored to accommodate different size ($R_{DS(on)}$) MOSFETs. The overcurrent function provides pulse-by-pulse current limiting during soft-start and short term transient conditions as well as a fault counter to handle longer duration overcurrent conditions. If a fault is detected the controller shuts down for a period of time determined by six (6) consecutive soft-start cycles. The controller automatically retries the output every seventh (7^{th}) soft-start cycle.

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Product Folder: TPS40022, Enhanced Low Input Voltage (2.25V-5.5V) Buck

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TPS40022PWPR	PREVIEW	HTSSOP (PWP) | 16		View Contents	1KU |	

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