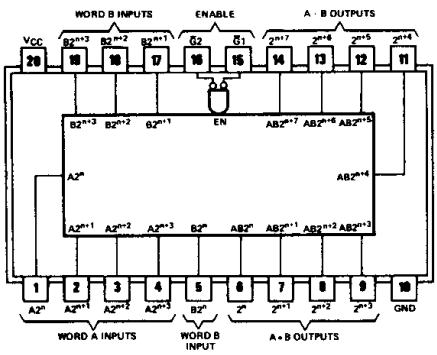
TYPES SN54LS275, SN54S274, SN54S275, SN74LS275, SN74S274, SN74S275
4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS
7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612121, OCTOBER 1976

- 'S274 Provides 8-Bit Product in Typically 45 ns
- 'S274 Can Provide Sub-Multiple Products for n-Bit-by-n-Bit Binary Numbers
- 'LS275 and 'S275 Accept 7 Bit-Slice Inputs and 2 Carry Inputs for Reduction to 4 Lines in Typically 45 ns
- These High-Complexity Functions Can Reduce Package Count by Nearly 50% in Most Parallel Multiplier Designs
- When SN74S274 is Combined With SN74H183 (or SN74LS183) and Schottky Look-Ahead Adders, Multiplication Times are Typically:

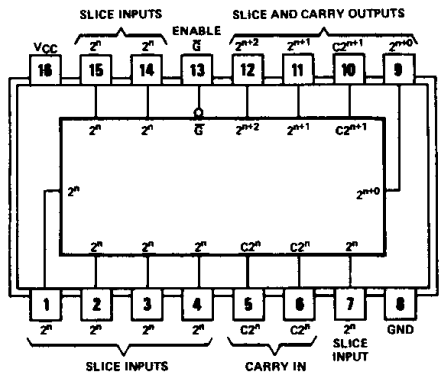
  16-Bit Product in 75 ns (79 ns)
  32-Bit Product in 116 ns (132 ns)

SN54S274 . . . J PACKAGE
SN74S274 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: When either (or both) $\overline{G}$ input(s) is (are) high, all eight outputs are off.

SN54LS275, SN54S275 . . . J PACKAGE
SN74LS275, SN74S275 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: When $\overline{G}$ is high, all four outputs are off.

description

These high-complexity Schottky-clamped TTL circuits are designed specifically to reduce the delay time required to perform high-speed parallel binary multiplication and significantly reduce package count. The 'S274 is a basic 4-bit-by-4-bit parallel multiplier in a single package, and as such, no additional components are required to obtain an 8-bit product. For word lengths longer than 4 bits, a number of 'S274 multipliers can be combined to generate sub-multiple partial products. These partial products can then be combined in Wallace trees to obtain the final product. See Typical Application Data.

The 'LS275 and 'S275 expandable bit-slice Wallace trees have been designed to accept up to seven bit-slice inputs and two carry inputs from previous slices for reduction to four lines.

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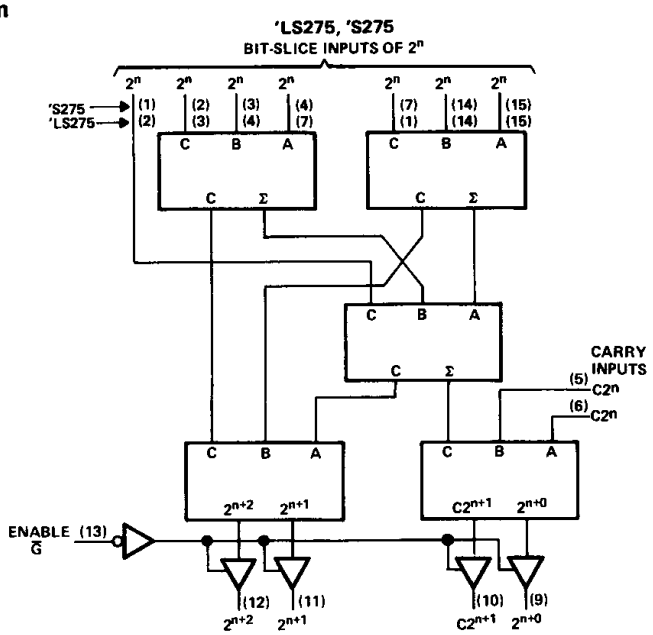
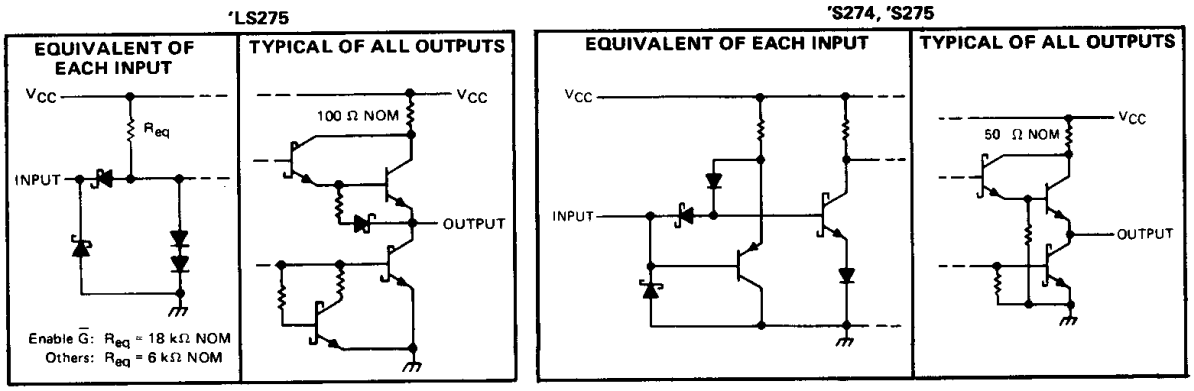
functional block diagram



NOTE: When one of of the $C2^n$ carry inputs is not used, it must be grounded. If neither $C2^n$ carry input is used, both $C2^n$ inputs are grounded and the $C2^{n+1}$ output is normally left open.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS275	7 V
'S274, 'S275	5.5 V
Off-state output voltage: 'LS275	7 V
'S274, 'S275	5.5 V
Operating free-air temperature range: SN54LS, SN54S Circuits	−55°C to 125°C
SN74LS, SN74S Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

	SN54LS275			SN74LS275			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS275			SN74LS275			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.2		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−20			−20	μA
I_I	Input current at maximum input voltage	Enable $\overline{G}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		All others					0.3			0.3	
I_{IH}	High-level input current	Enable $\overline{G}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		All others					60			60	
I_{IL}	Low-level input current	Enable $\overline{G}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−1.2			−1.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX			25	40		25	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any Slice or Carry	Any	C_L = 45 pF, R_L = 667 Ω, See Note 2		35	62	ns
t_{PHL}					42	66	
t_{PZH}	Enable $\overline{G}$	Any	C_L = 45 pF, R_L = 667 Ω, See Note 2		8	23	ns
t_{PZL}					13	23	
t_{PHZ}			C_L = 5 pF, R_L = 667 Ω, See Note 2		10	15	ns
t_{PLZ}					10	15	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54S274 SN54S275			SN74S274 SN74S275			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S274 SN54S275			SN74S274 SN74S275			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			105	155		105	155	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S274 SN54S275			SN74S274 SN74S275			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PHL}	Any A or B ('S274), or Any Slice or Carry ('S275)	Any	C_L = 30 pF, R_L = 400 Ω, See Note 3		50	95		50	70	ns
t_{PLH}					50	95		50	70	
t_{PZH}	Any Enable	Any	C_L = 5 pF, R_L = 400 Ω, See Note 3		15	45		15	30	ns
t_{PZL}					15	45		15	30	
t_{PHZ}					10	40		10	25	ns
t_{PLZ}					10	40		10	25	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

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TYPICAL APPLICATION DATA

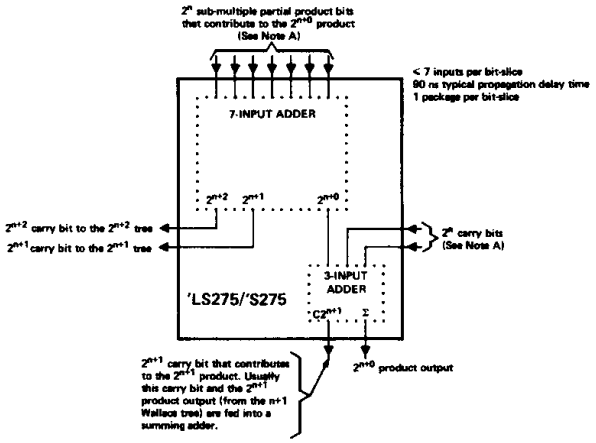


FIGURE 1—BASIC BIT-SLICE WALLACE TREE

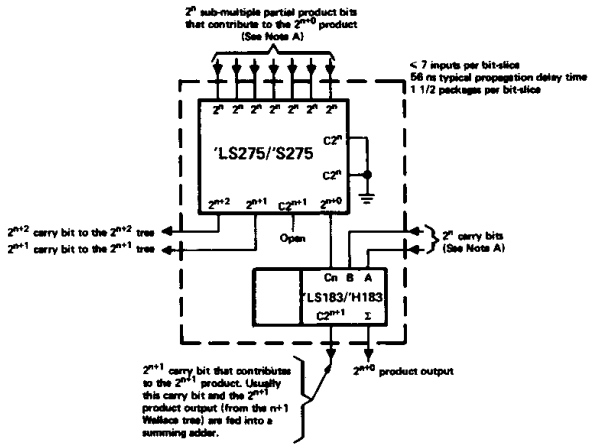


FIGURE 2—HIGH-SPEED BIT-SLICE WALLACE TREE

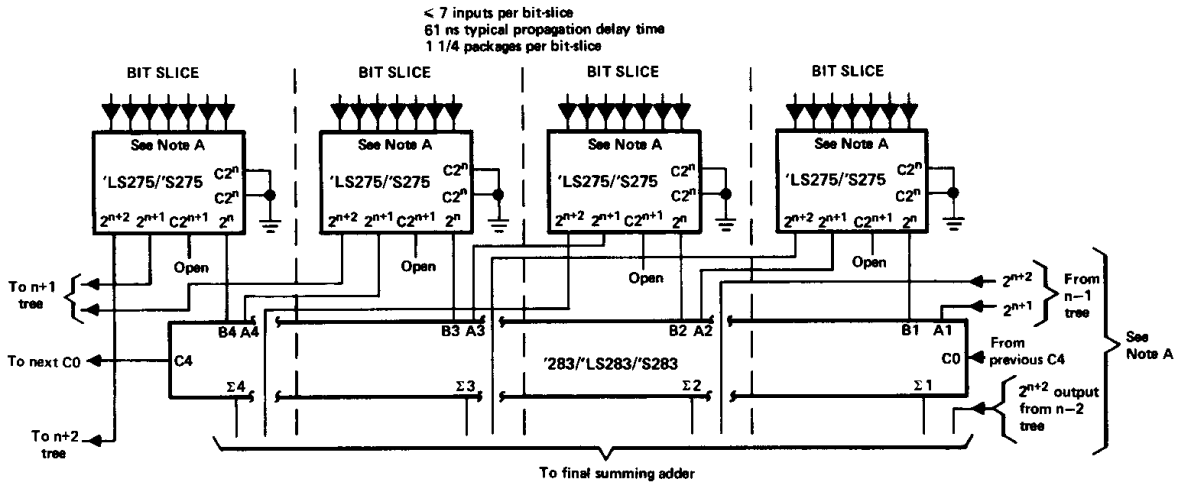
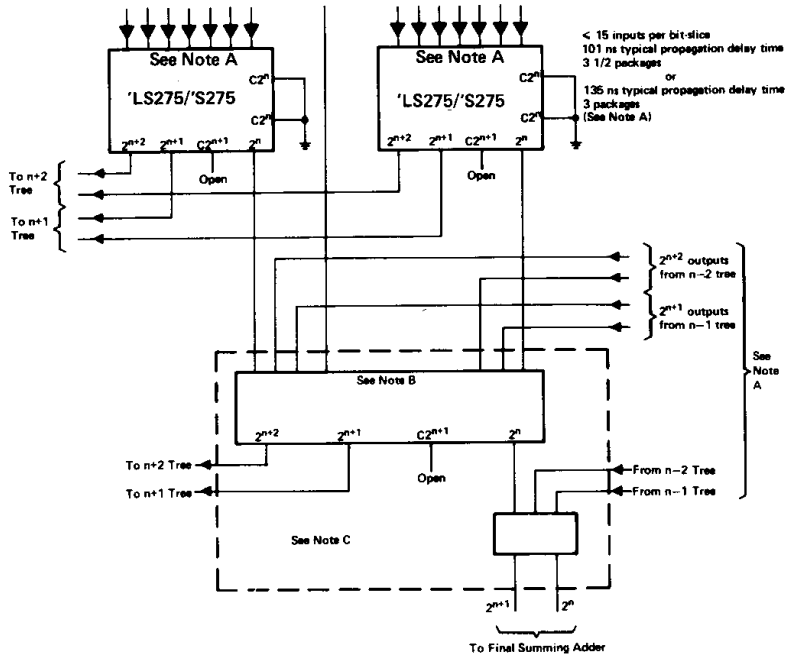


FIGURE 3—MODERATE-SPEED BIT-SLICE WALLACE TREE

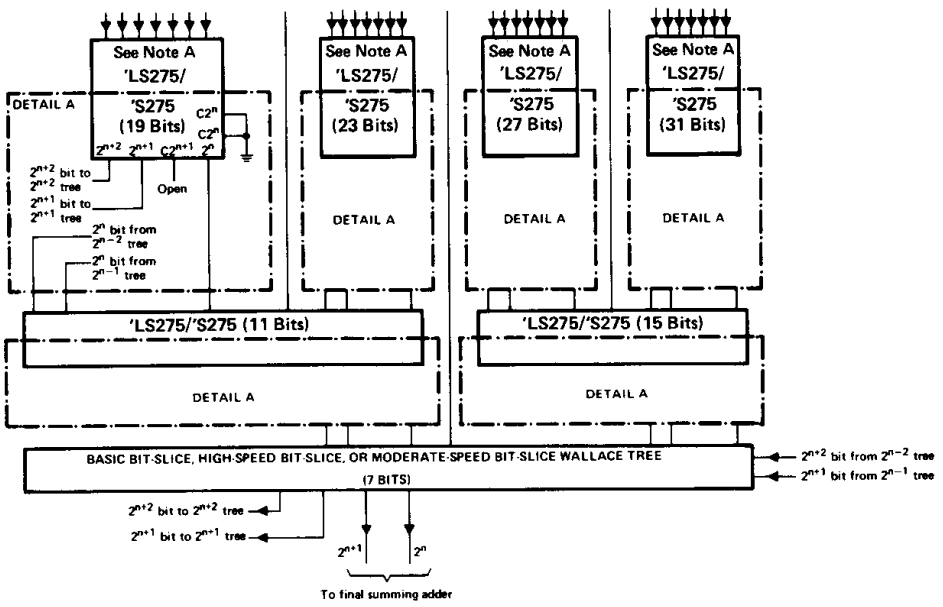
NOTE A: All unused inputs must be grounded.

TYPICAL APPLICATION DATA



NOTES: A. Ground unused inputs.
B. These outputs from preceeding trees may go to any of the inputs of the 'LS275/'S275.
C. The circuit within the dotted lines may be either the basic bit-slice Wallace tree or the high-speed Wallace tree. In the latter case both carry inputs of the 'LS275/'S275 must be grounded.

FIGURE 4—15-BIT-SLICE WALLACE TREE FOR 32-BIT X 32-BIT MULTIPLIER



NOTES: A. Ground unused inputs.
B. The number of bits in parentheses is the maximum number of bits this tree can combine if the remaining 'LS275/'S275 (all having a higher number in the parentheses) were not connected.

FIGURE 5—7-TO-31-BIT-SLICE WALLACE TREE FOR UP TO 64-BIT X 64-BIT MULTIPLIERS

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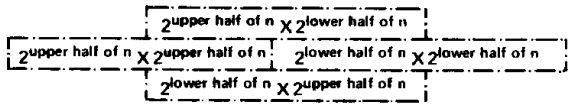
TYPICAL APPLICATION DATA



NOTE A: The left-hand half of each rectangle is the portion of word one used to obtain the product shown within the rectangle. Similarly, the right-hand half of each rectangle is the portion of word two used.

FIGURE 6—UNIVERSAL METHOD OF ADDING $\frac{n}{2}$-BIT PRODUCTS TO OBTAIN AN n-BIT PRODUCT

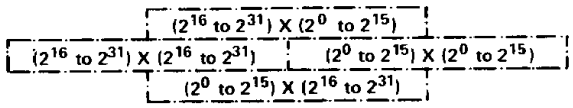


FIGURE 7—METHOD OF ADDING 32-BIT PRODUCTS TO OBTAIN A 64-BIT PRODUCT

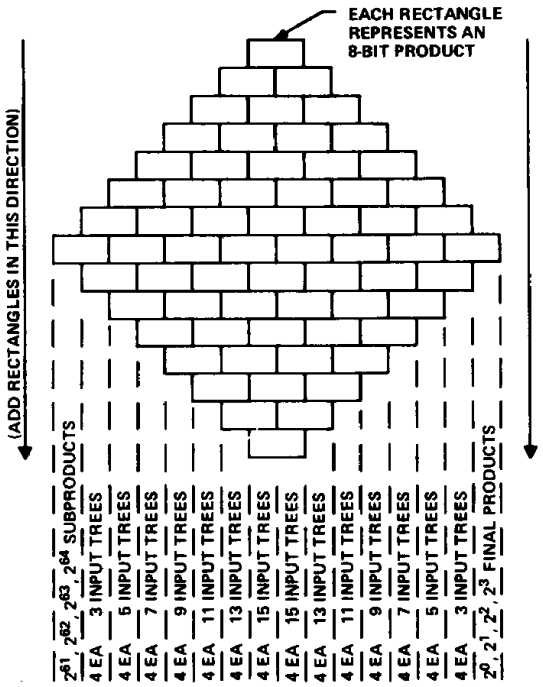
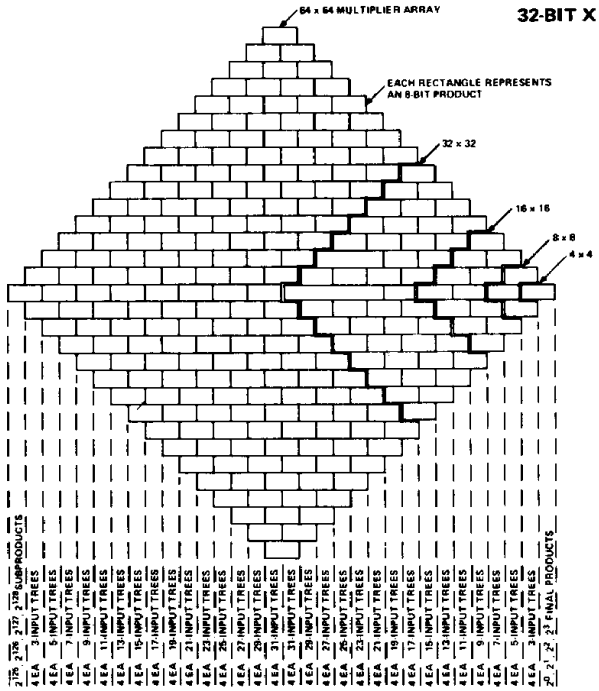


FIGURE 8—FINAL PRODUCTS AND ARRAY SUBPRODUCT ADDITIONS FOR 32-BIT X 32-BIT MULTIPLIER



NOTE A: See Note B of Figure 6 for designing trees with any number of inputs up to 31.

FIGURE 9—ARRAY ARRANGEMENT FOR VARIOUS MULTIPLIERS INCLUDING ARRAY SUBPRODUCT ADDITIONS FOR 64-BIT X 64-BIT MULTIPLIER

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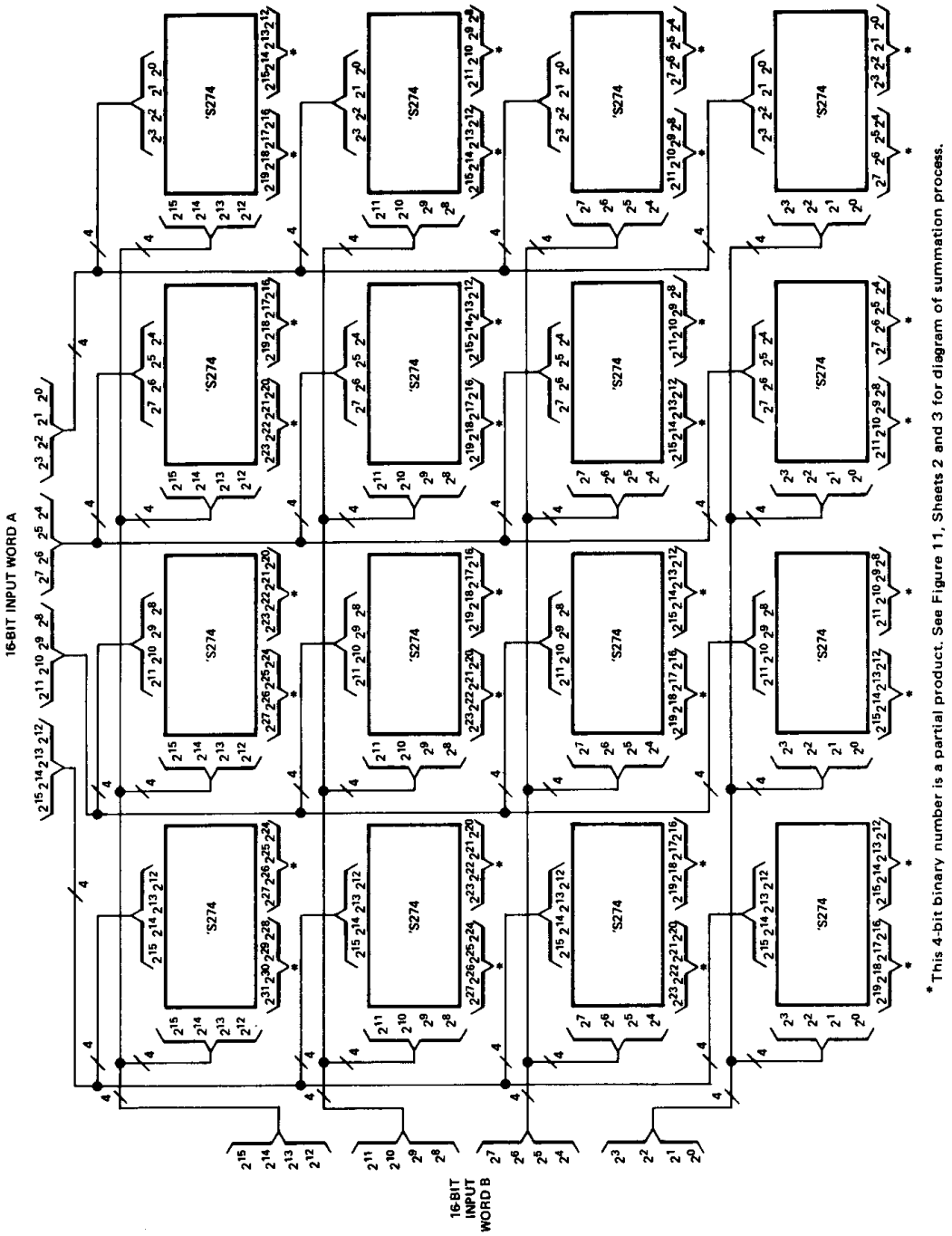
TYPICAL APPLICATION DATA



*This 4-bit binary number is a partial product. See Figure 11, Sheets 2 and 3 for diagram of summation process.

FIGURE 10–16-BIT X 16-BIT MULTIPLIER (SHEET 1 OF 3–OUTPUT CONNECTIONS)

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TYPICAL APPLICATION DATA

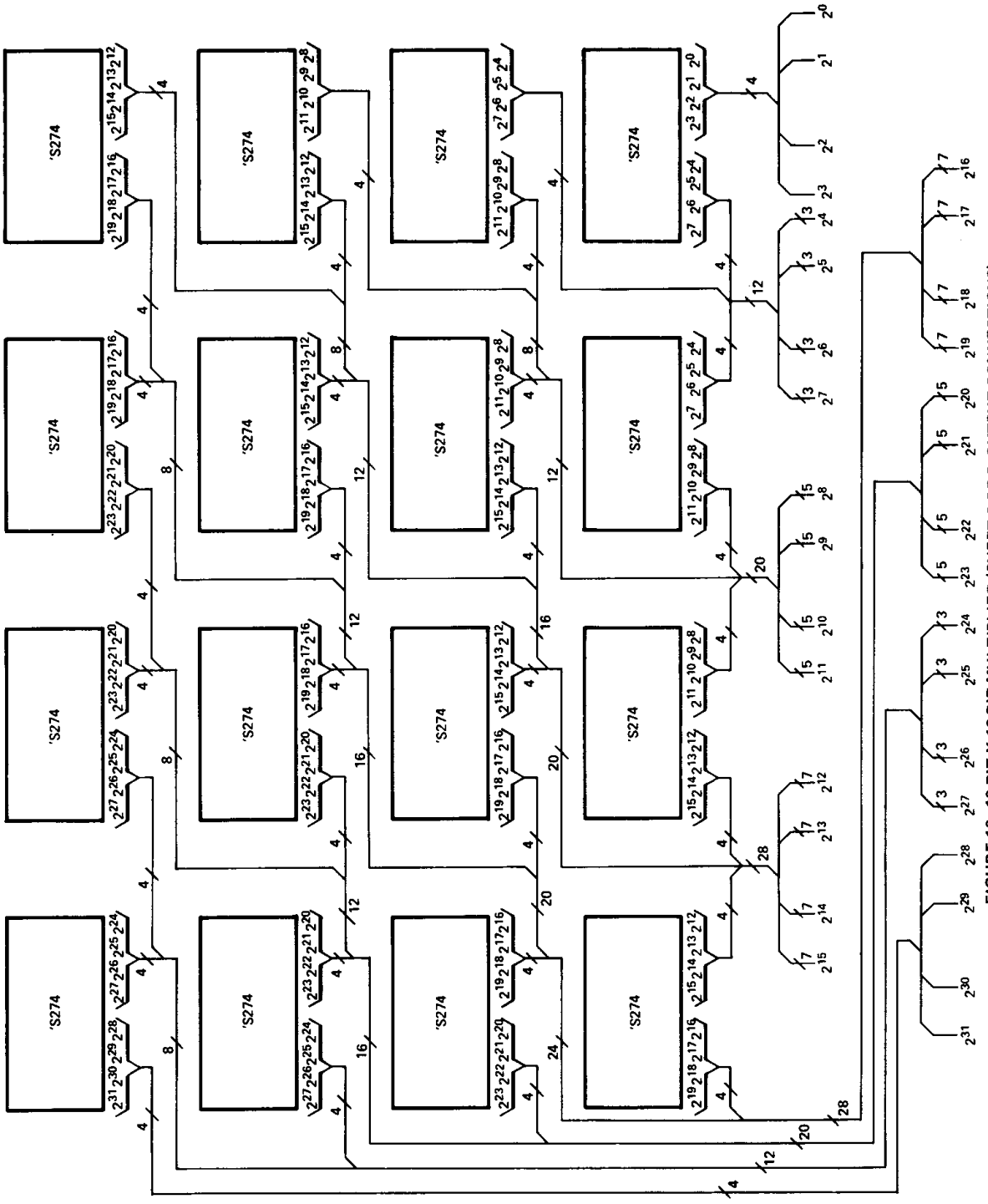
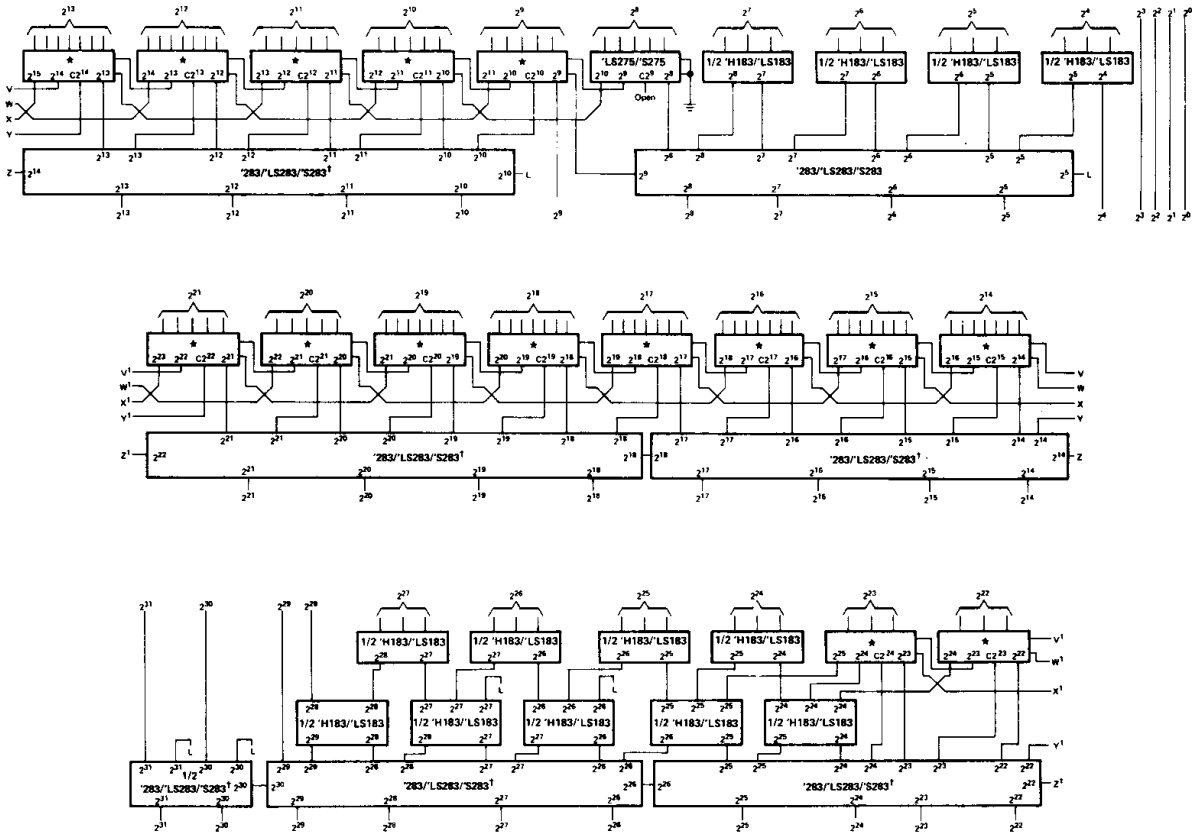


FIGURE 10—16-BIT X 16-BIT MULTIPLIER (SHEET 2 OF 3—OUTPUT CONNECTIONS)

TYPICAL APPLICATION DATA



*Each starred block may be either a basic bit-slice Wallace tree('LS275 or 'S275 only) or a high-speed bit-slice Wallace tree ('LS275 plus 1/2 'LS183 or 'S275 plus 1/2 'H183). In either case the function of the terminal is the same as the similarly located terminal of the basic bit-slice (Figure 1) or high-speed bit-slice Wallace tree (Figure 2). Also for either tree, when only five inputs of the seven-input adder of the 'LS275/'S275 are used, the remaining two inputs must be grounded. When the high-speed adder is used, the $C2^n$ inputs of the 'LS275/'S275 must be grounded.

†For improved performance SN74LS181/SN74S181 ALUs with SN74S182 look-ahead generators can be substituted for the SN74283/SN74LS283/SN74S283 adders. Typically, the multiplication time will be reduced by 18 to 32 nanoseconds.

FIGURE 10–16-BIT X 16-BIT MULTIPLIER
(SHEET 3 OF 3–SUMMING PARTIAL PRODUCTS)

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